System Extension Data Book

- CPU Supervisors
- Digital Potentiometers
- Silicon Timed Circuits
- Thermal Products

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TABLE OF CONTENTS

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS0620	SOFTWARE	N/A	DS0620	TMEX
DS1000	14–Pin DIP	0 to 70	DS1000–xxx	xxx = 020 to 500 ns
	14–Pin DIP Sheared NC	0 to 70	DS1000K–xxx	xxx = 020 to 500 ns
	8–Pin DIP	0 to 70	DS1000M–xxx	xxx = 020 to 500 ns
	14–Pin GULLWING	0 to 70	DS1000G–xxx	xxx = 020 to 500 ns
	8–Pin GULLWING	0 to 70	DS1000H–xxx	xxx = 020 to 500 ns
	16–Pin SOIC	0 to 70	DS1000S–xxx	xxx = 020 to 500 ns
	8–Pin SOIC	0 to 70	DS1000Z–xxx	xxx = 020 to 500 ns
DS1003	8-Pin DIP	0 to 70	DS1003M–16	
	8–Pin DIP	0 to 70	DS1003M–20	
	8–Pin DIP	0 to 70	DS1003M–25	
	8–Pin DIP	0 to 70	DS1003M–33	
	8–Pin DIP	0 to 70	DS1003M–40	
	8–Pin GULLWING	0 to 70	DS1003H–16	
	8–Pin GULLWING	0 to 70	DS1003H–20	
	8–Pin GULLWING	0 to 70	DS1003H–25	
	8–Pin GULLWING	0 to 70	DS1003H–33	
	8–Pin GULLWING	0 to 70	DS1003H–40	
	14–Pin DIP	0 to 70	DS1003–16	
	14–Pin DIP	0 to 70	DS1003–20	
	14–Pin DIP	0 to 70	DS1003–25	
	14–Pin DIP	0 to 70	DS1003–33	
	14–Pin DIP	0 to 70	DS1003–40	
	14–Pin GULLWING	0 to 70	DS1003G–16	
	14–Pin GULLWING	0 to 70	DS1003G–20	
	14–Pin GULLWING	0 to 70	DS1003G–25	
	14–Pin GULLWING	0 to 70	DS1003G–33	
	14–Pin GULLWING	0 to 70	DS1003G–40	
DS1004	8–Pin DIP	0 to 70	DS1004M–002	13 ns total delay
	8–Pin DIP	0 to 70	DS1004M–003	17 ns total delay
	8–Pin DIP	0 to 70	DS1004M–004	21 ns total delay
	8–Pin DIP	0 to 70	DS1004M–005	25 ns total delay
	8–Pin SOIC	0 to 70	DS1004Z–002	13 ns total delay
	8–Pin SOIC	0 to 70	DS1004Z–003	17 ns total delay
	8–Pin SOIC	0 to 70	DS1004Z–004	21 ns total delay
	8–Pin SOIC	0 to 70	DS1004Z–005	25 ns total delay
DS1005	14–Pin DIP	0 to 70	DS1005–xxx	xxx = 060 to 250 ns
	14–Pin DIP Sheared NC	0 to 70	DS1005K–xxx	xxx = 060 to 250 ns
	8–Pin DIP	0 to 70	DS1005M–xxx	xxx = 060 to 250 ns
	14–Pin GULLWING	0 to 70	DS1005G–xxx	xxx = 060 to 250 ns
	8–Pin GULLWING	0 to 70	DS1005H–xxx	xxx = 060 to 250 ns
	16–Pin SOIC	0 to 70	DS1005S–xxx	xxx = 060 to 250 ns
DS1007	16–Pin DIP	0 to 70	DS1007–xxx	xxx = 001 to 014
	16–Pin SOIC	0 to 70	DS1007S–xxx	xxx = 001 to 014

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS1010	14–Pin DIP	0 to 70	DS1010–xxx	xxx = 050 to 500 ns
	14–Pin GULLWING	0 to 70	DS1010G–xxx	xxx = 050 to 500 ns
	16–Pin SOIC	0 to 70	DS1010S–xxx	xxx = 050 to 500 ns
DS1012	8–Pin DIP	0 to 70	DS1012M–xxx	
	8–Pin GULLWING	0 to 70	DS1012H–xxx	
	8–Pin SOIC	0 to 70	DS1012Z–xxx	
DS1013	14–Pin DIP	0 to 70	DS1013–xxx	xxx = 010 to 200 ns
	8–Pin DIP	0 to 70	DS1013M–xxx	xxx = 010 to 200 ns
	14–Pin GULLWING	0 to 70	DS1013G–xxx	xxx = 010 to 200 ns
	8–Pin GULLWING	0 to 70	DS1013H–xxx	xxx = 010 to 200 ns
	14–Pin Sheared	0 to 70	DS1013K–xxx	xxx = 010 to 200 ns
	16–Pin SOIC	0 to 70	DS1013S–xxx	xxx = 010 to 200 ns
DS1020	16–Pin DIP	0 to 70	DS1020–15	0.15 ns Steps
	16–Pin DIP	0 to 70	DS1020–25	0.25 ns Steps
	16–Pin DIP	0 to 70	DS1020–50	0.50 ns Steps
	16–Pin DIP	0 to 70	DS1020–100	1.00 ns Steps
	16–Pin DIP	0 to 70	DS1020–200	2.00 ns Steps
	16–Pin SOIC	0 to 70	DS1020S–15	0.15 ns Steps
	16–Pin SOIC	0 to 70	DS1020S–25	0.25 ns Steps
	16–Pin SOIC	0 to 70	DS1020S–50	0.50 ns Steps
	16–Pin SOIC	0 to 70	DS1020S–100	1.00 ns Steps
	16–Pin SOIC	0 to 70	DS1020S–200	2.00 ns Steps
DS1033	8–Pin DIP	0 to 70	DS1033M–xxx	xxx = 008 to 030 ns
	8–Pin SOIC	0 to 70	DS1033Z–xxx	xxx = 008 to 030 ns
	20–Pin TSSOP	0 to 70	DS1033E–xxx	xxx = 008 to 030 ns
DS1035	8–Pin DIP	0 to 70	DS1035M–xxx	xxx = 006 to 030 ns
	8–Pin SOIC	0 to 70	DS1035Z–xxx	xxx = 006 to 030 ns
	20–Pin TSSOP	0 to 70	DS1035E–xxx	xxx = 006 to 030 ns
DS1040	8–Pin DIP	0 to 70	DS1040M–75	75 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–100	100 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–150	150 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–200	200 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–250	250 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–500	500 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–B50	50 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–D60	60 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–A15	15 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–A20	20 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–A32	32.5 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–B40	40 ns max pulse width
	8–Pin DIP	0 to 70	DS1040M–D70	70 ns max pulse width
	8–Pin GULLWING	0 to 70	DS1040H–75	75 ns max pulse width
	8–Pin GULLWING	0 to 70	DS1040H–100	100 ns max pulse width
	8–Pin GULLWING	0 to 70	DS1040H–150	150 ns max pulse width
	8–Pin GULLWING	0 to 70	DS1040H–200	200 ns max pulse width
	8–Pin GULLWING	0 to 70	DS1040H–250	250 ns max pulse width

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	8–Pin GULLWING	0 to 70	DS1040H–500	500 ns max pulse width
	8–Pin GULLWING	0 to 70	DS1040H–B50	50 ns max pulse width
	8–Pin GULLWING	0 to 70	DS1040H–D60	60 ns max pulse width
	8–Pin GULLWING	0 to 70	DS1040H–A15	15 ns max pulse width
	8–Pin GULLWING	0 to 70	DS1040H–A20	20 ns max pulse width
	8–Pin GULLWING	0 to 70	DS1040H–A32	32.5 ns max pulse width
	8–Pin GULLWING	0 to 70	DS1040H–B40	40 ns max pulse width
	8–Pin GULLWING	0 to 70	DS1040H–D70	70 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–75	75 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–100	100 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–150	150 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–200	200 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–250	250 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–500	500 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–B50	50 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–D60	60 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–A15	15 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–A20	20 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–A32	32.5 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–B40	40 ns max pulse width
	8–Pin SOIC	0 to 70	DS1040Z–D70	70 ns max pulse width
DS1044	14–Pin DIP	0 to 70	DS1044–xxx	xxx = 005 to 025 ns
	14–Pin GULLWING	0 to 70	DS1044G–xxx	xxx = 005 to 025 ns
	14–Pin SOIC	0 to 70	DS1044R–xxx	xxx = 005 to 025 ns
DS1045	16–Pin DIP	0 to 70	DS1045–2	2 ns Steps
	16–Pin DIP	0 to 70	DS1045–3	3 ns Steps
	16–Pin DIP	0 to 70	DS1045–4	4 ns Steps
	16–Pin DIP	0 to 70	DS1045–5	5 ns Steps
	16–Pin SOIC	0 to 70	DS1045S–2	2 ns Steps
	16–Pin SOIC	0 to 70	DS1045S–3	3 ns Steps
	16–Pin SOIC	0 to 70	DS1045S–4	4 ns Steps
	16–Pin SOIC	0 to 70	DS1045S–5	5 ns Steps
DS1200	10–Pin DIP	0 to 70	DS1200	
	10–Pin DIP	–40 to +85	DS1200N	
	16–Pin SOIC	0 to 70	DS1200S	
	16–Pin SOIC	–40 to +85	DS1200SN	
DS1201	Electronic Key/Tag	0 to 70	DS1201	
DS1202	8–Pin DIP	0 to 70	DS1202	24 x 8 RAM
	8–Pin DIP	–40 to +85	DS1202N	24 x 8 RAM
	8–Pin SOIC	0 to 70	DS1202S–8	24 x 8 RAM
	16–Pin SOIC	0 to 70	DS1202S	24 x 8 RAM
	16–Pin SOIC	–40 to +85	DS1202SN	24 x 8 RAM
DS1204V	Electronic Key/Tag	0 to +70	DS1204U–G01	Generic Code #1
		0 to +70	DS1204U–G02	Generic Code #2
		0 to +70	DS1204U–G03	Generic Code #3
		0 to +70	DS1204U–G04	Generic Code #4

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
		0 to +70	DS1204U–G05	Generic Code #5
		0 to +70	DS1204U–xxx	xxx = 011 to 999
		0 to +70	DS1204U–G1C	Generic Code #1 w/cap
		0 to +70	DS1204U–G2C	Generic Code #2 w/cap
		0 to +70	DS1204U–G3C	Generic Code #3 w/cap
		0 to +70	DS1204U–G4C	Generic Code #4 w/cap
		0 to +70	DS1204U–G5C	Generic Code #5 w/cap
DS1205S	16–Pin SOIC	0 to +70	DS1205S	
	16–Pin SOIC	–40 to +85	DS1205SN	
DS1205V	Electronic Key/Tag	0 to +70	DS1205U	
DS1206	14–Pin DIP	0 to 70	DS1206	
	14–Pin DIP	–40 to +85	DS1206N	
	16–Pin SOIC	0 to 70	DS1206S	
	16–Pin SOIC	–40 to +85	DS1206SN	
DS1207	Electronic Key/Tag	0 to +70	DS1207–G01	Generic Code #1
		0 to +70	DS1207–G02	Generic Code #2
		0 to +70	DS1207–G03	Generic Code #3
		0 to +70	DS1207–G04	Generic Code #4
		0 to +70	DS1207–G05	Generic Code #5
		0 to +70	DS1207–xxx	xxx = 001 to 999
		0 to +70	DS1207–G1C	Generic Code #1 w/cap
		0 to +70	DS1207–G2C	Generic Code #2 w/cap
		0 to +70	DS1207–G3C	Generic Code #3 w/cap
		0 to +70	DS1207–G4C	Generic Code #4 w/cap
		0 to +70	DS1207–G5C	Generic Code #5 w/cap
DS1210	8–Pin DIP	0 to 70	DS1210	
	8–Pin DIP	–40 to +85	DS1210N	
	16–Pin SOIC	0 to 70	DS1210S	
	16–Pin SOIC	–40 to +85	DS1210SN	
DS1211	20–Pin DIP	0 to 70	DS1211	
	20–Pin DIP	–40 to +85	DS1211N	
	20–Pin SOIC	0 to 70	DS1211S	
	20–Pin SOIC	–40 to +85	DS1211SN	
DS1212	28–Pin DIP	0 to 70	DS1212	
	28–Pin DIP	–40 to +85	DS1212N	
	28–Pin PLCC	0 to 70	DS1212Q	
	28–Pin PLCC	–40 to +85	DS1212QN	
DS1213B	Socket	0 to 70	DS1213B	
DS1213C	Socket	0 to 70	DS1213C	
DS1213D	Socket	0 to 70	DS1213D	
DS1215	16–Pin DIP	0 to 70	DS1215	
	16–Pin DIP	–40 to +85	DS1215N	
	16–Pin SOIC	0 to 70	DS1215S	
DS1216B	28–Pin Socket	0 to 70	DS1216B	16K/64K RAM
DS1216C	28–Pin Socket	0 to 70	DS1216C	64K/256K RAM
DS1216D	32–Pin Socket	0 to 70	DS1216D	256K/1M RAM

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS1216E	28–Pin Socket	0 to 70	DS1216E	64K/256K ROM
DS1216F	32–Pin Socket	0 to 70	DS1216F	64K/256K/1M ROM
DS1217A		0 to +70	DS1217A 16K–25	16K Bit Density
		0 to +70	DS1217A 64K–25	64K Bit Density
		0 to +70	DS1217A 128K–25	128K Bit Density
		0 to +70	DS1217A 192K–25	192K Bit Density
		0 to +70	DS1217A 256K–25	256K Bit Density
DS1217M		0 to +70	DS1217M 512–25	512K Bit Density
		0 to +70	DS1217M 1–15	1 Megabit Density
		0 to +70	DS1217M 2–25	2 Megabit Density
		0 to +70	DS1217M 3–25	3 Megabit Density
		0 to +70	DS1217M 4–25	4 Megabit Density
DS1218	8–Pin DIP	0 to 70	DS1218	
	8–Pin SOIC	0 to 70	DS1218S	
DS1220AB/AD	24–Pin Encap. DIP	0 to +70	DS1220AB–200	200 ns
	24–Pin Encap. DIP	0 to +70	DS1220AB–150	150 ns
	24–Pin Encap. DIP	0 to +70	DS1220AB–120	120 ns
	24–Pin Encap. DIP	0 to +70	DS1220AB–100	100 ns
	24–Pin Encap. DIP	–40 to +85	DS1220AB–200–IND	200 ns
	24–Pin Encap. DIP	–40 to +85	DS1220AB–100–IND	100 ns
	24–Pin Encap. DIP	0 to +70	DS1220AD–200	200 ns
	24–Pin Encap. DIP	0 to +70	DS1220AD–150	150 ns
	24–Pin Encap. DIP	0 to +70	DS1220AD–120	120 ns
	24–Pin Encap. DIP	0 to +70	DS1220AD–100	100 ns
	24–Pin Encap. DIP	–40 to +85	DS1220AD–200–IND	200 ns
	24–Pin Encap. DIP	–40 to +85	DS1220AD–100–IND	100 ns
DS1220Y	24–Pin Encap. DIP	0 to 70	DS1220Y–200	200 ns
	24–Pin Encap. DIP	0 to 70	DS1220Y–150	150 ns
	24–Pin Encap. DIP	0 to 70	DS1220Y–120	120 ns
	24–Pin Encap. DIP	0 to 70	DS1220Y–100	100 ns
	24–Pin Encap. DIP	–40 to +85	DS1220Y–200–IND	200 ns
	24–Pin Encap. DIP	–40 to +85	DS1220Y–100–IND	100 ns
DS1221	16–Pin DIP	0 to 70	DS1221	
	16–Pin DIP	–40 to +85	DS1221N	
	16–Pin SOIC	0 to 70	DS1221S	
	16–Pin SOIC	–40 to +85	DS1221SN	
DS1222	14–Pin DIP	0 to 70	DS1222	
	14–Pin DIP	–40 to +85	DS1222N	
	16–Pin SOIC	0 to 70	DS1222S	
	16–Pin SOIC	–40 to +85	DS1222SN	
DS1225AB/AD	28–Pin Encap. DIP	0 to 70	DS1225AB–200	200 ns
	28–Pin Encap. DIP	0 to 70	DS1225AB–150	150 ns
	28–Pin Encap. DIP	0 to 70	DS1225AB–85	85 ns
	28–Pin Encap. DIP	0 to 70	DS1225AB–70	70 ns
	28–Pin Encap. DIP	–40 to +85	DS1225AB–200–IND	200 ns
	28–Pin Encap. DIP	–40 to +85	DS1225AB–150–IND	150 ns

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	28–Pin Encap. DIP	–40 to +85	DS1225AB–70–IND	70 ns
	28–Pin Encap. DIP	0 to 70	DS1225AD–200	200 ns
	28–Pin Encap. DIP	0 to 70	DS1225AD–150	150 ns
	28–Pin Encap. DIP	0 to 70	DS1225AD–85	85 ns
	28–Pin Encap. DIP	0 to 70	DS1225AD–70	70 ns
	28–Pin Encap. DIP	–40 to +85	DS1225AD–200–IND	200 ns
	28–Pin Encap. DIP	–40 to +85	DS1225AD–150–IND	150 ns
	28–Pin Encap. DIP	–40 to +85	DS1225AD–70–IND	70 ns
DS1225Y	28–Pin Encap. DIP	0 to 70	DS1225Y–200	200 ns
	28–Pin Encap. DIP	0 to 70	DS1225Y–170	170 ns
	28–Pin Encap. DIP	0 to 70	DS1225Y–150	150 ns
	28–Pin Encap. DIP	–40 to +85	DS1225Y–200–IND	200 ns
	28–Pin Encap. DIP	–40 to +85	DS1225Y–150–IND	150 ns
DS1228	16–Pin DIP	0 to 70	DS1228	
	16–Pin SOIC	0 to 70	DS1228S	
DS1229	20–Pin DIP	0 to 70	DS1229	
	20–Pin SOIC	0 to 70	DS1229S	
DS1230Y/AB	28–Pin Encap. DIP	0 to 70	DS1230AB–200	200 ns
	28–Pin Encap. DIP	0 to 70	DS1230AB–150	150 ns
	28–Pin Encap. DIP	0 to 70	DS1230AB–120	120 ns
	28–Pin Encap. DIP	0 to 70	DS1230AB–100	100 ns
	28–Pin Encap. DIP	0 to 70	DS1230AB–85	85 ns
	28–Pin Encap. DIP	0 to 70	DS1230AB–70	70 ns
	28–Pin Encap. DIP	–40 to +85	DS1230AB–200–IND	200 ns
	28–Pin Encap. DIP	–40 to +85	DS1230AB–120–IND	120 ns
	28–Pin Encap. DIP	–40 to +85	DS1230AB–70–IND	70 ns
	28–Pin Encap. DIP	0 to 70	DS1230Y–200	200 ns
	28–Pin Encap. DIP	0 to 70	DS1230Y–150	150 ns
	28–Pin Encap. DIP	0 to 70	DS1230Y–120	120 ns
	28–Pin Encap. DIP	0 to 70	DS1230Y–100	100 ns
	28–Pin Encap. DIP	0 to 70	DS1230Y–85	85 ns
	28–Pin Encap. DIP	0 to 70	DS1230Y–70	70 ns
	28–Pin Encap. DIP	–40 to +85	DS1230Y–200–IND	200 ns
	28–Pin Encap. DIP	–40 to +85	DS1230Y–120–IND	120 ns
	28–Pin Encap. DIP	–40 to +85	DS1230Y–70–IND	70 ns
DS1231	8–Pin DIP	0 to 70	DS1231–20	20
	8–Pin DIP	0 to 70	DS1231–35	35
	8–Pin DIP	0 to 70	DS1231–50	50
	8–Pin DIP	–40 to +85	DS1231N–20	20
	8–Pin DIP	–40 to +85	DS1231N–35	35
	8–Pin DIP	–40 to +85	DS1231N–50	50
	8–Pin GULLWING	0 to 70	DS1231G–20	20
	8–Pin GULLWING	0 to 70	DS1231G–35	35
	8–Pin GULLWING	0 to 70	DS1231G–50	50
	8–Pin GULLWING	–40 to +85	DS1231GN–20	20
	8–Pin GULLWING	–40 to +85	DS1231GN–35	35

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	8–Pin GULLWING	–40 to +85	DS1231GN–50	50
	16–Pin SOIC	0 to 70	DS1231S–20	20
	16–Pin SOIC	0 to 70	DS1231S–35	35
	16–Pin SOIC	0 to 70	DS1231S–50	50
	16–Pin SOIC	–40 to +85	DS1231SN–20	20
	16–Pin SOIC	–40 to +85	DS1231SN–35	35
	16–Pin SOIC	–40 to +85	DS1231SN–50	50
DS1232	8–Pin DIP	0 to 70	DS1232	
	8–Pin DIP	–40 to +85	DS1232N	
	8–Pin GULLWING	0 to 70	DS1232G	
	8–Pin GULLWING	–40 to +85	DS1232GN	
	16–Pin SOIC	0 to 70	DS1232S	
	16–Pin SOIC	–40 to +85	DS1232SN	
DS1232LP	8–Pin DIP	0 to 70	DS1232LP	
	8–Pin DIP	–40 to +85	DS1232LPN	
	8–Pin SOIC	0 to 70	DS1232LPS–2	
	8–Pin SOIC	–40 to _85	DS1232LPSN–2	
	16–Pin SOIC	0 to 70	DS1232LPS	
	16–Pin SOIC	–40 to +85	DS1232LPSN	
DS1233 5V	TO–92	–40 to +85	DS1233–5	5% MONITOR
	TO–92	–40 to +85	DS1233–10	10% MONITOR
	TO–92	–40 to +85	DS1233–15	15% MONITOR
	SOT–223	–40 to +85	DS1233Z–5	5% MONITOR
	SOT–223	–40 to +85	DS1233Z–10	10% MONITOR
	SOT–223	–40 to +85	DS1233Z–15	15% MONITOR
DS1233A 3.3V	TO–92	–40 to +85	DS1233A–10	10% MONITOR
	TO–92	–40 to +85	DS1233A–15	15% MONITOR
	SOT–223	–40 to +85	DS1233AZ–10	10% MONITOR
	SOT–223	–40 to +85	DS1233AZ–15	15% MONITOR
DS1233D 5V	TO–92	–40 to +85	DS1233D–5	5% MONITOR
	TO–92	–40 to +85	DS1233D–10	10% MONITOR
	TO–92	–40 to +85	DS1233D–15	15% MONITOR
	SOT–223	–40 to +85	DS1233DZ–5	5% MONITOR
	SOT–223	–40 to +85	DS1233DZ–10	10% MONITOR
	SOT–223	–40 to +85	DS1233DZ–15	15% MONITOR
DS1234	14–Pin DIP	0 to 70	DS1234	
	16–Pin SOIC	0 to 70	DS1234S	
DS1236	16–Pin DIP	0 to 70	DS1236	10% MONITOR
	16–Pin DIP	0 to 70	DS1236–5	5% MONITOR
	16–Pin DIP	–40 to +85	DS1236N	10% MONITOR
	16–Pin DIP	–40 to +85	DS1236N–5	5% MONITOR
	16–Pin SOIC	0 to 70	DS1236S	10% MONITOR
	16–Pin SOIC	0 to 70	DS1236S–5	5% MONITOR
	16–Pin SOIC	–40 to +85	DS1236SN	10% MONITOR
	16–Pin SOIC	–40 to +85	DS1236SN–5	5% MONITOR

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS1236A	16–Pin DIP	0 to 70	DS1236A	10% MONITOR
	16–Pin DIP	0 to 70	DS1236A–5	5% MONITOR
	16–Pin DIP	–40 to +85	DS1236AN	10% MONITOR
	16–Pin DIP	–40 to +85	DS1236AN–5	5% MONITOR
	16–Pin SOIC	0 to 70	DS1236AS	10% MONITOR
	16–Pin SOIC	0 to 70	DS1236AS–5	5% MONITOR
	16–Pin SOIC	–40 to +85	DS1236ASN	10% MONITOR
	16–Pin SOIC	–40 to +85	DS1236ASN–5	5% MONITOR
DS1237	16–Pin DIP	0 to 70	DS1237–x	x = 1 to 8
	16–Pin SOIC	0 to 70	DS1237S–x	x = 1 to 8
DS1238	16–Pin DIP	0 to 70	DS1238	10% MONITOR
	16–Pin DIP	0 to 70	DS1238–5	5% MONITOR
	16–Pin DIP	–40 to +85	DS1238N	10% MONITOR
	16–Pin SOIC	0 to 70	DS1238S	10% MONITOR
	16–Pin SOIC	0 to 70	DS1238S–5	5% MONITOR
DS1238A	16–Pin DIP	0 to 70	DS1238A	10% MONITOR
	16–Pin DIP	0 to 70	DS1238A–5	5% MONITOR
	16–Pin SOIC	0 to 70	DS1238AS	10% MONITOR
	16–Pin SOIC	0 to 70	DS1238AS–5	5% MONITOR
DS1239	16–Pin DIP	0 to 70	DS1239	10% MONITOR
	16–Pin DIP	0 to 70	DS1239–5	5% MONITOR
	16–Pin DIP	–40 to +85	DS1239N	10% MONITOR
	16–Pin DIP	–40 to +85	DS1239N–5	5% MONITOR
	16–Pin SOIC	0 to 70	DS1239S	10% MONITOR
	16–Pin SOIC	0 to 70	DS1239S–5	5% MONITOR
	16–Pin SOIC	–40 to +85	DS1239SN	10% MONITOR
	16–Pin SOIC	–40 to +85	DS1239SN–5	5% MONITOR
DS1243Y	28–Pin Encap. DIP	0 to 70	DS1243Y	8K x 8 RAM; 200 ns
DS1244Y	28–Pin Encap. DIP	0 to 70	DS1244Y–000	32K x 8 RAM; 200 ns
	28–Pin Encap. DIP	0 to 70	DS1244Y–120	32K x 8 RAM; 120 ns
	28–Pin Encap. DIP	0 to 70	DS1244Y–150	32K x 8 RAM; 150 ns
DS1245Y/AB	32–Pin Encap. DIP	0 to 70	DS1245AB–120	120 ns
	32–Pin Encap. DIP	0 to 70	DS1245AB–100	100 ns
	32–Pin Encap. DIP	0 to 70	DS1245AB–85	85 ns
	32–Pin Encap. DIP	0 to 70	DS1245AB–70	70 ns
	32–Pin Encap. DIP	–40 to +85	DS1245AB–120–IND	120 ns
	32–Pin Encap. DIP	–40 to +85	DS1245AB–70–IND	70 ns
	32–Pin Encap. DIP	0 to 70	DS1245Y–120	120 ns
	32–Pin Encap. DIP	0 to 70	DS1245Y–100	100 ns
	32–Pin Encap. DIP	0 to 70	DS1245Y–85	85 ns
	32–Pin Encap. DIP	0 to 70	DS1245Y–70	70 ns
	32–Pin Encap. DIP	–40 to +85	DS1245Y–120–IND	120 ns
	32–Pin Encap. DIP	–40 to +85	DS1245Y–70–IND	70 ns
DS1248Y	32–Pin Encap. DIP	0 to 70	DS1248Y–000	128K x 8 RAM; 200 ns
	32–Pin Encap. DIP	0 to 70	DS1248Y–120	128K x 8 RAM; 120 ns
	32–Pin Encap. DIP	0 to 70	DS1248y–150	128K x 8 RAM; 150 ns

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS1250		0 to +70	DS1250	
DS1258K	Kit	N/A	DS1258K–001	For CyberCard
	Kit	N/A	DS1258K–002	For CyberKey
DS1259	16–Pin DIP	0 to 70	DS1259	
	16–Pin DIP	–40 to +85	DS1259N	
	16–Pin SOIC	0 to 70	DS1259S	
	16–Pin SOIC	–40 to +85	DS1259SN	
DS1260		0 to 70	DS1260–25	250 mAHr
		0 to 70	DS1260–50	500 mAHr
		0 to 70	DS1260–100	1000 mAHr
DS1267	14–Pin DIP	0 to 70	DS1267–10	10K ohms
	14–Pin DIP	0 to 70	DS1267–50	50K ohms
	14–Pin DIP	0 to 70	DS1267–100	100K ohms
	14–Pin DIP	–40 to +85	DS1267N–10	10K ohms
	14–Pin DIP	–40 to +85	DS1267N–50	50K ohms
	14–Pin DIP	–40 to +85	DS1267N–100	100K ohms
	14–Pin SOIC	0 to 70	DS1267S–10	10K ohms
	14–Pin SOIC	0 to 70	DS1267S–50	50K ohms
	14–Pin SOIC	0 to 70	DS1267S–100	100K ohms
	14–Pin SOIC	–40 to +85	DS1267SN–10	10K ohms
	14–Pin SOIC	–40 to +85	DS1267SN–50	50K ohms
	14–Pin SOIC	–40 to +85	DS1267SN–100	100K ohms
	20–Pin TSSOP	0 to 70	DS1267E–10	10K ohms
	20–Pin TSSOP	0 to 70	DS1267E–50	50K ohms
	20–Pin TSSOP	0 to 70	DS1267E–100	100K ohms
DS1275	8–Pin DIP	0 to 70	DS1275	
	8–Pin SOIC	0 to 70	DS1275S	
DS1280	44–Pin Flat Pack	0 to 70	DS1280FP–44	
	80–Pin Flat Pack	0 to 70	DS1280FP–80	
DS1283	28–Pin DIP	0 to 70	DS1283	50 X 8 RAM
	28–Pin DIP	–40 to +85	DS1283N	50 x 8 RAM
	28–Pin SOIC	0 to 70	DS1283S	50 X 8 RAM
	28–Pin SOIC	–40 to +85	DS1283SN	50 x 8 RAM
DS1284	28–Pin DIP	0 to 70	DS1284	50 X 8 RAM
	28–Pin PLCC	0 to 70	DS1284Q	50 X 8 RAM
	28–Pin PLCC	–40 to +85	DS1284QN	50 X 8 RAM
DS1285	24–Pin DIP	0 to 70	DS1285	50 X 8 RAM
	24–Pin DIP	–40 to +85	DS1285N	50 x 8 RAM
	28–Pin PLCC	0 to 70	DS1285Q	50 X 8 RAM
	28–Pin PLCC	–40 to +85	DS1285QN	50 X 8 RAM
DS1286	28–Pin Encap. DIP	0 to 70	DS1286	50 X 8 RAM
DS1287	24–Pin Encap. DIP	0 to 70	DS1287	50 X 8 RAM
DS1287A	24–Pin Encap. DIP	0 to 70	DS1287A	50 X 8 RAM
DS129X	16–Pin Encap. DIP	0 to 70	DS1290	
	16–Pin DIP	0 to 70	DS1291	
	16–Pin DIP	–40 to +85	DS1291N	

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	24–Pin Encap. DIP	0 to 70	DS1292	
	24–Pin DIP	0 to 70	DS1293	
	24–Pin DIP	–40 to +85	DS1293N	
DS1302	8–Pin DIP	0 to 70	DS1302	31 x 8 RAM
	8–Pin DIP	–40 to +85	DS1302N	31 x 8 RAM
	8–Pin SOIC	0 to 70	DS1302S	31 x 8 RAM
	8–Pin SOIC	–40 to +85	DS1302SN	31 x 8 RAM
	8–Pin SOIC (150 mils)	0 to 70	DS1302Z	31 x 8 RAM
	8–Pin SOIC (150 mils)	–40 to +85	DS1302ZN	31 x 8 RAM
DS1330Y/AB	34–Pin LPM	0 to 70	DS1330ABLPM–100	100 ns
	34–Pin LPM	0 to 70	DS1330ABLPM–70	70 ns
	34–Pin LPM	0 to 70	DS1330YLPM–100	100 ns
	34–Pin LPM	0 to 70	DS1330YLPM–70	70 ns
DS1336	16–Pin DIP	0 to 70	DS1336	
	16–Pin DIP	–40 to +85	DS1336N	
	16–Pin SOIC	0 to 70	DS1336S	
	16–Pin SOIC	–40 to +85	DS1336SN	
DS1345Y/AB	34–Pin LPM	0 to 70	DS1345ABLPM–100	100 ns
	34–Pin LPM	0 to 70	DS1345ABLPM–70	70 ns
	34–Pin LPM	0 to 70	DS1345YLPM–100	100 ns
	34–Pin LPM	0 to 70	DS1345YLPM–70	70 ns
DS1350Y/AB	34–Pin LPM	0 to 70	DS1350ABLPM–100	100 ns
	34–Pin LPM	0 to 70	DS1350ABLPM–70	70 ns
	34–Pin LPM	0 to 70	DS1350YLPM–100	100 ns
	34–Pin LPM	0 to 70	DS1350YLPM–70	70 ns
DS1380	24–Pin DIP	0 to 70	DS1380	
	24–Pin SOIC	0 to 70	DS1380S	
DS1381	24–Pin Encap. DIP	0 to 70	DS1381	
DS1385	24–Pin DIP	0 to 70	DS1385	4K x 8 RAM
	28–Pin SOIC	0 to 70	DS1385S	4K x 8 RAM
DS1386	32–Pin Encap. DIP	0 to 70	DS1386–8–120	8K x 8 RAM; 120 ns
	32–Pin Encap. DIP	0 to 70	DS1386–8–150	8K x 8 RAM; 150 ns
	32–Pin Encap. DIP	0 to 70	DS1386–32–120	32K x 8 RAM; 120 ns
	32–Pin Encap. DIP	0 to 70	DS1386–32–150	32K x 8 RAM; 150 ns
DS1387	24–Pin Encap. DIP	0 to 70	DS1387	4K x 8 RAM
DS1395	28–Pin DIP	0 to 70	DS1395	4K x 8 RAM
	28–Pin SOIC	0 to 70	DS1395S	4K x 8 RAM
DS1397	28–Pin Encap. DIP	0 to 70	DS1397	4K x 8 RAM
DS1401			DS1401–xx	xx = 04 to 24, Nr. of Button ports
DS1402			DS1402RP4	RJ–11/Probe, 1.2m (4 feet)
			DS1402BB4	Two Buttons, 1.2m (4 feet)
			DS1402BP4	Button/Probe, 1.2m (4 feet)

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
			DS1402BR4	Button/RJ–11, 1.2m (4 feet)
DS1410	Button Holder/Parallel	0 to 70	DS1410	
DS1412	Button Holder/Serial	0 to 70	DS1412	
DS1414	Button Holder/Network	0 to 70	DS1414	
DS1420	F50	–40 to +85	DS1420L–F50	
DS1422	D50	–40 to +85	DS14220–F50	
DS1425	F50	–40 to +70	DS1425L–F50	
DS1427	F50	–40 to +70	DS1427L–F50	
DS1485	24–Pin DIP	0 to 70	DS1485	8K x 8 RAM
	28–Pin SOIC	0 to 70	DS1485S	8K x 8 RAM
DS1486	32–Pin Encap. DIP	0 to 70	DS1486–120	128K x 8 RAM; 120 ns
	32–Pin Encap. DIP	0 to 70	DS1486–150	128K x 8 RAM; 150 ns
DS1488	24–Pin Encap. DIP	0 to 70	DS1488	8K x 8 RAM
DS1494	Touch Memory	–40 to +70	DS1494L–F5	F5 MicroCan
DS1495	28–Pin DIP	0 to 70	DS1495	8K x 8 RAM
	28–Pin SOIC	0 to 70	DS1495S	8K x 8 RAM
DS1497	28–Pin Encap. DIP	0 to 70	DS1497	8K x 8 RAM
DS1585	28–Pin DIP	0 to 70	DS1585	8K x 8 RAM
	28–Pin SOIC	0 to 70	DS1585S	8K x 8 RAM
DS1587	28–Pin Encap. DIP	0 to 70	DS1587	8K x 8 RAM
	34–Pin Encap. LPM	0 to 70	DS1587L	8K x 8 RAM
DS1589	28–Pin DIP	0 to 70	DS1589	8K x 8 RAM
	28–Pin SOIC	0 to 70	DS1589S	8K x 8 RAM
DS1593	28–Pin Encap. DIP	0 to 70	DS1593	8K x 8 RAM
DS1602	8–Pin DIP	0 to 70	DS1602	
	8–Pin SOIC	0 to 70	DS1602S	
DS1603	7–Pin Encap. SIP	0 to 70	DS1603	
DS1609	24–Pin DIP	–40 to +85	DS1609	
	24–Pin SOIC	–40 to +85	DS1609S	
DS1610	16–Pin DIP	0 to 70	DS1610	
	16–Pin DIP	–40 to +85	DS1610N	
	16–Pin SOIC	0 to 70	DS1610S	
	16–Pin SOIC	–40 to +85	DS1610SN	
DS1611	16–Pin DIP	0 to 70	DS1611	
	16–Pin DIP	–40 to +85	DS1611N	
	16–Pin SOIC	0 to 70	DS1611S	
	16–Pin SOIC	–40 to +85	DS1611SN	
	20–Pin TSSOP	0 to 70	DS1611E	
	20–Pin TSSOP	–40 to +85	DS1611EN	
DS1612	16–Pin DIP	0 to 70	DS1612	
	16–Pin DIP	–40 to +85	DS1612N	
	16–Pin SOIC	0 to 70	DS1612S	
	16–Pin SOIC	–40 to +85	DS1612SN	
	20–Pin TSSOP	0 to 70	DS1612E	
	20–Pin TSSOP	–40 to +85	DS1612EN	

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS1613C	Socket	0 to 70	DS1613C	
DS1613D	Socket	0 to 70	DS1613D	
DS1620	8–Pin DIP	–55 to +125	DS1620	
	8–Pin SOIC	–55 to +125	DS1620S	
DS1630Y/AB	28–Pin Encap. DIP	0 to 70	DS1630AB–120	120 ns
	28–Pin Encap. DIP	0 to 70	DS1630AB–100	100 ns
	28–Pin Encap. DIP	0 to 70	DS1630AB–85	85 ns
	28–Pin Encap. DIP	0 to 70	DS1630AB–70	70 ns
	28–Pin Encap. DIP	–40 to +85	DS1630AB–70–IND	70 ns
	34–Pin LPM	0 to 70	DS1630ABLPM–100	100 ns
	34–Pin LPM	0 to 70	DS1630ABLPM–70	70 ns
	34–Pin LPM	–40 to +85	DS1630ABLPM–70–IND	70 ns
	28–Pin Encap. DIP	0 to 70	DS1630Y–120	120 ns
	28–Pin Encap. DIP	0 to 70	DS1630Y–100	100 ns
	28–Pin Encap. DIP	0 to 70	DS1630Y–85	85 ns
	28–Pin Encap. DIP	0 to 70	DS1630Y–70	70 ns
	28–Pin Encap. DIP	–40 to +85	DS1630Y–70–IND	70 ns
	34–Pin LPM	0 to 70	DS1630YLPM–100	100 ns
	34–Pin LPM	0 to 70	DS1630YLPM–70	70 ns
	34–Pin LPM	–40 to +85	DS1630YLPM–70–IND	70 ns
DS1632	16–Pin DIP	0 to 70	DS1632	
	16–Pin DIP	–40 to +85	DS1632N	
	16–Pin SOIC	0 to 70	DS1632S	
	16–Pin SOIC	–40 to +85	DS1632SN	
DS1633	3–Pin TO–220	–40 to +85	DS1633XX	See data sheet for complete specifications.
DS1640	16–Pin DIP	0 to 70	DS1640	
	16–Pin DIP	–40 to +85	DS1640N	
	16–Pin SOIC	0 to 70	DS1640S	
	16–Pin SOIC	–40 to +85	DS1640SN	
	16–Pin DIP	0 to 70	DS1640C	Consumer Grade
	16–Pin SOIC	0 to 70	DS1640SC	Consumer Grade
DS1642	24–Pin Encap. DIP	0 to 70	DS1642–120	2K x 8 RAM; 120 ns
	24–Pin Encap. DIP	0 to 70	DS1642–150	2K x 8 RAM; 150 ns
DS1643	28–Pin Encap. DIP	0 to 70	DS1643–120	8K x 8 RAM; 120 ns
	28–Pin Encap. DIP	0 to 70	DS1643–150	8K x 8 RAM; 150 ns
	26–Pin Encap. LPM	0 to 70	DS1643L–120	8K x 8 RAM; 120 ns
	26–Pin Encap. LPM	0 to 70	DS1643L–150	8K x 8 RAM; 150 ns
DS1644	28–Pin Encap. DIP	0 to 70	DS1644–120	32K x 8 RAM; 120 ns
	28–Pin Encap. DIP	0 to 70	DS1644–150	32K x 8 RAM; 150 ns
	34–Pin Encap. LPM	0 to 70	DS1644L–120	32K x 8 RAM; 120 ns
	34–Pin Encap. LPM	0 to 70	DS1644L–150	32K x 8 RAM; 150 ns
DS1645Y/AB	32–Pin Encap. DIP	0 to 70	DS1645AB–120	120 ns
	32–Pin Encap. DIP	0 to 70	DS1645AB–100	100 ns
	32–Pin Encap. DIP	0 to 70	DS1645AB–85	85 ns
	32–Pin Encap. DIP	0 to 70	DS1645AB–70	70 ns

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	32–Pin Encap. DIP	–40 to +85	DS1645AB–70–IND	70 ns
	34–Pin LPM	0 to 70	DS1645ABLPM–100	100 ns
	34–Pin LPM	0 to 70	DS1645ABLPM–70	70 ns
	34–Pin LPM	–40 to +85	DS1645ABLPM–70–IND	70 ns
	32–Pin Encap. DIP	0 to 70	DS1645Y–120	120 ns
	32–Pin Encap. DIP	0 to 70	DS1645Y–100	100 ns
	32–Pin Encap. DIP	0 to 70	DS1645Y–85	85 ns
	32–Pin Encap. DIP	0 to 70	DS1645Y–70	70 ns
	32–Pin Encap. DIP	–40 to +85	DS1645Y–70–IND	70 ns
	34–Pin LPM	0 to 70	DS1645YLPM–100	100 ns
	34–Pin LPM	0 to 70	DS1645YLPM–70	70 ns
	34–Pin LPM	–40 to +85	DS1645YLPM–70–IND	70 ns
DS1645EE	32–Pin Encap. DIP	0 to 70	DS1645EE–100	100 ns
	32–Pin Encap. DIP	0 to 70	DS1645EE–85	85 ns
	32–Pin Encap. DIP	0 to 70	DS1645EE–70	70 ns
	32–Pin Encap. DIP	–40 to +85	DS1645EE–70–IND	70 ns
DS1646	32–Pin Encap. DIP	0 to 70	DS1646–120	128K x 8 RAM; 120 ns
	32–Pin Encap. DIP	0 to 70	DS1646–150	128K x 8 RAM; 150 ns
	34–Pin Encap. LPM	0 to 70	DS1646L–120	128K x 8 RAM; 120 ns
	34–Pin Encap. LPM	0 to 70	DS1646L–150	128K x 8 RAM; 150 ns
DS1650Y/AB	32–Pin Encap. DIP	0 to 70	DS1650AB–100	100 ns
	32–Pin Encap. DIP	0 to 70	DS1650AB–85	85 ns
	32–Pin Encap. DIP	0 to 70	DS1650AB–70	70 ns
	32–Pin Encap. DIP	–40 to +85	DS1650AB–70–IND	70 ns
	34–Pin LPM	0 to 70	DS1650ABLPM–100	100 ns
	34–Pin LPM	0 to 70	DS1650ABLPM–70	70 ns
	34–Pin LPM	–40 to +85	DS1650ABLPM–70–IND	70 ns
	32–Pin Encap. DIP	0 to 70	DS1650Y–100	100 ns
	32–Pin Encap. DIP	0 to 70	DS1650Y–85	85 ns
	32–Pin Encap. DIP	0 to 70	DS1650Y–70	70 ns
	32–Pin Encap. DIP	–40 to +85	DS1650Y–70–IND	70 ns
	34–Pin LPM	0 to 70	DS1650YLPM–100	100 ns
	34–Pin LPM	0 to 70	DS1650YLPM–70	70 ns
	34–Pin LPM	–40 to +85	DS1650YLPM–70–IND	70 ns
DS1651	8–Pin DIP	–25 to +85	DS1651	
	8–Pin SOIC	–25 to +85	DS1651S	
DS1652	8–Pin DIP	–25 to +85	DS1652	
	8–Pin SOIC	–25 to +85	DS1652S	
DS1653	16–Pin DIP	–25 to +85	DS1653	
	16–Pin SOIC	–25 to +85	DS1653S	
DS1658Y/AB	40–Pin Encap. DIP	0 to 70	DS1658AB–100	100 ns
	40–Pin Encap. DIP	0 to 70	DS1658AB–70	70 ns
	40–Pin Encap. DIP	–40 to +85	DS1658AB–70–IND	70 ns
	40–Pin Encap. DIP	0 to 70	DS1658Y–100	100 ns
	40–Pin Encap. DIP	0 to 70	DS1658Y–70	70 ns
	40–Pin Encap. DIP	–40 to +85	DS1658Y–70–IND	70 ns

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS1666	14–Pin DIP	0 to 70	DS1666–10	10K ohms
	14–Pin DIP	0 to 70	DS1666–50	50K ohms
	14–Pin DIP	0 to 70	DS1666–100	100K ohms
	14–Pin DIP	–40 to +85	DS1666N–10	10K ohms
	14–Pin DIP	–40 to +85	DS1666N–50	50K ohms
	14–Pin DIP	–40 to +85	DS1666N–100	100K ohms
	16–Pin SOIC	0 to 70	DS1666S–10	10K ohms
	16–Pin SOIC	0 to 70	DS1666S–50	50K ohms
	16–Pin SOIC	0 to 70	DS1666S–100	100K ohms
	16–Pin SOIC	–40 to +85	DS1666SN–10	10K ohms
	16–Pin SOIC	–40 to +85	DS1666SN–50	50K ohms
	16–Pin SOIC	–40 to +85	DS1666SN–100	100K ohms
DS1667	20–Pin DIP	0 to 70	DS1667–10	10K ohms
	20–Pin DIP	0 to 70	DS1667–50	50K ohms
	20–Pin DIP	0 to 70	DS1667–100	100K ohms
	20–Pin DIP	–40 to +85	DS1667N–10	10K ohms
	20–Pin DIP	–40 to +85	DS1667N–50	50K ohms
	20–Pin DIP	–40 to +85	DS1667N–100	100K ohms
	20–Pin SOIC	0 to 70	DS1667S–10	10K ohms
	20–Pin SOIC	0 to 70	DS1667S–50	50K ohms
	20–Pin SOIC	0 to 70	DS1667S–100	100K ohms
	20–Pin SOIC	–40 to +85	DS1667SN–10	10K ohms
	20–Pin SOIC	–40 to +85	DS1667SN–50	50K ohms
	20–Pin SOIC	–40 to +85	DS1667SN–100	100K ohms
DS1668	6–Pin Pushbutton	0 to 70	DS1668–10	10K ohms
	6–Pin Pushbutton	0 to 70	DS1668–50	50K ohms
	6–Pin Pushbutton	0 to 70	DS1668–100	100K ohms
DS1669	8–Pin DIP	0 to 70	DS1669–10	10K ohms
	8–Pin DIP	0 to 70	DS1669–50	50K ohms
	8–Pin DIP	0 to 70	DS1669–100	100K ohms
	8–Pin DIP	–40 to +85	DS1669N–10	10K ohms
	8–Pin DIP	–40 to +85	DS1669N–50	50K ohms
	8–Pin DIP	–40 to +85	DS1669N–100	100K ohms
	8–Pin SOIC	0 to 70	DS1669S–10	10K ohms
	8–Pin SOIC	0 to 70	DS1669S–50	50K ohms
	8–Pin SOIC	0 to 70	DS1669S–100	100K ohms
	8–Pin SOIC	–40 to +85	DS1669SN–10	10K ohms
	8–Pin SOIC	–40 to +85	DS1669SN–50	50K ohms
	8–Pin SOIC	–40 to +85	DS1669SN–100	100K ohms
DS1689	28–Pin DIP	0 to 70	DS1689	114 x 8 RAM
	28–Pin SOIC	0 to 70	DS1689S	114 x 8 RAM
DS1693	28–Pin Encap. DIP	0 to 70	DS1693	114 x 8 RAM
DS1710	16–Pin DIP	0 to 70	DS1710	
	16–Pin DIP	–40 to +85	DS1710N	
	16–Pin SOIC	0 to 70	DS1710S	
	16–Pin SOIC	–40 to +85	DS1710SN	

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	20–Pin TSSOP	0 to 70	DS1710E	
	20–Pin TSSOP	–40 to +85	DS1710EN	
DS1730Y	32–Pin Encap. DIP	0 to 70	DS1730Y–200	200 ns
	32–Pin Encap. DIP	0 to 70	DS1730Y–150	150 ns
	32–Pin Encap. DIP	–40 to +85	DS1730Y–150–IND	150 ns
	34–Pin LPM	0 to 70	DS1730YLPM–200	200 ns
	34–Pin LPM	0 to 70	DS1730YLPM–150	150 ns
	34–Pin LPM	–40 to +85	DS1730YLPM–150–IND	150 ns
DS1745Y	32–Pin Encap. DIP	0 to 70	DS1745Y–200	200 ns
	32–Pin Encap. DIP	0 to 70	DS1745Y–150	150 ns
	32–Pin Encap. DIP	–40 to +85	DS1745Y–150–IND	150 ns
	34–Pin LPM	0 to 70	DS1745YLPM–200	200 ns
	34–Pin LPM	0 to 70	DS1745YLPM–150	150 ns
	34–Pin LPM	–40 to +85	DS1745YLPM–150–IND	150 ns
DS1750Y	32–Pin Encap. DIP	0 to 70	DS1750Y–200	200 ns
	32–Pin Encap. DIP	0 to 70	DS1750Y–150	150 ns
	32–Pin Encap. DIP	–40 to +85	DS1750Y–150–IND	150 ns
	34–Pin LPM	0 to 70	DS1750YLPM–200	200 ns
	34–Pin LPM	0 to 70	DS1750YLPM–150	150 ns
	34–Pin LPM	–40 to +85	DS1750YLPM–150–IND	150 ns
DS1758Y/AB	40–Pin Encap. DIP	0 to 70	DS1758Y–200	200 ns
	40–Pin Encap. DIP	0 to 70	DS1758Y–150	150 ns
	40–Pin Encap. DIP	–40 to +85	DS1758Y–150–IND	150 ns
DS1802	20–Pin DIP	0 to 70	DS1802	50K ohms
	20–Pin SOIC	0 to 70	DS1802S	50K ohms
	20–Pin TSSOP	0 to 70	DS1802E	50K ohms
DS1820	PR–35	–55 to +125	DS1820	
	8–Pin SOIC	–55 to +125	DS1820S	
DS1821	PR–35	–55 to +125	DS1821	
	8–Pin SOIC	–55 to +125	DS1821S	
	TO–220	–55 to +125	DS1821T	
DS1833	TO–92	–40 to +85	DS1833–5	5% MONITOR
	TO–92	–40 to +85	DS1833–10	10% MONITOR
	TO–92	–40 to +85	DS1833–15	15% MONITOR
	SOT–223	–40 to +85	DS1833Z–5	5% MONITOR
	SOT–223	–40 to +85	DS1833Z–10	10% MONITOR
	SOT–223	–40 to +85	DS1833Z–15	15% MONITOR
DS1837	TO–220	0 to 70	DS1837	
	D–PAK	0 to 70	DS1837S	
DS1867	14–Pin DIP	0 to 70	DS1867–10	10K ohms
	14–Pin DIP	0 to 70	DS1867–50	50K ohms
	14–Pin DIP	0 to 70	DS1867–100	100K ohms
	16–Pin SOIC	0 to 70	DS1867S–10	10K ohms
	16–Pin SOIC	0 to 70	DS1867S–50	50K ohms
	16–Pin SOIC	0 to 70	DS1867S–100	100K ohms

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	20–Pin TSSOP	0 to 70	DS1867E–10	10K ohms
	20–Pin TSSOP	0 to 70	DS1867E–50	50K ohms
	20–Pin TSSOP	0 to 70	DS1867E–100	100K ohms
DS1868	14–Pin DIP	0 to 70	DS1868–10	10K ohms
	14–Pin DIP	0 to 70	DS1868–50	50K ohms
	14–Pin DIP	0 to 70	DS1868–100	100K ohms
	16–Pin DIP	0 to 70	DS1868S–10	10K ohms
	16–Pin DIP	0 to 70	DS1868S–50	50K ohms
	16–Pin DIP	0 to 70	DS1868S–100	100K ohms
	20–Pin TSSOP	0 to 70	DS1868E–10	10K ohms
	20–Pin TSSOP	0 to 70	DS1868E–50	50K ohms
	20–Pin TSSOP	0 to 70	DS1868E–100	100K ohms
DS1869	8–Pin DIP	0 to 70	DS1869–10	10K ohms
	8–Pin DIP	0 to 70	DS1869–50	50K ohms
	8–Pin DIP	0 to 70	DS1869–100	100K ohms
	8–Pin SOIC	0 to 70	DS1869S–10	10K ohms
	8–Pin SOIC	0 to 70	DS1869S–50	50K ohms
	8–Pin SOIC	0 to 70	DS1869S–100	100K ohms
DS12885	24–Pin DIP	0 to 70	DS12885	114 X 8 RAM
	24–Pin SOIC	0 to 70	DS12885S	114 x 8 RAM
	28–Pin PLCC	0 to 70	DS12885Q	114 X 8 RAM
	28–Pin PLCC	–40 to +85	DS12885QN	114 x 8 RAM
	32–Pin TQFP	0 to 70	DS12885T	114 x 8 RAM
DS12887	24–Pin Encap. DIP	0 to 70	DS12887	114 X 8 RAM
DS12887A	24–Pin Encap. DIP	0 to 70	DS12887A	114 X 8 RAM
DS1920	Touch Memory	–55 to +100	DS1920–F3	F3 MicroCan
	Touch Memory	–55 to +100	DS1920–F5	F5 MicroCan
DS1982	Touch Memory	–40 to +85	DS1982–F3	F3 MicroCan
	Touch Memory	–40 to +85	DS1982–F5	F5 MicroCan
DS1985	Touch Memory	–40 to +85	DS1985–F3	F3 MicroCan
	Touch Memory	–40 to +85	DS1985–F5	F5 MicroCan
DS1986	Touch Memory	–40 to +85	DS1986–F3	F3 MicroCan
	Touch Memory	–40 to +85	DS1986–F5	F5 MicroCan
DS1990A	Touch Memory	–40 to +85	DS1990A–F3	F3 MicroCan
	Touch Memory	–40 to +85	DS1990A–F5	F5 MicroCan
DS1991	Touch Memory	–40 to +70	DS1991L–F5	F5 MicroCan
DS1992	Touch Memory	–40 to +70	DS1992L–F5	F5 MicroCan
DS1993	Touch Memory	–40 to +70	DS1993L–F5	F5 MicroCan
DS1994	Touch Memory	–40 to +70	DS1994L–F5	F5 MicroCan
DS1995	Touch Memory	–40 to +70	DS1995L–F5	F5 MicroCan
DS1996	Touch Memory	–40 to +70	DS1996L–F5	F5 MicroCan
DS2009	28–Pin DIP (600 MIL)	0 to 70	DS2009–35	35 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2009–50	50 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2009–65	65 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2009–80	80 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2009–120	120 ns

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	28–Pin DIP (600 MIL)	–40 to +85	DS2009N–35	35 ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2009N–50	50 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2009D–35	35 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2009D–50	50 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2009D–65	65 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2009D–80	80 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2009D–120	120 ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2009DN–35	35 ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2009DN–50	50 ns
	32–Pin PLCC	0 to 70	DS2009R–35	35 ns
	32–Pin PLCC	0 to 70	DS2009R–50	50 ns
	32–Pin PLCC	0 to 70	DS2009R–65	65 ns
	32–Pin PLCC	0 to 70	DS2009R–80	80 ns
	32–Pin PLCC	0 to 70	DS2009R–120	120 ns
	32–Pin PLCC	–40 to +85	DS2009RN–35	35 ns
	32–Pin PLCC	–40 to +85	DS2009RN–50	50 ns
DS2010	28–Pin DIP (600 MIL)	0 to 70	DS2010–50	50 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2010–65	65 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2010–80	80 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2010–120	120 ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2010N–50	50 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2010D–50	50 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2010D–65	65 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2010D–80	80 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2010D–120	120 ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2010DN–50	50 ns
	32–Pin PLCC	0 to 70	DS2010R–50	50 ns
	32–Pin PLCC	0 to 70	DS2010R–65	65 ns
	32–Pin PLCC	0 to 70	DS2010R–80	80 ns
	32–Pin PLCC	0 to 70	DS2010R–120	120 ns
	32–Pin PLCC	–40 to +85	DS2010RN–50	50 ns
DS2011	28–Pin DIP (600 MIL)	0 to 70	DS2011–50	50 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2011–65	65 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2011–80	80 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2011–120	120 ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2011N–50	50 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2011D–50	50 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2011D–65	65 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2011D–80	80 ns
	28–Pin DIP (300 MIL)	0 to 70	DS2011D–120	120 ns
	28–Pin DIP (300 MIL)	–40 to +85	DS2011DN–50	50 ns
	32–Pin PLCC	0 to 70	DS2011R–50	50 ns
	32–Pin PLCC	0 to 70	DS2011R–65	65 ns
	32–Pin PLCC	0 to 70	DS2011R–80	80 ns
	32–Pin PLCC	0 to 70	DS2011R–120	120 ns
	32–Pin PLCC	–40 to +85	DS2011RN–50	50 ns

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
DS2012	28–Pin DIP (600 MIL)	0 to 70	DS2012–50	50 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2012–65	65 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2012–80	80 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2012–120	120 ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2012N–50	50 ns
	32–Pin PLCC	0 to 70	DS2012R–50	50 ns
	32–Pin PLCC	0 to 70	DS2012R–65	65 ns
	32–Pin PLCC	0 to 70	DS2012R–80	80 ns
	32–Pin PLCC	0 to 70	DS2012R–120	120 ns
	32–Pin PLCC	–40 to +85	DS2012RN–50	50 ns
DS2013	28–Pin DIP (600 MIL)	0 to 70	DS2013–50	50 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2013–65	65 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2013–80	80 ns
	28–Pin DIP (600 MIL)	0 to 70	DS2013–120	120 ns
	28–Pin DIP (600 MIL)	–40 to +85	DS2013N–50	50 ns
	32–Pin DIP (300 MIL)	0 to 70	DS2013D–50	50 ns
	32–Pin DIP (300 MIL)	0 to 70	DS2013D–65	65 ns
	32–Pin DIP (300 MIL)	0 to 70	DS2013D–80	80 ns
	32–Pin DIP (300 MIL)	0 to 70	DS2013D–120	120 ns
	32–Pin DIP (300 MIL)	–40 to +85	DS2013DN–50	50 ns
DS2016	24–Pin DIP	–40 to +85	DS2016	
	24–Pin SOIC	–40 to +85	DS2016S	
DS2064	28–Pin DIP	–40 to +85	DS2064	
	28–Pin SOIC	–40 to +85	DS2064S	
DS2223	TO–92	–40 to +85	DS2223	
	SOT–223	–40 to +85	DS2223Z	
DS2224	TO–92	–40 to +85	DS2224	
	SOT–223	–40 to +85	DS2224Z	
DS2227	STIK	0 to 70	DS2227–120	120 ns
	STIK	0 to 70	DS2227–100	100 ns
	STIK	0 to 70	DS2227–70	70 ns
DS2229	STIK	0 to 70	DS2229–85	85 ns
DS22B57	28–Pin DIP	–40 to +85	DS22B57	
	28–Pin SOIC	–40 to +85	DS22B57S	
DS2401	TO–92	–40 to +85	DS2401	
	SOT–223	–40 to +85	DS2401Z	
	6–Lead TSOC	–40 to +85	DS2401P	
DS2404	16–Pin DIP	0 to 70	DS2404	512 x 8 RAM
	16–Pin SOIC	0 to 70	DS2404S	512 x 8 RAM
	16–Pin SSOP	0 to 70	DS2404B	512 x 8 RAM
DS2404S–C01	16–Pin SOIC	–40 to +85	DS2404S–C01	Custom 001/Dual Port
DS2405	TO–92	–40 to +85	DS2405	
	SOT–223	–40 to +85	DS2405Z	
	6–Lead TSOC	–40 to +85	DS2405P	
DS2430	TO–92	0 to 70	DS2430	
	TO–92	–40 to +85	DS2430N	

ORDERING INFORMATION

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
	8–Pin SOIC	0 to 70	DS2430Z	
	8–Pin SOIC	–40 to +85	DS2430ZN	
	20–Pin TSSOP	0 to 70	DS2430E	
	20–Pin TSSOP	–40 to +85	DS2430EN	
DS2434	PR–35	–40 to +85	DS2434	
DS2435	PR–35	–40 to +85	DS2435	
DS2502	TO–92	–40 to +85	DS2502	
	8–Pin SOIC	–40 to +85	DS2502S	
	6–Lead TSOC	–40 to +85	DS2502P	
DS2505	TO–92	–40 to +85	DS2505	
	6–Lead TSOC	–40 to +85	DS2505P	
DS2506	PR–35	–40 to +85	DS2506	
DS620X		0 to 70	DS6200	
		0 to 70	DS6201	
		0 to 70	DS6204U	Generic Code #1
		0 to 70	DS6207	Generic Code #1
DS6417		0 to 70	DS6417–001	1 Megabit Density
		0 to 70	DS6417–002	2 Megabit Density
		0 to 70	DS6417–004	4 Megabit Density
		0 to 70	DS6417–256	256K–bit Density
		0 to 70	DS6417–512	512K–bit Density2
		0 to 70	DS6417P–001	1 Megabit Density
		0 to 70	DS6417P–002	2 Megabit Density
		0 to 70	DS6417P–004	4 Megabit Density
		0 to 70	DS6417P–256	256K–bit Density
		0 to 70	DS6417P–512	512K–bit Density
DS9000			DS9000	
DS9002			DS9002	
DS9003			DS9003	
DS9005			DS9005	
DS9006			DS9006	
DS908x			DS9080V	Cyber Key Flushmount–Vertical
			DS9080A	Cyber Key Flushmount–Angled
			DS9081V	Cyber Key Recessed–Vertical
			DS9081A	Cyber Key Recessed–Angled
			DS9082V	Cyber Card Flushmount–Vertical
			DS9082A	Cyber Card Flushmount–Angled
			DS9084V	Cyber Card EV Recessed–Vertical, Beige

DEVICE	PACKAGE TYPE	OPERATING TEMP. RANGE (CELSIUS)	ORDERING NUMBER	SPEED OR VERSION
			DS9084V–001	Cyber Card EV Recessed–Vertical, Black
			DS9084A	Cyber Card EV Recessed–Angled, Beige
			DS9084A–001	Cyber Card EV Recessed–Angled, Black
			DS9085A–001	Cyber Card, Cyber Key
			DS9085V–001	Cyber Card, Cyber Key
DS9092			DS9092	Panel–mount Probe
			DS9092T	Panel–mount Probe with Tactile Pin
			DS9092GT	Hand–Grip with Tactile Pin
DS9092K	Kit		DS9092K	
DS9092R	tabbed MicroCan		DS9092R–000	Standard
	tabbed MicroCan		DS9092R–L00	with Logo
DS9093			DS9093F	Snap–in Fob
			DS9093P	Perm. Mount, One Screw
			DS9093S	Perm. Mount, Two Screws
			DS9093RA	Lock Ring
			DS9093RB	Flange Enlargement
DS9094			DS9094F	Thru–Hole Mount, F5
			DS9094FS	Surface Mount, F5
DS9096P			DS9096P	Permanent Bond
DS9097			DS9097	Standard
			DS9097E	Enhanced for EPROM
DS9098			DS9098	Retainer for F5 MicroCan
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			DS9100B	Touch & Hold, Center Part
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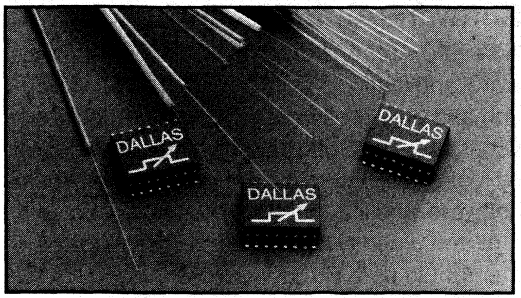


Silicon Timed Circuits

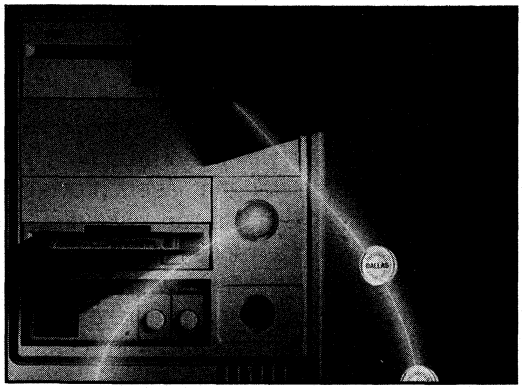
Silicon Timed Circuits (often referred to as delay lines) are chips that make subtle adjustments to the timing of high-performance electronics so that they will perform optimally. Because of the precision that lasers provide, some Silicon Timed Circuits can make timing adjustments down to a fraction of a nanosecond, which is the time it takes light to travel about a foot. For more information, call our Timing Problem Hotline at (214) 450-5348.

Timekeeping

A self-contained lithium energy source in conjunction with a silicon chip and quartz form a permanently powered clock/calendar within a single component. Various computer interfaces are available including phantom, serial, PC DOS, and bytewide memory.

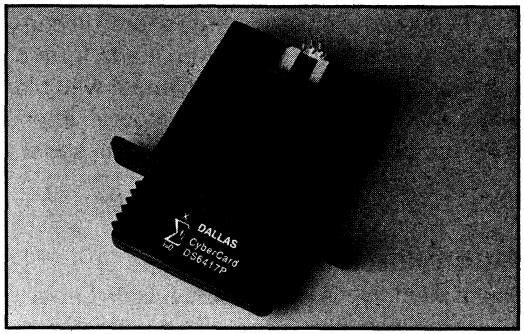
Automatic Identification

Touch Memory™ is a self-stick, Silicon Label™ in a stainless steel can. This MicroCan™ provides all the advantages canning has to offer, such as low cost, ruggedness, and the ability to preserve contents. The MicroCan's greatest advantage, however, is that a standalone chip can leave the confines of the computer and travel virtually anywhere to bring digital data to the point of use. Information can be updated time after time while the label is still affixed to its object. Wherever the silicon-labelled object goes, information is served up on the spot without recourse to remote networks. This family also includes low-cost memory chips in T0-92 packages.



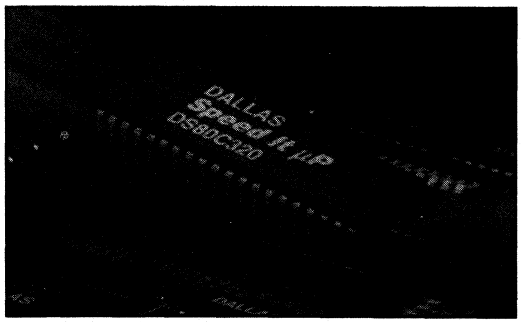
Software Authorization

Software Authorization products protect software applications from unauthorized execution and provide a means for PC and network access control. Software protection is achieved by using a Button as the "on" switch for a software application. The presence of a Button and validity of its contents determine the right to use. Buttons are very effective for implementing time- or count-based metering as a way of extending the temporary right to use software while maintaining protection control.



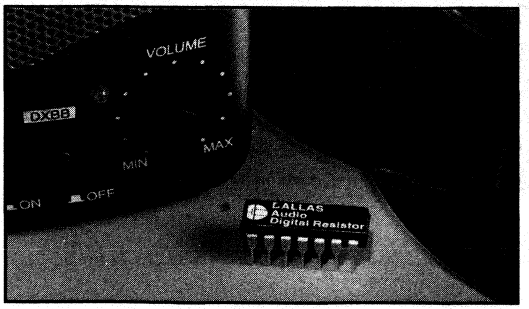
User-Insertable Memory

Nonvolatile memories with densities from 256 to four million bits are packaged so that they can be simply plugged in. A built-in lithium energy source ensures storage of programs and data for more than 10 years in the absence of power. Applications for such products include portable data carrier, computer identification, system access control, secure personnel areas, calibration, automatic system setup, and traveling workrecords. All products can be read or written by a PC.



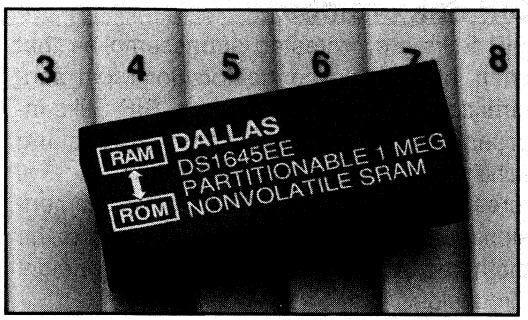
Microcontrollers

The DS80C320 High-Speed Micro is an 8051 family device that offers the highest performance in the industry for an 8-bit microcontroller. Pin- and instruction set-compatible with the standard 80C32, the High-Speed Micro uses only 4 clocks per instruction, as compared with 12 on other 8051's. Our DS500x Soft Micros convert industry-standard bytewide SRAM into high-performance, nonvolatile read/write storage.



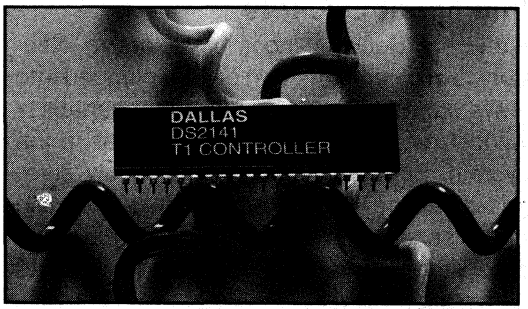
System Extension

These products add a variety of special features to systems without encumbering design. A digital potentiometer is an all-silicon version of an electrical element used in almost all electronic equipment. Whereas mechanical pots are usually brought up to the surface of the equipment and adjusted with a dial, digital pots can be set remotely while they are in a system. CPU supervisors monitor vital conditions for a microprocessor.



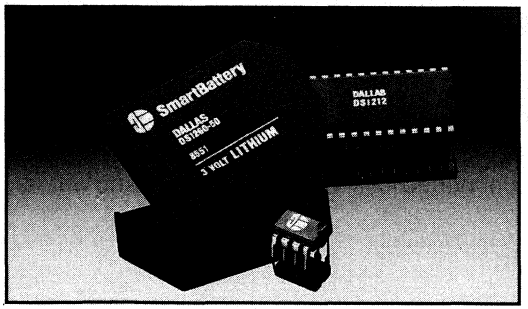
Nonvolatile RAM

Dallas Semiconductor has combined its circuitry and understanding of ultra low-power CMOS SRAM with improvements in long-life lithium power sources to develop a family of nonvolatile RAMs that retain data for more than 10 years in the absence of main power. When power goes out of tolerance, the built-in lithium energy source automatically switches on and write protection guards data from garbling during power loss.



Telecommunications

A comprehensive product family addresses the requirements of high-speed, digital voice/data transmission and monitoring in T1, CEPT, or Primary Rate ISDN networks. ADPCM processors double or quadruple the capacity of voice communication channels through DSP compression techniques.

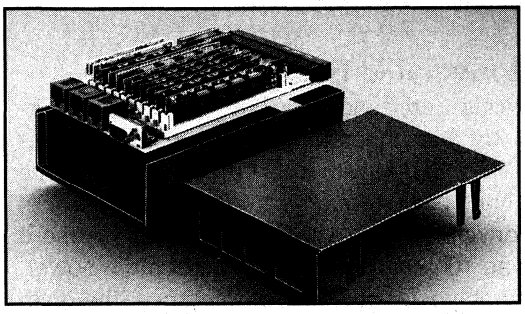


Battery Backup & Chargers

The Battery Backup chip set crashproofs microprocessor-based systems, ensuring that no information is lost when main power fails. When power returns, computing resumes as if the failure had not occurred. Battery Chargers contain all the circuitry needed to recharge a 3-cell NiCad or lithium battery pack in a 3-pin package.

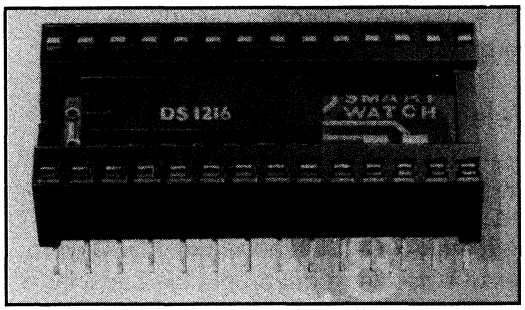
Teleservicing

Teleservicing products can monitor equipment performance 24 hours a day, release software revisions, perform diagnostics, and make adjustments — all from a desktop computer over an ordinary telephone line.



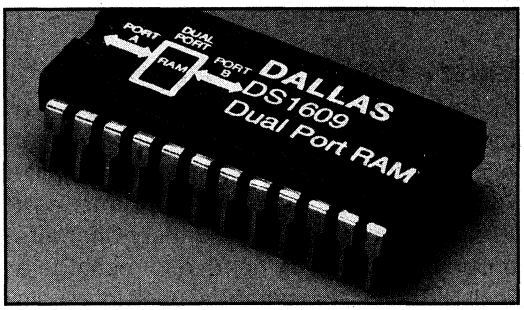
SIP Stik Prefabs

SIP Stiks are pretested subassemblies that snap into locking connectors for rapid construction of electronic systems. SIP Stiks increase density over traditional packing schemes five times by taking advantage of three, rather than the standard two, dimensions. SIP Stiks insert perpendicularly into the motherboard, making efficient use of the height dimension.



Intelligent Sockets

Intelligent Sockets incorporate active electronics in connectors that can be plugged into a system. Each adds an important capability without requiring substantive changes in the system. Some products in this family safeguard data in RAM for more than 10 years in the absence of external power. Others can time stamp and date events as well as nonvolatize RAM.



Multiport Memory

A complete family of FIFOs features identical pinouts that allow them to be interchanged. Designed for first-in, first-out processing for storing and retrieving data, the products are dual-ported for simultaneous reads and writes.

Dallas Semiconductor Corporation designs, manufactures, and markets electronic chips and chip-based subsystems. Founded in 1984, the Company uses customer problems as an entry point to develop products with widespread applications. The Company is committed to new product development as a means to increase future revenues and to diversify its markets, products, and customers.

Advanced technologies have given the Company a competitive edge over traditional approaches to semiconductors. Combining lithium energy cells with low-power CMOS chips powers chips for the useful life of the equipment. Direct laser writing enhances chip capabilities with high levels of precision and unique identities.

In its 10-year history, Dallas Semiconductor has developed 190 base products with over 1,000 variations shipped to more than 8,000 customers worldwide. A direct sales force and distribution network sell to original equipment manufacturers (OEMs) in personal computers and workstations, scientific and medical equipment, industrial controls, automatic identification, telecommunications, consumer electronics, and other markets.

Sales for 1993 totaled $156,860,000. Dallas Semiconductor has 748 employees. On March 19, 1990, the Company started trading on the New York Stock Exchange under the symbol DS.

TECHNOLOGY

Dallas Semiconductor's special technologies make possible Soft Silicon™ solutions—dynamic, flexible, chip-based products that can be molded in the final manufacturing stages or during use. Soft Silicon is made possible by lithium energy and direct laser writing.

Lithium

Using micro energy management techniques, Dallas Semiconductor has reduced power requirements to the point where a miniature lithium energy source powers products for the useful life of the equipment. Chips and Stiks (snap-in subassemblies) are made virtually crashproof with minimum current design techniques and special freshness seals that keep lithium cells from expending any energy until power is applied for the first time. Through these technologies, Dallas products remember data throughout their operating life and can accept change.

Laser

Direct laser writing makes each chip unique at low cost. A sub-micron positioning laser and control software developed at Dallas can engrave individual chips with digital patterns. This ability to routinely alter, reconfigure, or program individual chips after completion of wafer fabrication broadens the application base of products having similar design. Direct laser writing allows Dallas Semiconductor to develop highly accurate products for applications where precision is paramount.

As a result of these Late Definition technologies, exact chip definition can be left to the OEM. Certain chips can even be defined and redefined by the end system itself.

MANUFACTURING AND FACILITIES

As of January 7, 1994, the Company owns 309,000 square feet of building space and 22.9 acres of land in Dallas. The Company's wafer fabrication facility is a model of efficiency and is capable of producing all of its requirements. An expansion of that facility will begin production in mid-1994. When fully equipped, this facility will more than double the Company's fabrication capacity and make available the latest technology, permitting the design of circuits with geometries as small as 0.5 microns.

QUALITY SYSTEM

Product quality at Dallas Semiconductor results from a combination of design techniques, vendor controls, manufacturing methods, process monitors, and quality control inspections. SPC monitors placed at strategic points ensure that potential defects are detected promptly.

QUALITY CONTROL PROCESSES

- *Incoming Quality Control (IQC):* Piece parts and raw materials are inspected by IQC. New vendors and piece parts receive a First Article Inspection; subsequent incoming materials receive a sample inspection per MIL–STD–105.
- *In–Process Inspections:* Each manufacturing operation inspects its own work, ensuring immediate feedback and preventing deviations from going undetected due to subsequent processing.
- *Statistical Process Control (SPC):* Implemented in manufacturing, this process determines what inputs to the product flow are critical and how to track and control those inputs. Quality Engineering provides training, computer analysis, and feedback to manufacturing.
- *In–Process Sample Tests:* In order to guarantee the accuracy and completeness of in–process inspections and SPC monitors, QC Toll Gates at strategic locations perform sample inspections per MIL–STD–105.

RELIABILITY SYSTEM

Reliability is accomplished through a rigorous, comprehensive methodology of qualifying, analyzing, and monitoring new equipment, processes, products, and packages. A state–of–the–art environmental facility allows accelerated stresses to be performed and monitored in–house. In addition, a metallurgical laboratory has been equipped to perform real-time x–ray, x–ray florescence, and solderability measurements.

To minimize the human influence on the outcome of the reliability activity, a dedicated group of technicians and assistants handle all reliability stressing and testing. Reliability data resides on a customized computer–based tracking and retrieval system. Technical support includes oven and chamber calibrations, 100% electrical board checks, and strict electrostatic protection.

PRODUCT QUALIFICATION

Product qualification activity at Dallas Semiconductor involves a series of accelerated stress tests applied to production–ready material and follows a defined qualification plan. Random samples from at least three production lots, equally representing the production version of the product, are tested to meet reliability requirements. Any device failures detected during production qualification or subsequent monitoring are fully analyzed in our Failure Analysis Laboratory.

Products at Dallas Semiconductor fall into one of three classifications: Prototype or Engineering Sample, Prequal, and Fully Qualified.

- *Prototype or Engineering Sample:* Prototype products have not been fully characterized to all data sheet limits. However, based upon limited data, these products will meet data sheet limits. Final test and all processes used to manufacture the product are under engineering control. Qualification of the product has not started. The brand on prototype products will be PROTO or ES.
- *Prequal:* Prequal products meet prototype requirements and are characterized to all data sheet limits. Final test and all processes used to manufacture the product are stable and under manufacturing control. Qualification of the product has started.
- *Fully Qualified:* Fully qualified products meet prototype and prequal requirements. The qualification requirements given in the next section have been completed. Product must statistically meet reliability failure rates and quality requirements as established by Quality and Reliability Engineering.

Tables 1, 2 and 3 list the tests which a Dallas Semiconductor product must pass in order to be classified as fully qualified.

RELIABILITY MONITOR PROGRAM

In order to maintain continuous qualification status on all products, Dallas Semiconductor has implemented an extensive Reliability Monitor Program (RMP). The RMP monitors all design, wafer fabrication, and assembly processes in the qualified products database. Product is selected monthly from finished goods and subjected to a series of reliability tests similar to those used in the original qualification. Any failures generated from these tests require analysis to root cause and corrective action.

Data from the RMP is published quarterly and is available on demand.

FULL QUALIFICATION REQUIREMENTS FOR INTEGRATED CIRCUIT PRODUCTS Table 1

STRESS/TEST	CONDITION	DURATION	ACCEPTANCE CRITERIA (LTPD)
Outgoing Elec. Test	Data Sheet	0 Hr.	0.15%
Infant Life	125°C, 7.0V	48 Hr.	0.3%
High Temperature Operating Life	125°C, 5.5V	1000 Hr.	*0.4%
Use Condition Prediction	55°C, 5.5V	10 years	50 Fits
High Voltage Life	125°C, 7.0V	1000 Hr.	*0.4%
High Temperature Storage	150°C, No Bias	1000 Hr.	2.0%
Temperature Humidity Bias	85°C/85% RH, 5.5V	1000 Hr.	1.0%
Autoclave	121°C, 2 ATM Steam, Unbiased	168 Hr.	1.5%
Temperature Cycle	–55°C to +125°C	1000 cycle	1.0%
X–Ray	MIL–STD–883 Method 2012		15%
Bond Pull	MIL–STD–883 Method 2011	Premold	1.5%
Dimensions	MIL–STD–883 Method 2016		15%
Lead Integrity	MIL–STD–883 Method 2004		3.0%
Solderability	MIL–STD–883 Method 2003	8 Hr. Steamage	3.0%
ESD	MIL–STD–883 Method 3015		> ±1000 volts
Latch–up	JEDEC Std. 17		> 100 mW/pin

* Combined high voltage life and operating life requirement.

FULL QUALIFICATION REQUIREMENTS FOR MODULE PRODUCTS Table 2

STRESS/TEST	CONDITION	DURATION	ACCEPTANCE CRITERIA (LTPD)
Outgoing Elec. Test	Data Sheet	0 Hr.	0.15%
Use Condition Prediction	55°C, 5.5V	10 years	50 Fits
High Temperature Storage	85°C, No Bias	1000 Hr.	2.0%
*Temperature Humidity Bias	85°C/85% RH, 5.5V	959 Hr.	1.0%
Temperature Cycle	–40°C to +85°C	1000 cycle	1.0%
X–Ray	MIL–STD–883 Method 2012		15%
Dimensions	MIL–STD–883 Method 2016		15%
Lead Integrity	MIL–STD–883 Method 2004		3.0%
Solderability	MIL–STD–883 Method 2003	8 Hr. Steamage	3.0%

* Selected products.

FULL QUALIFICATION REQUIREMENTS FOR SIPSTICK AND TOUCH MEMORY PRODUCTS Table 3

STRESS/TEST	CONDITION	DURATION	ACCEPTANCE CRITERIA (LTPD)
Outgoing Elec. Test	Data Sheet	0 Hr.	0.15%
High Temperature Storage	85°C, No Bias	1000 Hr.	7.0%
Temperature Humidity	60°C/90% RH	288 Hr.	7.0%
Temperature Cycle	–40°C to +85°C	500 cycle	7.0%

BATTERY MANAGEMENT

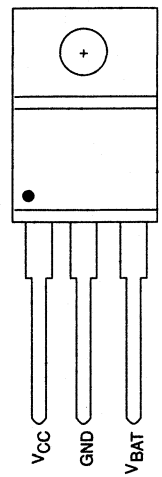
DALLAS SEMICONDUCTOR

DS1633
High–Speed Battery Recharger

FEATURES

- Recharges Lithium, NiCad, NiMH and Lead acid batteries
- Retains battery and power supply limits in onboard memory
- Serial 1–wire interface is used to program operating limits
- 3-pin TO–220 package
- Operating range 0°C to 70°C
- Applications include consumer electronics, portable/ cellular phones, pagers, medical instruments, backup memory systems, security systems
- Configurable to operate with 5V or 6V supplies

PIN ASSIGNMENT TO–220



See Mech. Drawing Pg. 488

PIN DESCRIPTION

V_{CC}	–	Supply Voltage
V_{BAT}	–	Battery Output
GND	–	Ground

DESCRIPTION

The DS1633 Battery Recharger is designed to be a complete battery charging system for standard charge or trickle charge applications. It can be configured to be used with either 5V or 6V supplies and battery voltages as high as 4.7V (3.7V for 5V supplies). The device is flexible enough to be used with a variety of battery chemistries and cell capacities. It provides timer termination of standard charge and automatically shifts into trickle charge. Battery voltage can be monitored and charging terminated if it exceeds a preset maximum as a safety feature. The output load line can be specified as the usual constant current recharge with a voltage limit or it can be configured to approximate any practical load line. All parameters, such as power supply range, charge current load line, trickle charge rate, and timer setting, are programmed into nonvolatile memory using the battery pin as a 1–wire communication port. To ease the task of configuring the device to specific application needs, Dallas Semiconductor makes available a programming kit, the DS1633K, containing easy–to–use software and hardware for IBM personal computers.

The DS1633 is able to offer this flexibility due to its unique architecture (see Figure 1). The device monitors the battery voltage and adjusts the values of the output impedance (R_{TH}) and open circuit voltage (V_{OC}) it presents to the battery. These values can be adjusted at 32 user definable points (breakpoints) that occur roughly every 37mV. This allows the device to approximate a wide range of charging lines; it is not limited to constant current or even monotonically decreasing functions.

OPERATION

Normal Mode

Upon application of power, the DS1633 will perform an initialization cycle requiring eight seconds. During this period it will determine if a battery is connected to the battery input by applying a voltage through 5 KΩ output impedance and looking for a non–zero current flow out of the pin. If a battery is connected, the value of the battery voltage will be determined using a 7–bit A/D convertor. This value will be used to determine which of the 32 user–defined breakpoints should be used to set R_{TH} and V_{OC}. Generally, as the battery charges the battery voltage will increase. When the battery voltage reaches or exceeds each user–defined breakpoint, the values of R_{TH} and V_{OC} will be modified accordingly. The battery voltage is measured and adjustments are made every eight seconds. The battery detection is performed at one–second intervals. If the amount of time the battery has been charging exceeds the preset limit, the device will apply the V_{OC} and R_{TH} as before, but only for a fraction of the eight–second cycle time. This duty cycle can be as low as 1/64 or as high as 1. In this way trickle charge can be accomplished by time averaging a short pulse over a longer period. Refer to Figure 2 for a detailed flow diagram of normal operation.

PROGRAMMING MODE

Register Structure

To configure a DS1633 to operate with a unique load line the user must program a set of 25–bit internal registers (Table 1). The first 32 (0–31) of these registers contain the information needed to locate each breakpoint and what the R_{TH} and V_{OC} are at that breakpoint, as well as the duty cycle to be used after the optional timer has expired. The last (32) register contains the bits which select the system power supply level (5V or 6V), the timer option, and the time limit (2 to 32 hours in 2–hour increments).

BREAKPOINT REGISTER STRUCTURE

Break Point Voltage Field

The break point voltage field specifies the range of battery voltage over which the R_{TH}, V_{OC} and pulse frequency information contained in that register is valid. This information is valid when the battery voltage meets or exceeds the breakpoint value, but is less than the next breakpoint value:

$$V_{BPX} \leq V_{BAT} < V_{BP(x+1)}$$

The xth breakpoint voltage (V_{BPX}) is determined according to the following formula:

$$V_{BPX}(n) = (n/127)(4.699V) \text{ ; for } 0 \leq n \leq 127$$

The value for n is entered in the field as a 7–bit binary value, LSB first. For reliable operation the first (x=0) breakpoint should be programmed such that $V_{BP0} = 0$. Successive breakpoints should be programmed with increasing values, that is:

$$V_{BPX} < V_{BP(x+1)}$$

If not all of the available breakpoints are used, the unused points should be assigned the maximum V_{BP} value (n=127) of 4.699V with R_{TH} and V_{OC} set to their maximum values (5060Ω and 5.5V) and the duty cycle field set to its minimum or zero value.

OPEN CIRCUIT VOLTAGE FIELD

The open circuit voltage field specifies the value of V_{OC} to be applied to the battery. V_{OC} can be set for values between 1.3V and 5.5V. This field is entered as a 7–bit binary value, LSB first. The value of $V_{OC}(n)$ is determined as follows:

$$V_{OC}(n) = 1.3V + n(5.5V - 1.3V)/127 \text{ ; for } 0 \leq n \leq 127$$

For reliable operation of the battery detection circuitry, the minimum value of V_{OC} should be greater than the maximum battery voltage.

THEVENIN RESISTANCE FIELD

The Thevenin resistance field specifies the value of output resistance between the low impedance V_{OC} source and the battery pin. This resistance can have one of 128 values ranging from 5060Ω to 7.5Ω with a 5% difference in successive values. This field is entered as a 7–bit binary value, LSB first. The value of $R_{TH}(n)$ is determined as follows:

$$R_{TH}(n) = 7.5(0.95^{n-127}) \text{ ; for } 0 \leq n \leq 127$$

PULSE WIDTH FIELD

The pulse width field specifies the amount of time (PW) during each eight second charging and evaluation cycle that V_{OC} and R_{TH} will be applied after the optional timer has expired. PW can have one of 8 values ranging from 8 seconds to 0. The field is entered as a 3–bit binary value, LSB first. The value of PW is determined as follows:

$$PW(n) = 2^n/16 \text{ ; for } 1 \leq n \leq 7$$

$$PW(n) = 0 \text{ ; for } n = 0$$

CHARGE ON FIELD

This is a one bit field which specifies if V_{OC} and R_{TH} for this breakpoint are to be applied at all for the case of an unexpired timer. Its usefulness is in permitting certain breakpoints to be turned off if the battery voltage exceeds a maximum during standard charge. If the timer has expired or is not used, this is accomplished for those breakpoints using the 3 pulse width bits (PW = 000).

A one in this field means that the V_{OC} and R_{TH} are to be applied when the breakpoint is the current one.

CONFIGURATION REGISTER STRUCTURE

V_{TRIP} Field

This is a one–bit field which specifies the valid supply voltage for the device. A one in this field indicates a 6V system is being used and the part will not begin charging until the applied V_{CC} exceeds 5.7V. Conversely, a zero indicates a 5V system and charging will begin when V_{CC} exceeds 4.75V.

TIMER STATUS FIELD

This is a one bit field which indicates if the timer is to be used. A one in this field indicates that timer is used, a zero that it is not.

TIMER VALUE FIELD

This field specifies the maximum time (T_{MAX}) for standard or non–pulsed charging. During the period when the timer has not expired, V_{OC} and R_{TH} will be applied to the battery input if the charge on bit is a one. When the elapsed charge time exceeds the value in this register, V_{OC} and R_{TH} will be applied at a duty cycle determined by the PW field for each breakpoint. The field is entered as a 4–bit binary value, LSB first. The timer can have values from 2 to 32 hours, determined by the following:

$$T_{MAX}(n) = 2(n + 1) \text{ ; for } 0 \leq n \leq 15$$

PROGRAMMING OPERATION

The data for the 33 registers is stored in nonvolatile memory and can be written only once. All 33 registers must be programmed before any can be read. Note that although the configuration register contains only 6 bits, 25 bits are required to be entered; therefore, fill it with 19 0's. The registers are programmed sequentially, starting at register 0. As each register is programmed, an internal pointer moves to the next register until all 33 have been programmed. To enter the program/read mode, V_{CC} must be taken to 8V for a minimum of 1 ms and returned to 5V. The V_{BAT} pin is now configured to operate as a single wire I/O line. The hardware interface is shown in Figure 3.

RESET TIMING

To issue a reset to the device the V_{BAT} pin must be brought low and held low for a minimum of 480 µs after which it is released and will return to a high level through the internal pullup resistor. After the line is allowed to return high it must not be pulled low for at least 1 µs. Refer to Figure 4.

WRITE TIMING

A logic 0 is written by bringing the V_{BAT} pin low for at least 60 µs, but not more than 120 µs. A logic 1 is written by bringing the V_{BAT} pin low for at least 1 µs, but not more than 15 µs. After the line is allowed to return high it must not be pulled low for at least 60 µs. Refer to Figure 4.

READ TIMING

A read is performed by bringing the V_{BAT} pin low for at least 1 µs, but not more than 5 µs and then releasing it. A logic 1 is indicated by the pin returning high. The state of the V_{BAT} pin should be sampled at most 15 µs after V_{BAT} is pulled low. A high level indicates a read '1', a low level indicates a read '0'.

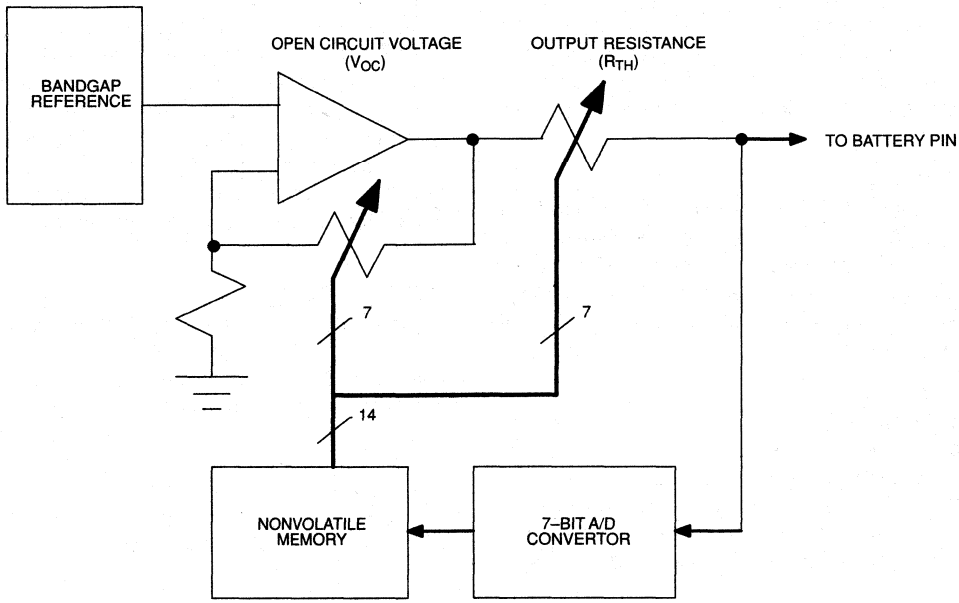
PROGRAMMING

To program the DS1633 the single line I/O must be enabled by bringing V_{CC} to 8V for at least 1 ms and then back to 5V. The first register can now be written. The register data must be preceded by 3 consecutive logic 1 write cycles. The register data can now be entered according to the write cycle timing detailed above, from LSB to MSB. To commit the data to the nonvolatile memory the V_{BAT} pin is brought to 12V, with V_{CC} at 8V, for at least 250 ms. When V_{BAT} is released and returns to 5V and a reset cycle is issued the device is ready for the next register. Be careful not to issue multiple resets as this will move the pointer. This sequence is repeated until all 33 registers are programmed. When all registers have been programmed, the DS1633 disables the serial interface and begins normal operation.

VERIFICATION

To verify the data contained in the registers the single line I/O must be enabled by bringing V_{CC} to 8V for at least 1 ms. Unlike the programming operation, the read operation allows random access of the registers. A read cycle is preceded by 4 logic ones, a 6–bit register address, entered LSB first, and 18 logic ones. The device will now output the contents of the register, LSB first, on the next 25 read cycles. To read another register, issue a reset and repeat the sequence.

SIMPLIFIED BLOCK DIAGRAM Figure 1

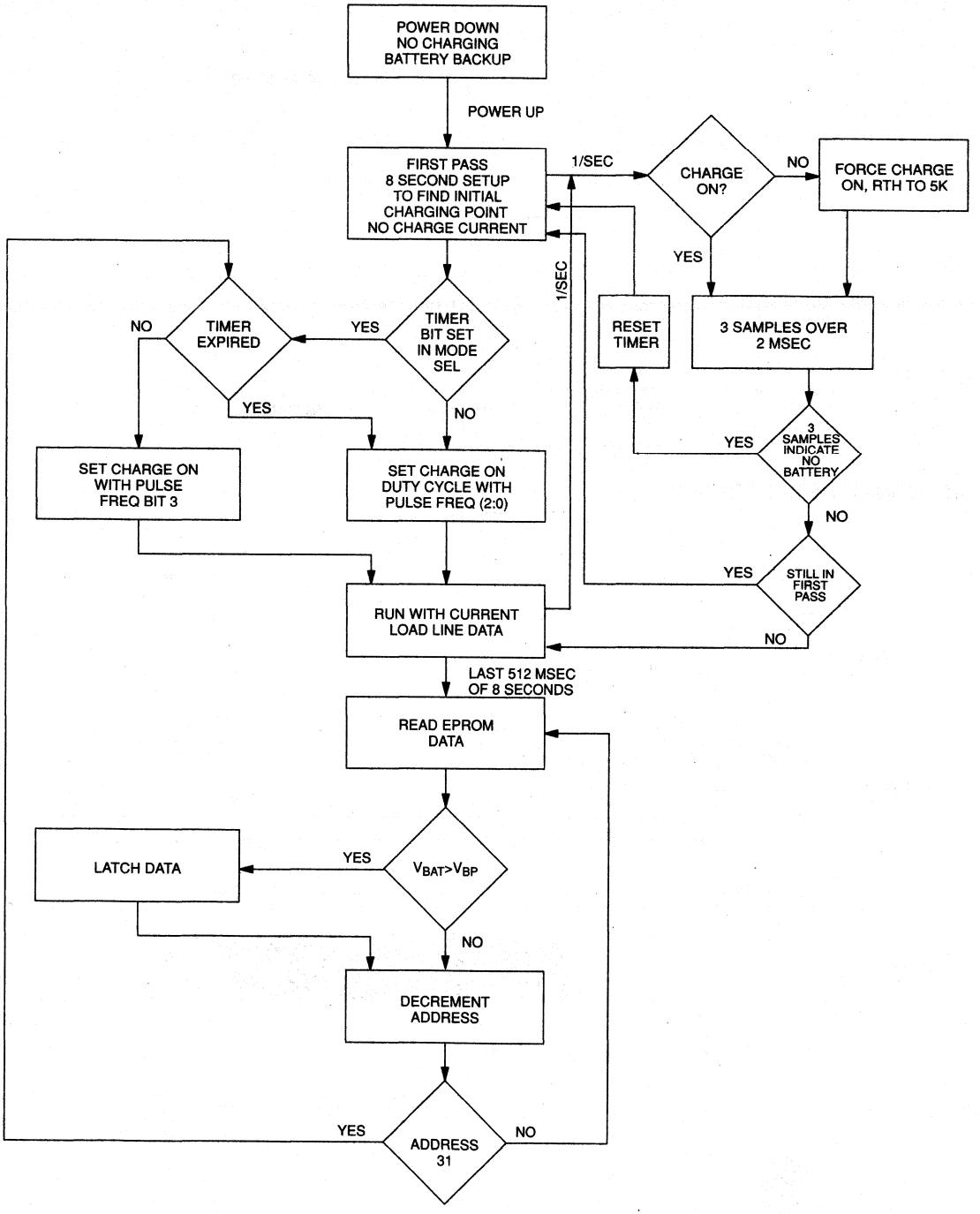


DS1633 REGISTER STRUCTURE Table 1

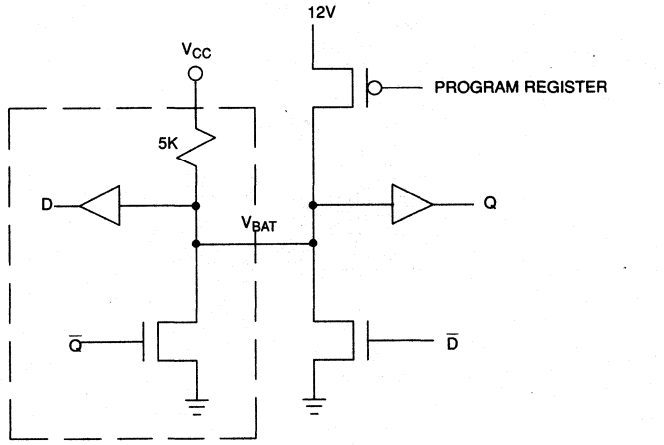
MSB **DS1633 MEMORY ARRAY MAP** **LSB**

REGISTER	CHARGE ON	PULSE WIDTH	THEVENIN RESISTANCE FIELD	OPEN CIRCUIT VOLTAGE	BREAKPOINT VOLTAGE		
0	CO_0	PW_0	R_{TH0}	V_{OC0}	V_{BP0}		
1							
2							
3							
•							
•							
•							
30							
31	CO_{31}	PW_{31}	R_{TH31}	V_{OC31}	V_{BP31}		
32	MUST FILL UNUSED BITS WITH 0'S				TIMER VALUE	TIMER STATUS	V_{TRIP}

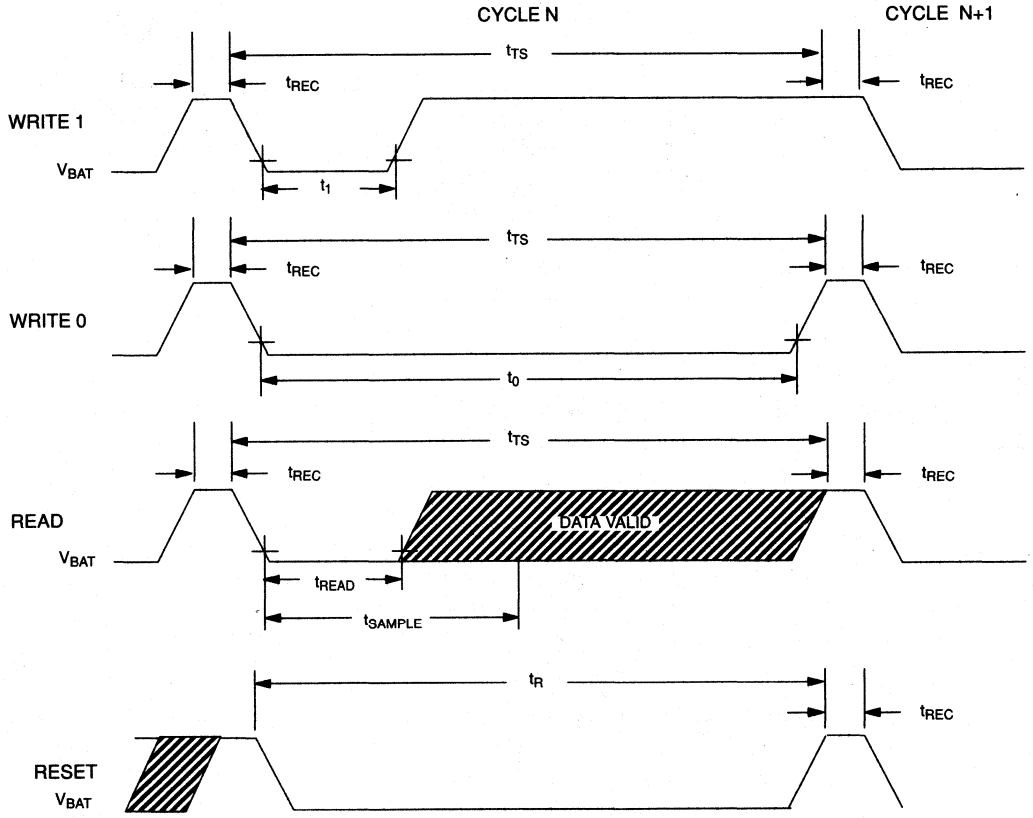
DS1633 OPERATION FLOW CHART Figure 2



HARDWARE INTERFACE FOR PROGRAMMING Figure 3



I/O SIGNAL TIMING Figure 4



REGISTER VALUE CROSS REFERENCE Table 2

HEX	DEC	R_{TH}	V_{OC}	V_{BP}
00	0	5.060E+03	1.30	0.000
01	1	4.807E+03	1.33	0.037
02	2	4.567E+03	1.37	0.074
03	3	4.338E+03	1.40	0.111
04	4	4.122E+03	1.43	0.148
05	5	3.915E+03	1.47	0.185
06	6	3.720E+03	1.50	0.222
07	7	3.534E+03	1.53	0.259
08	8	3.357E+03	1.56	0.296
09	9	3.189E+03	1.60	0.333
0A	10	3.030E+03	1.63	0.370
0B	11	2.878E+03	1.66	0.407
0C	12	2.734E+03	1.70	0.444
0D	13	2.598E+03	1.73	0.481
0E	14	2.468E+03	1.76	0.518
0F	15	2.344E+03	1.80	0.555
10	16	2.227E+03	1.83	0.592
11	17	2.116E+03	1.86	0.629
12	18	2.010E+03	1.90	0.666
13	19	1.909E+03	1.93	0.703
14	20	1.814E+03	1.96	0.740
15	21	1.723E+03	1.99	0.777
16	22	1.637E+03	2.03	0.814
17	23	1.555E+03	2.06	0.851
18	24	1.478E+03	2.09	0.888
19	25	1.404E+03	2.13	0.925
1A	26	1.333E+03	2.16	0.962
1B	27	1.267E+03	2.19	0.999
1C	28	1.203E+03	2.23	1.036
1D	29	1.143E+03	2.26	1.073
1E	30	1.086E+03	2.29	1.110
1F	31	1.032E+03	2.33	1.147
20	32	9.802E+02	2.36	1.184
21	33	9.312E+02	2.39	1.221
22	34	8.846E+02	2.42	1.258
23	35	8.404E+02	2.46	1.295
24	36	7.984E+02	2.49	1.332
25	37	7.585E+02	2.52	1.369
26	38	7.205E+02	2.56	1.406
27	39	6.845E+02	2.59	1.443
28	40	6.503E+02	2.62	1.480
29	41	6.178E+02	2.66	1.517
2A	42	5.869E+02	2.69	1.554
2B	43	5.575E+02	2.72	1.591
2C	44	5.297E+02	2.76	1.628
2D	45	5.032E+02	2.79	1.665
2E	46	4.780E+02	2.82	1.702
2F	47	4.541E+02	2.85	1.739
30	48	4.314E+02	2.89	1.776
31	49	4.098E+02	2.92	1.813
32	50	3.894E+02	2.95	1.850
33	51	3.699E+02	2.99	1.887
34	52	3.514E+02	3.02	1.924
35	53	3.338E+02	3.05	1.961
36	54	3.171E+02	3.09	1.998
37	55	3.013E+02	3.12	2.035
38	56	2.862E+02	2.15	2.072
39	57	2.719E+02	3.19	2.109
3A	58	2.583E+02	3.22	2.146
3B	59	2.454E+02	3.25	2.183
3C	60	2.331E+02	3.28	2.220
3D	61	2.215E+02	3.32	2.257
3E	62	2.104E+02	3.35	2.294
3F	63	1.999E+02	3.38	2.331
40	64	1.899E+02	3.42	2.368
41	65	1.804E+02	3.45	2.405
42	66	1.714E+02	3.48	2.442
43	67	1.628E+02	3.52	2.479
44	68	1.547E+02	3.55	2.516
45	69	1.469E+02	3.58	2.553
46	70	1.396E+02	3.61	2.590
47	71	1.326E+02	3.65	2.627
48	72	1.260E+02	3.68	2.664
49	73	1.197E+02	3.71	2.701
4A	74	1.137E+02	3.75	2.738
4B	75	1.080E+02	3.78	2.775

HEX	DEC	R_{TH}	V_{OC}	V_{BP}
4C	76	1.026E+02	3.81	2.812
4D	77	9.747E+01	3.85	2.849
4E	78	9.260E+01	3.88	2.886
4F	79	8.797E+01	3.91	2.923
50	80	8.357E+01	3.95	2.960
51	81	7.939E+01	3.98	2.997
52	82	7.542E+01	4.01	3.034
53	83	7.165E+01	4.04	3.071
54	84	6.807E+01	4.08	3.108
55	85	6.467E+01	4.11	3.145
56	86	6.143E+01	4.14	3.182
57	87	5.836E+01	4.18	3.219
58	88	5.544E+01	4.21	3.256
59	89	5.267E+01	4.24	3.293
5A	90	5.004E+01	4.28	3.330
5B	91	4.753E+01	4.31	3.367
5C	92	4.516E+01	4.34	3.404
5D	93	4.290E+01	4.38	3.441
5E	94	4.076E+01	4.41	3.478
5F	95	3.873E+01	4.44	3.515
60	96	3.678E+01	4.47	3.552
61	97	3.494E+01	4.51	3.589
62	98	3.320E+01	4.54	3.626
63	99	3.154E+01	4.57	3.663
64	100	2.996E+01	4.61	3.700
65	101	2.846E+01	4.64	3.737

HEX	DEC	R_{TH}	V_{OC}	V_{BP}
66	102	2.704E+01	4.67	3.774
67	103	2.569E+01	4.71	3.811
68	104	2.440E+01	4.74	3.848
69	105	2.318E+01	4.77	3.885
6A	106	2.202E+01	4.81	3.922
6B	107	2.092E+01	4.84	3.959
6C	108	1.988E+01	4.87	3.996
6D	109	1.888E+01	4.90	4.033
6E	110	1.794E+01	4.94	4.070
6F	111	1.704E+01	4.97	4.107
70	112	1.619E+01	5.00	4.144
71	113	1.538E+01	5.04	4.181
72	114	1.461E+01	5.07	4.218
73	115	1.388E+01	5.10	4.255
74	116	1.319E+01	5.14	4.292
75	117	1.253E+01	5.17	4.329
76	118	1.190E+01	5.20	4.366
77	119	1.131E+01	5.24	4.403
78	120	1.074E+01	5.27	4.440
79	121	1.020E+01	5.30	4.477
7A	122	9.693E+00	5.33	4.514
7B	123	9.208E+00	5.37	4.551
7C	124	8.748E+00	5.40	4.588
7D	125	8.310E+00	5.43	4.625
7E	126	7.895E+00	5.47	4.662
7F	127	7.500E+00	5.50	4.699

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
5V Mode Supply Voltage, Operation	V_{CC1}	4.75	5	6.5	V	1,2
6V Mode Supply Voltage, Operation	V_{CC2}	5.7	6	6.5	V	1,3,4
Supply Voltage, V_{BAT}, Programming	V_{BATP}	12	12	13	V	
I_{BAT}, Programming	I_{BATP}			100	µA	
V_{CC} Supply Voltage, Programming	V_{CC3}	8		8.5	V	
Logic 1 Input	V_{IH}	2.0	–	V_{CC}+0.3	V	
Logic 0 Input	V_{IL}	–0.3	–	+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5.75V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current, Operation Mode	$I_{CC1,2}$			1	mA	6
Supply Current, Programming Mode	I_{CC3}			10	mA	
Output Low, Voltage	V_{OL}			0.4	V	
Output Low, Current	I_{OL}	1			mA	
V_{BAT} Leakage Current with V_{CC} at 0V	I_{BAT}			100	nA	5
Pullup resistance on I/O	R_{PU}		5K			
Breakpoint Voltage (n=0)	$V_{BP}(0)$		0		V	
Breakpoint Voltage (n=127)	$V_{BP}(127)$	4.649	4.699	4.749	V	
Open Circuit Voltage (n=0)	$V_{OC}(0)$		1.3		V	
Open Circuit Voltage (n=127)	$V_{OC}(127)$	5.45	5.50	5.55	V	
Thevenin Resistance (n=0)	$R_{TH}(0)$		7.5		Ω	7
Thevenin Resistance (n=127)	$R_{TH}(127)$	4933	5060	5187	Ω	7
Timer Value (n=0)	$T_{MAX}(0)$	1.8	2	2.2	hours	
Timer Value (n=15)	$T_{MAX}(127)$	28.8	32	35.2	hours	

AC ELECTRICAL CHARACTERISTICS: DATA TRANSMISSION PARAMETERS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Active	t_R	480			µs	
Logic 1 Active Low	t_1	1		15	µs	
Logic 0 Active Low	t_0	60		120	µs	
Read Enable Time	t_{READ}	1		5	µs	
Time from Read Enable to I/O Line Sampling	t_{SAMPLE}			15	µs	
Data Transfer Window	t_{TS}	60		120	µs	
Active Signal Pulse Width, Data I/O	t_{PW}	60		120	µs	
Recovery Time Between Windows	t_{REC}	1			µs	
Programming Pulse Width, V_{BAT}	t_{PRG}	250			ms	

NOTES:

1. All voltages referenced to ground.
2. 5V operation conditions.
3. 6V operation conditions.
4. For any $V_{OCMAX} \geq 4.5V$, $V_{TRIP} = 5.7V$ (6V operation) must be used.
5. High impedance isolation between V_{BAT} and V_{CC} with $V_{CC}=0$ is $\geq 45G\Omega$.
6. Does not include current supplied to the battery pin.
7. At 25°C, R_{TH} has a positive temperature coefficient of approximately 800 ppm/°C.

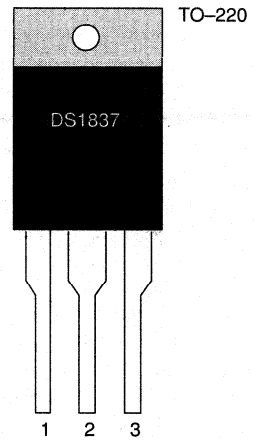
DALLAS SEMICONDUCTOR

DS1837
Quick Battery Recharger

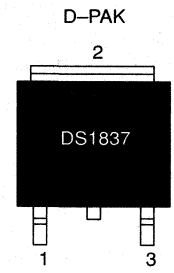
FEATURES

- Provides constant–current quick charge of up to 750 mA for NiCd, NiMH, lithium, and lead acid batteries
- No external components required
- Can easily charge 6–cell NiCd battery packs
- Charge termination by maximum voltage (VCO), and maximum time
- Retains charging parameters in on–board memory; programmable over serial one–wire interface
- Available in TO–220 or surface mount D–PAK packages
- Operating range of 0°C to 70°C
- Applications include portable computers, portable/ cellular phones, consumer electronics, and handheld instrumentation

PIN ASSIGNMENT



See Mech. Drawing Pg. 488



See Mech. Drawing Pg. 489

PIN DESCRIPTION

1	V_{CC}
2	GND
3	V_{BAT}

DESCRIPTION

The DS1837 Quick Battery Recharger is designed to be a complete battery charging system for quick, standard, and trickle charge applications. It can be configured to be used with supply voltages from 6V to 12V and battery voltages as high as 9.6V. The device is flexible enough to be used with a variety of battery chemistries and cell capacities. It provides a constant–current quick or standard charge with timer termination and automatically shifts into trickle charge. Battery voltage may be monitored and charging terminated if it exceeds a preset maximum as a safety feature. All parameters (charging current, trickle current, timer setting, and maximum battery voltage) are programmed into nonvolatile memory using the battery pin as a one–wire communication port. To ease the task of configuring the device to specific application needs, Dallas Semiconductor makes available a programming kit, the DS1837K, containing easy to use software and hardware for IBM–compatible personal computers.

BATTERY CHARGING AND TERMINATION TECHNIQUES

Batteries are made up of cells; several cells may be connected in series to achieve higher output voltages. Typical cell operating voltages are 1.2V for NiCd and NiMH batteries; lead–acid cells are about 2V, and lithium cells are approximately 3V. It is important to know the chemical makeup of your battery, and the number of cells which it has, in order to assure a reliable, effective, and safe charging sequence.

Cell capacity is specified as the cumulative current a cell can supply over time, usually measured in units of ampere–hours. The parameter for describing current is the C rate. The C rate expressed in units of amperes or milliamperes is numerically equal to the capacity of the cell expressed in units of ampere–hours or milliampere–hours. For example, the C rate for a 600 mAh battery is 600 milliamperes. A 300 mA charge current to the same battery is a 1/2C or C/2 rate.

During charging, current is injected into the cell to reverse the electrochemical reaction which takes place in the cell. This results in an increase in cell voltage. Eventually, the current applied to the cell is no longer converted to stored energy. Instead, it produces heat, and there is a marked increase in cell temperature and pressure. This condition is called overcharge.

There are several factors to consider in determining the best method of charging a battery. Excess cell pressure is to be avoided, as it may cause venting of the cell, which results in the loss of electrolyte and battery capacity. Heating is also a concern, as cell temperature also affects its life. While in the past charge rates have been low and have been able to continuously charge a cell, the time taken to fully charge a battery has been extremely long (14 to 20 hours). New battery formulations allow for charging at higher rates, but the potential for developing battery–damaging temperatures and pressures in overcharge require that the charge current be carefully controlled.

Charge rates of around 0.3C are termed by battery manufacturers as "quick" charge, while rates of around 0.1C are considered "standard" charge. Quick charging charges a battery in 4 to 6 hours, while standard charge takes 12 to 14 hours typically. Knowing when to terminate the charging process is critical to prevent spending excessive time in an overcharge state. These two charging techniques typically use a timer to measure the time that the charge current has been applied, and then terminates charging when the timer expires, usually then shifting into a trickle mode where a 0.01C to 0.05C current is applied to maintain charge on the battery. Another method of terminating standard or quick charging is to monitor the battery voltage and terminate charging when the battery voltage exceeds some threshold.

At higher charge rates (0.5C to 4C), these two termination methods are not recommended, as the potential for spending excessive time in overcharge is higher. Higher rate chargers usually require measuring battery temperature or change in battery voltage over time ($-\Delta V$) to determine when to terminate charging.

DETAILED PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	V_{CC}	**Power Supply** Input; 6V to 12V nominal.
2	GND	**Ground pin.**
3	V_{BAT}	**Battery** connection.

OPERATION

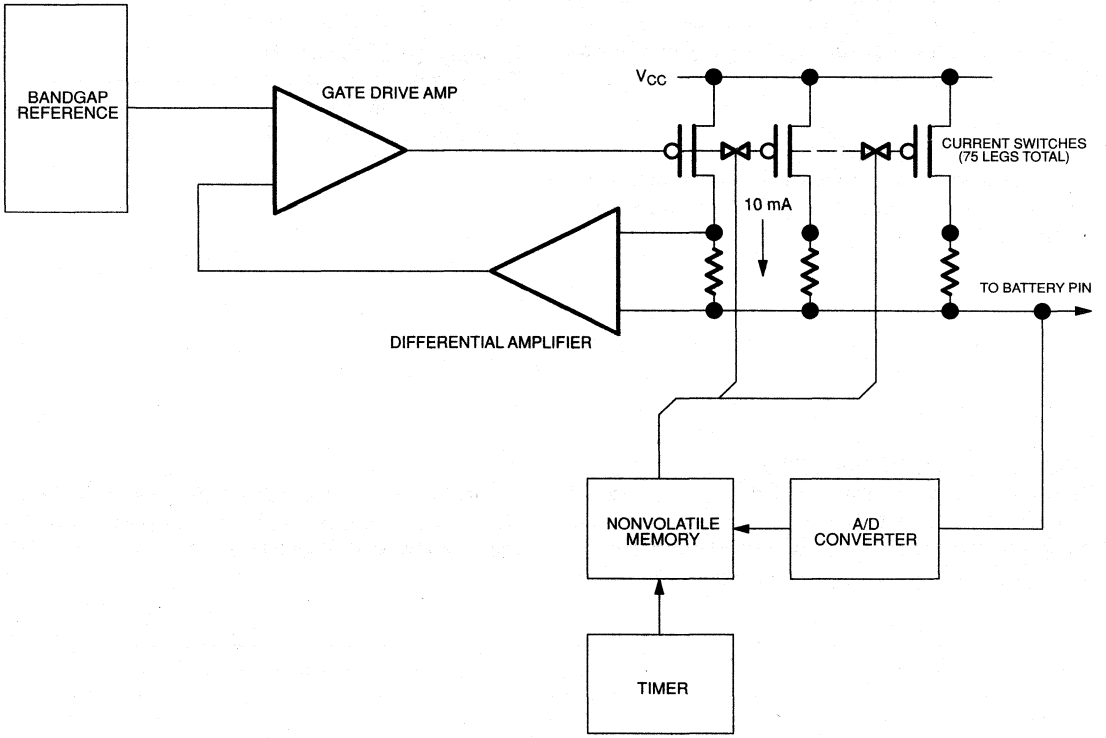
A block diagram of the DS1837 is shown in Figure 1. The DS1837 consists of 75 precision 10 mA current sources. The current is controlled through the use of a precision voltage reference, a differential amplifier, and a gate drive amplifier which adjusts the gate drive to the current sources to achieve 10 mA per leg. The charging current is realized by turning on the appropriate number of current sources (750 mA = all 75 sources on, 500 mA = 50 sources on). In addition to the current sources, an A/D converter is present to measure the battery voltage. A timer is included for use in termination of charge. All charging parameters reside in nonvolatile memory.

Upon application of power the DS1837 will perform an initialization cycle. During this period it will determine if a battery is connected to the battery input. If a battery is connected, the value of the battery voltage will be determined using the A/D converter.

Generally, as the battery charges the battery voltage will increase. When the battery voltage reaches or exceeds the user programmed limit, the standard charge rate will be decreased to the trickle charge rate. Likewise, should the amount of time which the battery has been charging exceed the preset limit the device will decrease the charge current to the trickle rate, by turning off the appropriate number of 10mA current sources.

Note that since the DS1837 is a high–current device, appropriate heat sinking is required.

DS1837 FUNCTIONAL BLOCK DIAGRAM Figure 1



PROGRAMMING THE DS1837

To configure a DS1837 for a given charge current and time, the user must specify four parameters in four 8–bit registers. These are described below.

I_{CHG} [REGISTER 0]

This register contains the value of the charging current, expressed as follows:

$I_{CHG}[0]$=10 mA	LSB
$I_{CHG}[1]$=10 mA	
$I_{CHG}[2]$=20 mA	
$I_{CHG}[3]$=40 mA	
$I_{CHG}[4]$=80 mA	
$I_{CHG}[5]$=160 mA	
$I_{CHG}[6]$=320 mA	
$I_{CHG}[7]$=110 mA	MSB

These values sum to 750 mA.

For a charge current of 200 mA, I_{CHG} would be set as 28h, or 00101000 binary.

BATMAX [REGISTER 1]

This register contains the value of the maximum battery voltage allowed for standard charge. This is expressed in terms:

$$BATMAX \geq \frac{320}{\text{max battery V}}$$

For example, a maximum battery voltage of 9.6V would require that

$$BATMAX \geq \frac{320}{9.6V} = 33.333$$

so, BATMAX would be set as 34, or 00100010 binary.

t [REGISTER 2]

This register specifies the maximum time (T_{MAX}) for standard charging. The register only uses the four LSBs of the 8 bit register. The timer can have values from 2 to 32 hours, determined by the following:

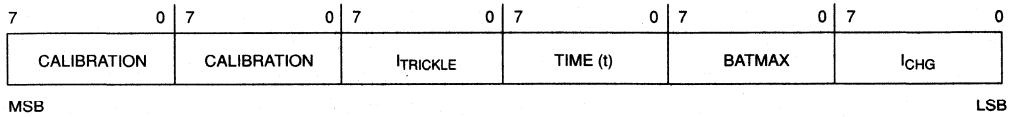
$$t_{MAX}(n) = 2(n + 1); \text{ for } 0 \leq n \leq 15$$

$I_{TRICKLE}$ [REGISTER 3]

This register contains the value of the trickle charge current. The current is expressed in the same manner as for the standard charge current.

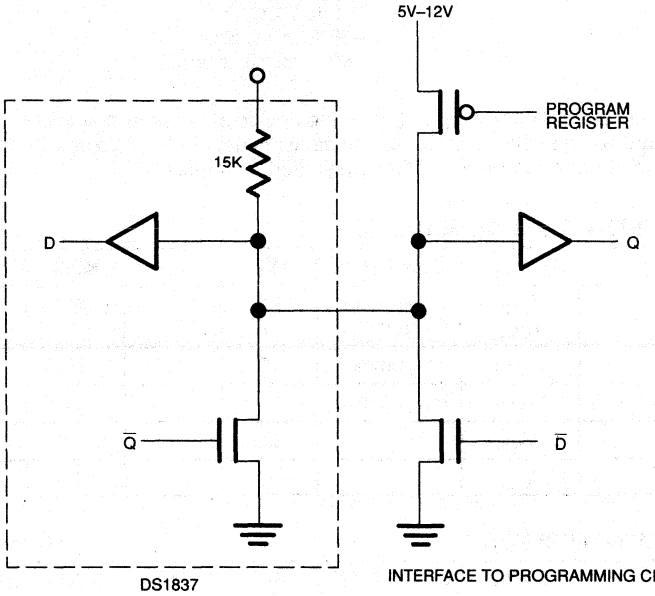
PROGRAMMING OPERATION

The data for the four registers described above is stored in nonvolatile EPROM memory and can be written only once. The four registers are part of a 48–bit shift register. The additional 16 bits are for factory calibration of the part and cannot be overwritten by the user. Zeros should be shifted into the part in these positions by the user. The bit order is as follows:



To enter the program/read mode, V_{CC} must be taken to 17V for a minimum of 1 ms and returned to <12V. The V_{BAT} pin is now configured to operate as a single wire I/O line. The hardware interface is shown in Figure 2.

HARDWARE INTERFACE FOR PROGRAMMING Figure 2



RESET TIMING

To issue a reset to the device the V_{BAT} pin must be brought low and held low for a minimum of 480 ms after which it is released and will return to a high level through the internal pull–up resistor. After the line is allowed to return high it must not be pulled low for at least 1 ms. Refer to the timing diagrams.

WRITE TIMING

A logic 0 is written by bringing the V_{BAT} pin low for at least 60 µs, but not more than 120 µs. A logic 1 is written by bringing the V_{BAT} pin low for at least 1 µs, but not more than 15 µs. After the line is allowed to return high it must not be pulled low for at least 60 µs.

READ TIMING

A read is performed by bringing the V_{BAT} pin low for at least 1 µs, but not more than 5 µs and then releasing it. A logic 1 is indicated by the pin returning high. The state of the V_{BAT} pin should be sampled at most 15 µs after V_{BAT} is pulled low. A high level indicates a read '1', a low level indicates a read '0'.

PROGRAMMING

To program the DS1837 the single line I/O must be enabled by bringing V_{CC} to 17V for at least 1 ms and then back to ≤12V. The register data may now be written. The register data must be preceded by an I/O reset followed by writing '011', LSB first. The register data can now be entered according to the write cycle timing detailed above, and is written LSB first. To commit data to the nonvolatile memory, an I/O reset, followed by writing '101' is entered. Next V_{BAT} is brought to 12V with V_{CC} at 8V for at least 10 ms. When the part has been programmed, the DS1837 disables the serial interface and will begin normal operation once power is cycled.

VERIFICATION

To verify the data contained in the registers after programming and powering down the part, the single line I/O must be enabled by bringing V_{CC} to 17V for at least 1 ms. A read cycle is preceded by '110', entered LSB first, after which the device will output the contents of the programming register. All 48 bits may be read, but reading may be terminated after the 32 user bits have been read. After verification, power must be cycled in order to return to normal operation.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to V_{CC}+0.7V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC1} V_{CC2}	Operation Programming	5.8 17	 17	13.2 18	V	1
Supply Voltage, V_{BAT}	V_{BATP}	Programming	12	12	13	V	
Supply Current, V_{BAT} pin	I_{BATP}	Programming			100	µA	
Logic 1	V_{IH}		2.2		V_{CC}+0.3	V	
Logic 0	V_{IL}		–0.3		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=12V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Current, Operation Mode	I_{CC}	Operation Programming			5 10	mA	
Battery Voltage	V_{BAT}	Charging	0		9.6	V	
V_{BAT} Leakage Current with V_{CC} at 0V	I_{BAT}				100	nA	
Pullup Resistance on I/O	R_{PU}			15		KΩ	
Charge Current	I_O		10		750	mA	
Charge Current Accuracy					±10	%	
Timer Value	T_{MAX}		1.7		36.8	hours	

AC ELECTRICAL CHARACTERISTICS: 1–WIRE INTERFACE

(0°C to 70°C; V_{CC}=12V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Active	t_{RSTL}	480		960	µs	
Logic 0 Active Low	t_0	60		120	µs	
Logic 1 Active Low	t_1	1		15	µs	
Time Slot	t_{TS}	60		120	µs	
Read Enable Time	t_{READ}	1		5	µs	
Time from Read Enable to I/O Line Sampling	t_{SAMPLE}			15	µs	
Recovery Time	t_{REC}	1			µs	
Program Mode Enable Pulse	t_{PE}	1			ms	
EPROM Write Cycle Time	t_{EW}	10		50	ms	

AC ELECTRICAL CHARACTERISTICS

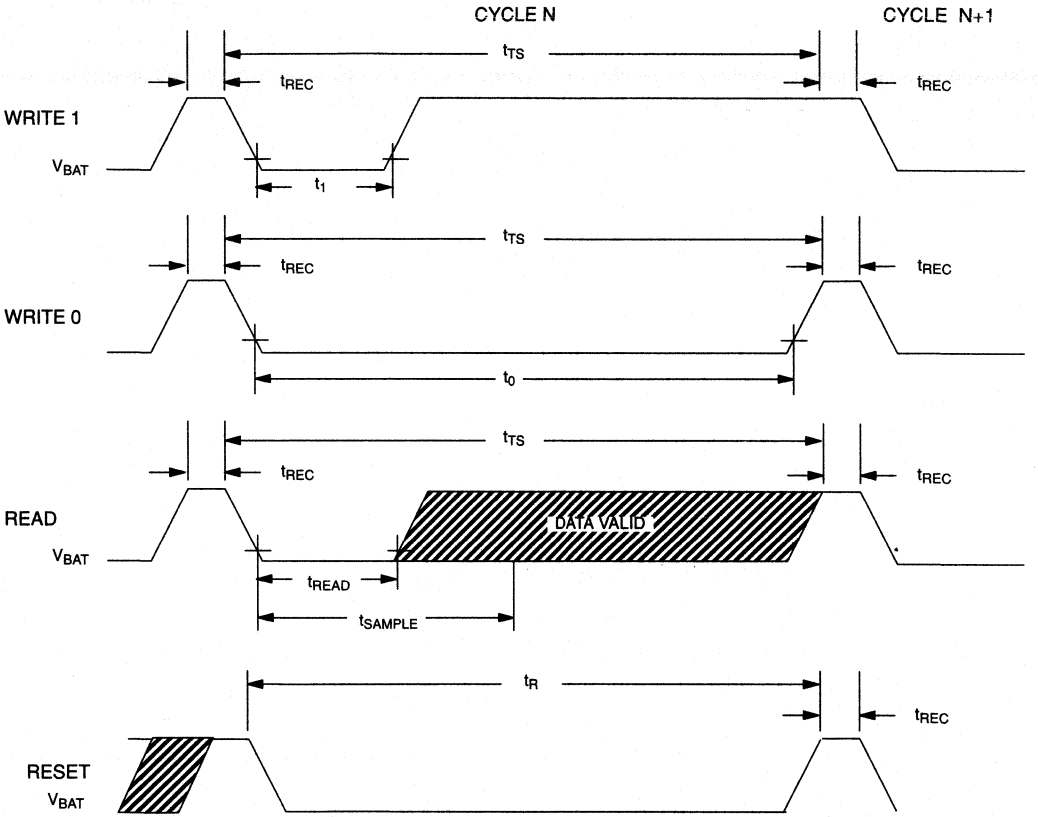
(0°C to 70°C; V_{CC}=12V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Accuracy	t_Q		±10	±15	%	

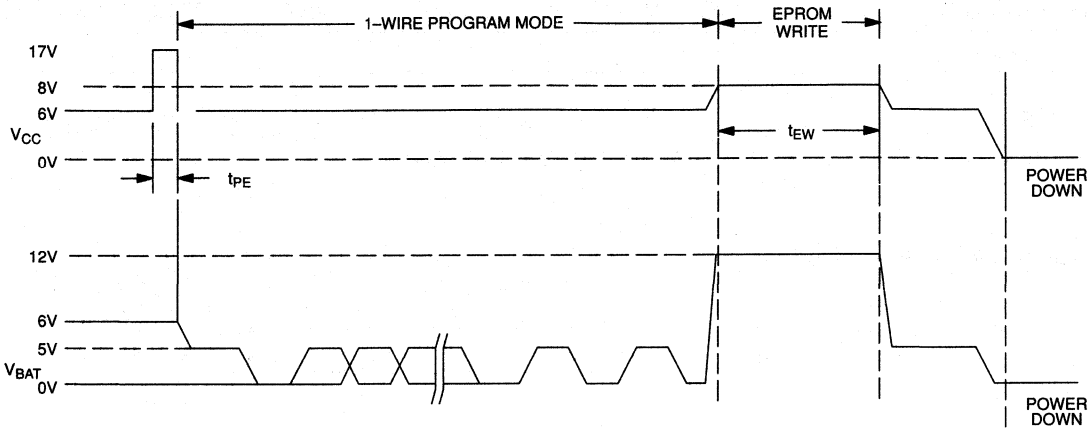
NOTE:

1. V_{CC1} must be at least 1V greater than desired battery voltage (V_{BAT}).

I/O SIGNAL TIMING Figure 4



PROGRAM MODE TIMING



DALLAS SEMICONDUCTOR

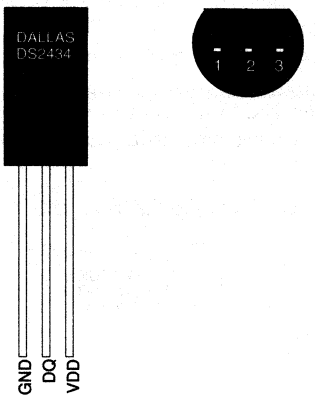
DS2434
Battery Identification Chip

FEATURES

- Provides unique ID number to battery packs
- Eliminates thermistors by sensing battery temperature on–chip
- 256–bit nonvolatile user memory available for storage of user data such as gas gauge and manufacturing information.
- Operating range of –40°C to +85°C
- Applications include portable computers, portable/cellular phones, consumer electronics, and handheld instrumentation.

PACKAGE OUTLINE

PR–35 PACKAGE



PIN DESCRIPTION

GND	–	Ground
DQ	–	Data In/Out
V_{DD}	–	Supply Voltage

DESCRIPTION

The DS2434 Battery Identification Chip provides a convenient method of tagging and identifying battery packs by manufacturer, chemistry, or other identifying parameters. The DS2434 allows the battery pack to be coded with a unique identification number, and also store information regarding the battery life and charge/discharge characteristics in its nonvolatile memory.

The DS2434 also performs the essential function of monitoring battery temperature, without the need for a thermistor in the battery pack.

Information is sent to/from the DS2434 over a 1–wire interface, so that battery packs need only have three output connectors; power, ground, and the 1–wire interface.

DETAILED PIN DESCRIPTION

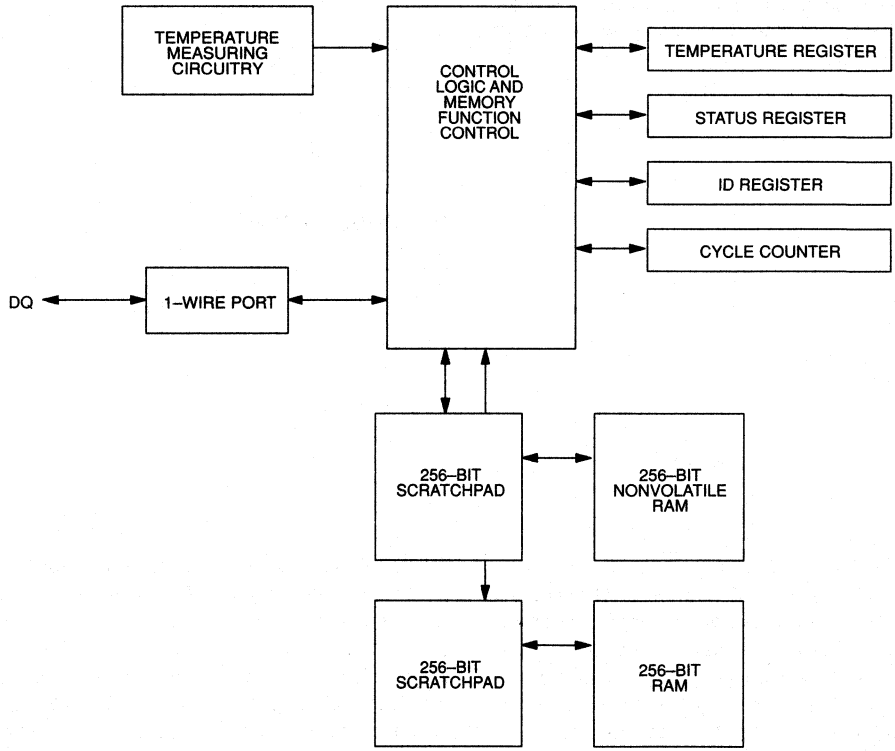
PIN	SYMBOL	DESCRIPTION
1	GND	**Ground pin.**
2	DQ	**Data Input/Output pin** for 1–wire communication port.
3	V_{DD}	**Supply pin** – input power supply.

OVERVIEW

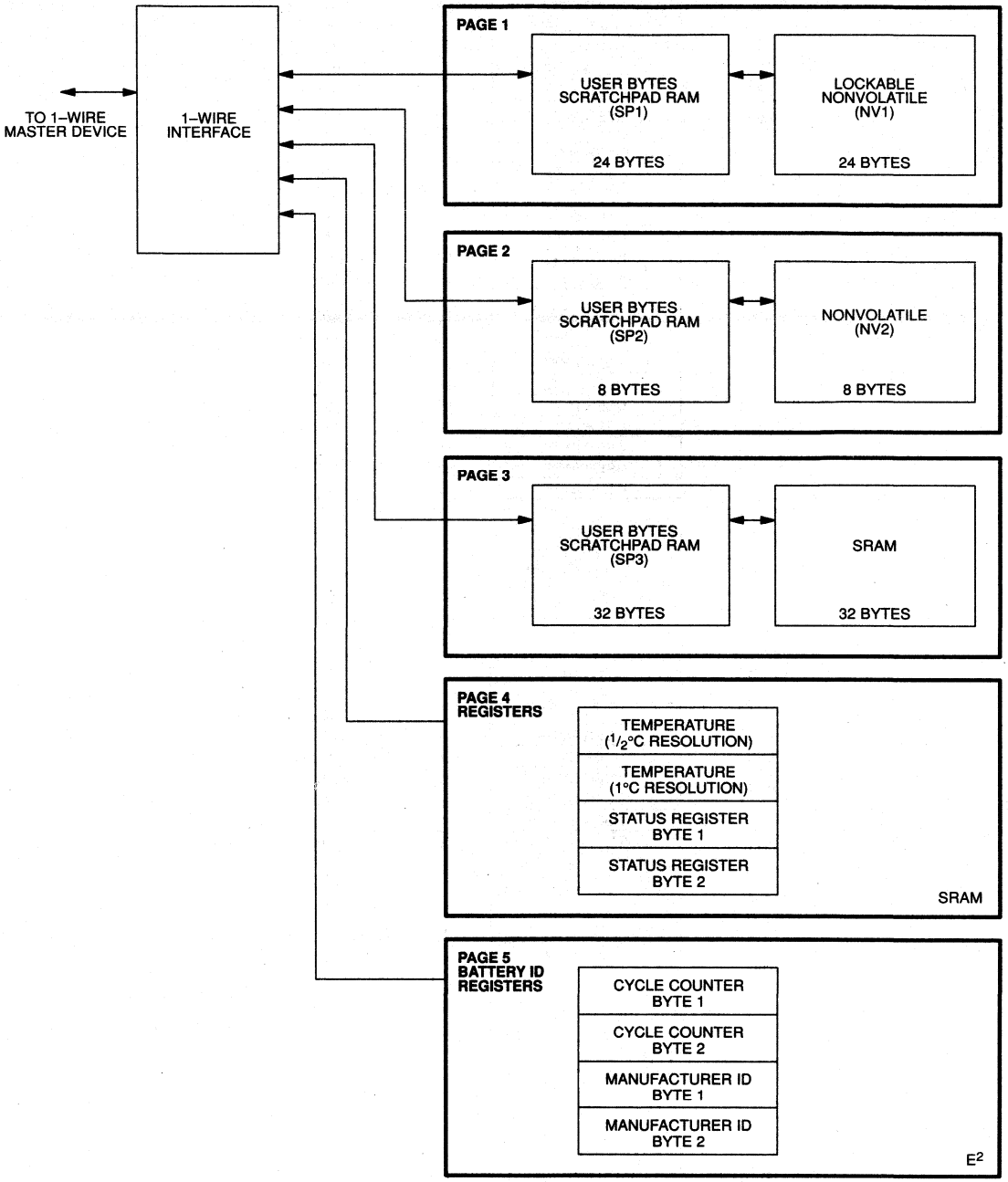
The DS2434 has five major components: 1) Scratchpad Memory, 2) Nonvolatile Memory, 3) On–board SRAM, 4) Temperature Sensor, and 5) ID Register. All data is read and written least significant bit first.

Access to the DS2434 is over a 1–wire interface. Charging parameters and other data such as battery chemistry, gas gauge information, and other user data would be stored in the DS2434, allowing this information to be permanently stored in the battery pack. Nonvolatile (E^2) RAM holds information even if the battery goes dead; as long as the battery remains within typical charge/discharge operating range, the SRAM provides battery–backed storage of information.

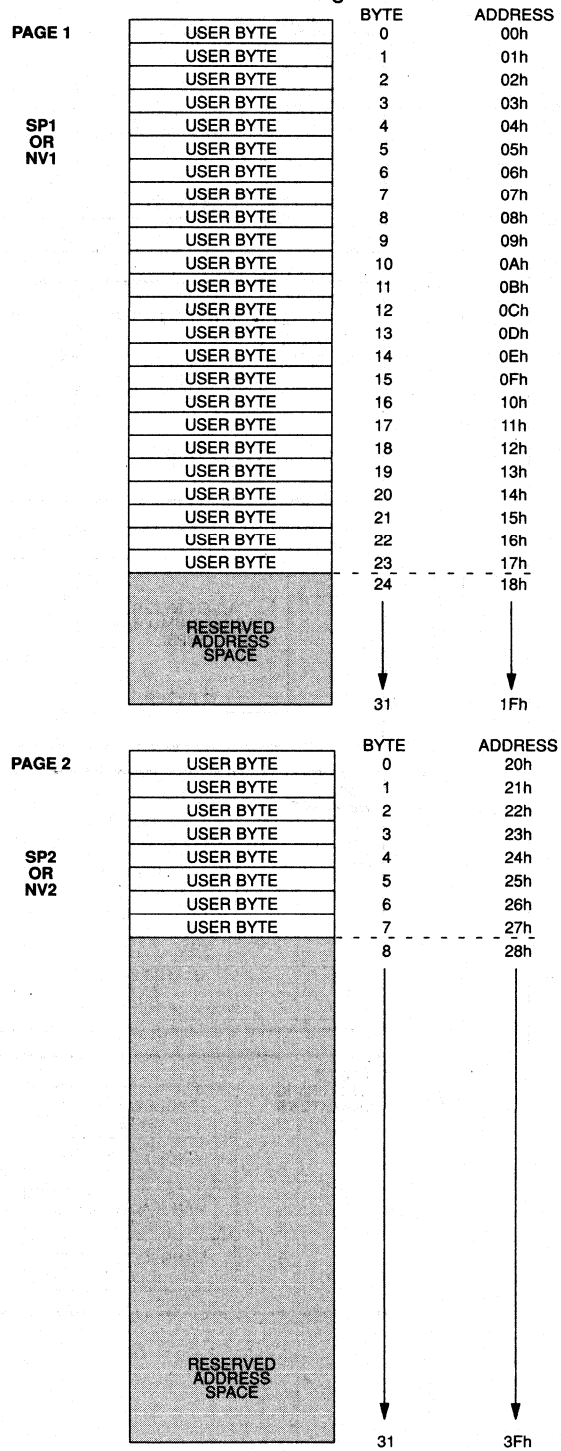
DS2434 BLOCK DIAGRAM Figure 1



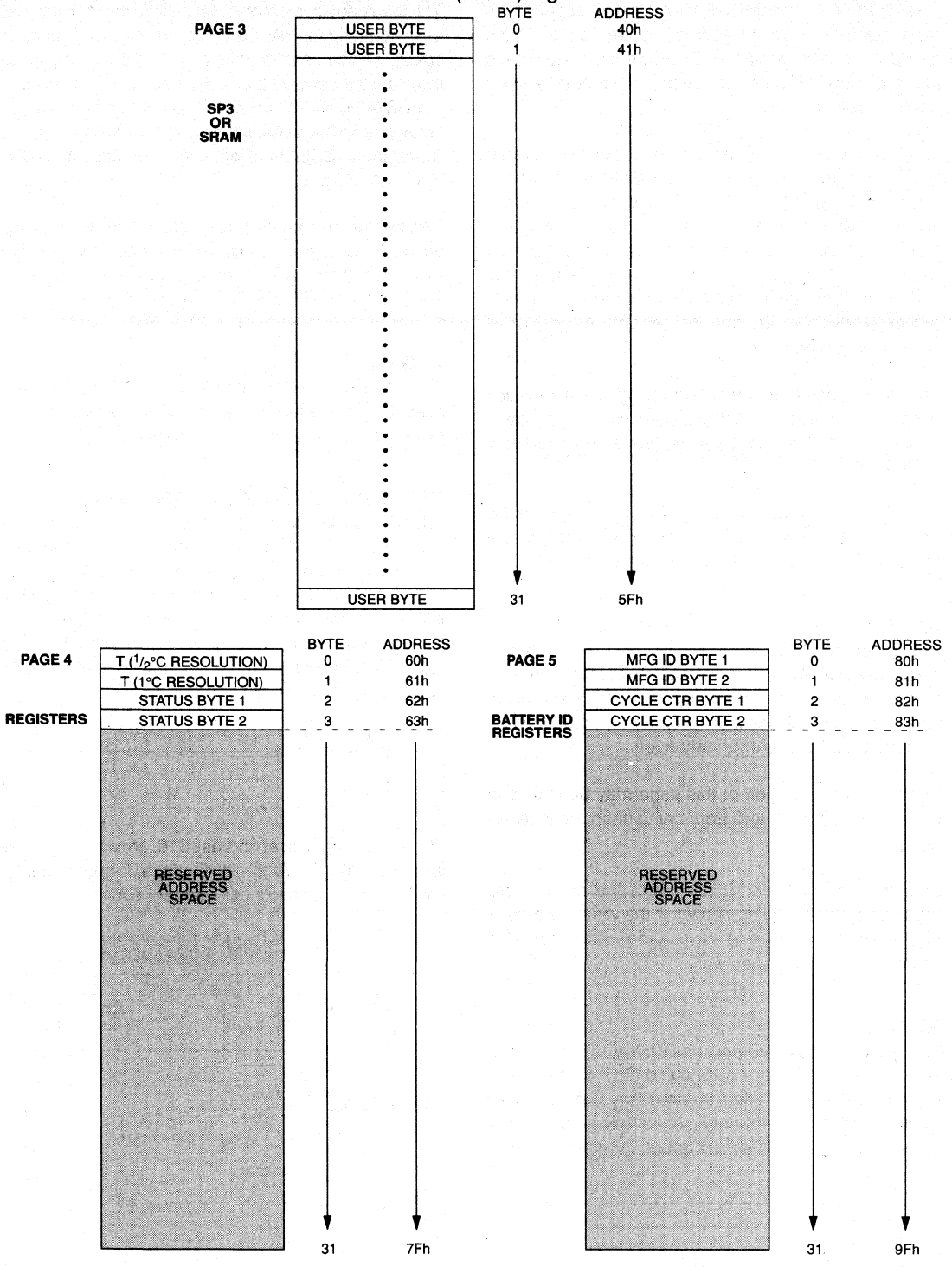
DS2434 MEMORY PARTITIONING Figure 2



DS2434 ADDRESSABLE RAM MEMORY MAP Figure 3



DS2434 ADDRESSABLE RAM MEMORY MAP (cont'd) Figure 3



MEMORY

The DS2434's memory is divided into five pages, each page filling 32 bytes of address space. Not all of the available addresses are used, however. Refer to the memory map of Figure 3 to see actual addresses which are available for use.

The first three pages of memory consist of a scratchpad RAM and then either a nonvolatile RAM (pages 1 and 2) or SRAM (page 3). The scratchpads help insure data integrity when communicating over the 1–wire bus. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command will transfer the data to the RAM (NV or SRAM). This process insures data integrity when modifying the memory.

The fourth page of memory consists of registers which contain the measured temperature value and status registers for the device; these registers are made from SRAM cells.

The fifth page of memory holds the ID number for the device and the cycle count registers in E^2 RAM, making these registers nonvolatile under all power conditions.

PAGE 1

The first page of memory has 24 bytes. It consists of a scratchpad RAM and a nonvolatile (E^2) RAM. These 24 bytes may be used to store any data the user wishes; such as battery chemistry descriptors, manufacturing lot codes, gas gauge information, etc.

The nonvolatile portion of this page may be locked to prevent data stored here from being changed inadvertantly.

Both the nonvolatile and the scratchpad portions are organized identically, as shown in the memory map of Figure 3. In this page, these two portions are referred to as NV1 and SP1, respectively.

PAGE 2

The second page of memory has 8 bytes. It consists of a scratchpad RAM and a nonvolatile (E^2) RAM. These eight bytes may be used to store any data the user wishes, such as battery chemistry descriptors, manufacturing lot codes, gas gauge information, etc.

PAGE 3

The third page of memory has a full 32 bytes. It consists of a scratchpad RAM and an SRAM. This address space may be used to store any data the user wishes, provided that, should the battery go dead and power to the DS2434 is lost, this data may also be lost without serious repercussions. Data which must remain even if power to the DS2434 is lost should be placed in either Page 1 or Page 2.

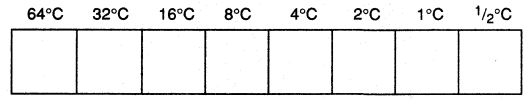
This section of memory may be used to store gas gauge and self discharge information. If the battery dies, and this information is lost, it is moot because the user can easily determine that the battery is dead.

PAGE 4

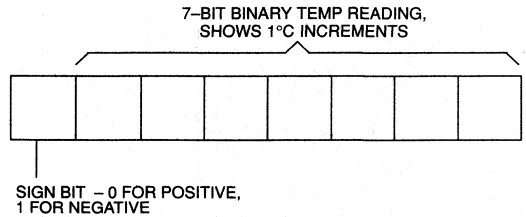
The fourth page of memory is used by the DS2434 to store the converted value of battery temperature. A two–byte status register is also provided.

TEMPERATURE REGISTERS (60h–61h)

The DS2434 can measure temperature without external components. The resulting temperature measurement is placed into two temperature registers. These registers are SRAM, and therefore will hold the values placed in them until the battery voltage falls below the minimum V_{DD} specified. The first register, at address 60h, provides $^1/_2$°C resolution for temperatures between 0°C and 127 $^1/_2$°C, formatted as follows:



The second register, at address 61h, provides 1°C resolution over the –40°C to +85°C range, formatted as follows in the binary two's complement coding.



STATUS/CONTROL REGISTER (62h–63h)

The status register is a two byte register at addresses 62h and 63h (consisting of SRAM). Address 62h is the least significant byte of the status register, and is currently the only address with defined status bits; the other byte at address 63h is reserved for future use. The status register is formatted as follows:

STATUS REGISTER

							LSB	
X	X	X	X	X	LOCK	NVB	TB	62h
X	X	X	X	X	X	X	X	63h

where

X = Don't Care

TB = Temperature Busy flag. "1" = temperature conversion in progress; "0" = temperature conversion complete, valid data in temperature register.

NVB = Nonvolatile memory busy flag. "1" = Copy from scratchpad to NVRAM in progress, "0" = nonvolatile memory is not busy. A copy to NVRAM may take from 2 ms to 10 ms (taking longer at lower supply voltages).

LOCK = NV1 Locked flag. "1" indicates that NV1 is locked; "0" indicates that NV1 is unlocked.

CYCLE COUNTER

MSB BYTE 2

32768	16384	8192	4096	2048	1024	512	256

83h

BYTE 1 LSB

128	64	32	16	8	4	2	0

82h

PAGE 5

The fifth page of memory holds the battery manufacturer ID number as well as a two–byte counter for counting the number of battery charge/discharge cycles.

ID REGISTER (80h and 81h)

The ID Register is a 16–bit ROM register that can contain a unique identification code, if purchased from Dallas Semiconductor. This ID number is programmed by Dallas Semiconductor, is unchangeable, and is unique to each customer. This ID number may be used to assure that batteries containing a DS2434 have the same manufacturer ID number as a charger configured to operate with that battery pack. This feature may be used to prevent charging of batteries for which the charging circuit has not been designed.

CYCLE COUNTER (82h and 83h)

The cycle counter register gives an indication of the number of charge/discharge cycles the battery pack has been through. This nonvolatile (E^2) register is incremented by the user through the use of a protocol to the DS2434, and is reset by another protocol. The counter is a straight binary counter, formatted as follows:

MEMORY FUNCTION COMMANDS

The protocols necessary for accessing the DS2434 are described in this section. Only these protocols may be written to the DS2434. Writing other protocols to the device may result in permanent damage to the part. These are summarized in Table 1, and examples of memory functions are provided in Tables 2 and 3.

PAGE 1 THROUGH PAGE 3 COMMANDS

Read Scratchpad [11h]

This command reads the contents of the scratchpad RAM on the DS2434. This command is followed by a start byte address. After issuing this command and providing the start address, the user may begin reading the data. The user may read data through the end of the scratchpad space (address 5Fh), with any reserved data bits reading all logic 1's and after which the data read will be all logic 1's.

Write Scratchpad [17h]

This command writes to the scratchpad RAM on the DS2434. This command is followed by a start byte address. After issuing this command and providing the start address, the user may begin writing data to the DS2434 scratchpad at the starting byte address.

Copy SP1 to NV1 [22h]
This command copies the entire contents (24 bytes) of Scratchpad 1 (SP1) to its corresponding nonvolatile memory (NV1). The nonvolatile RAM memory of the DS2434 cannot be written to directly by the bus master; however, the scratchpad RAM may be copied to the nonvolatile RAM. This prevents accidental overwriting of the nonvolatile RAM, and allows the data to be written first to the scratchpad, where it can be read back and verified before copying to the nonvolatile RAM. This command does not use a start address; the entire contents of the scratchpad will be copied to the nonvolatile RAM. The NVB bit will be set when the copy is in progress. NV1 is made with E^2 type memory cells that will accept at least 50000 changes.

Copy SP2 to NV2 [25h]
This command copies the entire contents (8 bytes) of SP2 (user bytes) to its corresponding nonvolatile memory (NV2). This command does not use a start address; the entire contents of SP2 will be copied to NV2. The NVB bit will be set when the copy is in progress. NV2 is made with E^2 type memory cells that will accept at least 50000 changes.

Copy SP3 to SRAM [28h]
This command copies the entire contents (32 bytes) of SP3 to its corresponding SRAM. This command does not use a start address; the entire contents of SP3 will be copied to the SRAM.

Copy NV1 to SP1 [71h]
This command copies the entire contents (24 bytes) of NV1 to its corresponding scratchpad RAM (SP1). This command does not use a start address; the entire contents of NV1 will be copied to SP1. The nonvolatile RAM memory of the DS2434 cannot be read directly by the bus master; however, the nonvolatile RAM may be copied to the scratchpad RAM.

Copy NV2 to SP2 [77h]
This command copies the entire contents (8 bytes) of NV2 (user bytes) to its corresponding scratchpad RAM (SP2). This command does not use a start address; the entire contents of NV2 will be copied to SP2. The nonvolatile RAM memory of the DS2434 cannot be read directly by the bus master; however, the nonvolatile RAM may be copied to the scratchpad RAM.

Copy SRAM to SP3 [7Ah]
This command copies the entire contents (32 bytes) of SRAM to its corresponding scratchpad RAM (SP3). This command does not use a start address; the entire contents of SRAM will be copied to SP3.The SRAM memory of the DS2434 cannot be read directly by the bus master; however, the SRAM may be copied to the scratchpad RAM.

Lock NV1 [43h]
This command prevents copying SP1 to NV1. This is done as an added measure of data security, preventing data from being changed inadvertently. NV1 may be copied up into SP1 while the part is locked. This allows NV1 to be read at any time. However, NV1 cannot be written to through a Copy SP1 to NV1 command without first unlocking the DS2434.

Unlock NV1 [44h]
This command unlocks NV1, to allow copying SP1 into NV1. This is done as an added measure of data security, preventing data from being changed inadvertently.

PAGE 4 AND 5 COMMANDS

Convert T [D2h]
This command instructs the DS2434 to initiate a temperature conversion cycle. This sets the TB flag. When the temperature conversion is done, the TB flag is reset and the current temperature value is placed in the temperature register. While a temperature conversion is taking place, all other memory functions are still available for use.

Read Registers [B2h]
This command reads the contents of the registers in Page 4 and 5. This command is followed by a start byte address. After issuing this command and providing the start address, the user may begin reading the data. The user may read data through the end of the register space (through address 63h in Page 4, address 83h in Page 5), after which the data read will be all logic 1's.

Increment Cycle [B5h]
This command increments the value in the cycle counter register. This command does not use a start address; no further data is required.

Reset Cycle Counter [B8h]
This command is used to reset the cycle counter register to zero, if desired.

DS2434 COMMAND SET Table 1

INSTRUCTION	DESCRIPTION	PROTOCOL	1–WIRE BUS MASTER STATUS AFTER ISSUING PROTOCOL	1–WIRE BUS DATA AFTER ISSUING PROTOCOL
PAGE 1 through PAGE 3 Memory Commands				
Read Scratchpad	Reads bytes from DS2434 Scratchpad.	11h <addr (00h–5Fh)>	RX	<read data>
Write Scratchpad	Writes bytes to DS2434 Scratchpad.	17h <addr 00h–5Fh)>	TX	<write data>
Copy SP1 to NV1	Copies entire contents of SP1 to NV1.	22h	Idle	{NVB bit in Status Register=1 until copy complete (10ms, typ)}
Copy SP2 to NV2	Copies entire contents of SP2 to NV2.	25h	Idle	{NVB bit in Status Register=1 until copy complete (10ms, typ)}
Copy SP3 to SRAM	Copies entire contents of SP3 to SRAM.	28h	Idle	Idle
Copy NV1 to SP1	Copies entire contents of NV1 to SP1.	71h	Idle	Idle
Copy NV2 to SP2	Copies entire contents of NV2 to SP2.	77h	Idle	Idle
Copy SRAM to SP3	Copies entire contents of SRAM to SP3.	7Ah	Idle	Idle
Lock NV1	Locks 24 bytes of SP1 and NV1 from reading and writing.	43h	Idle	{NVB bit in Status Register=1 until copy complete (10ms, typ)}
Unlock NV1	Unlocks 24 bytes of SP1 and NV1 for reading and writing.	44h	Idle	{NVB bit in Status Register=1 until copy complete (10ms, typ)}
PAGE 4 and PAGE 5 Register Commands				
Read Registers	Reads bytes from Temperature, Status and ID Registers.	B2h <addr (60h–63h, 80h–83h)>	RX	<read data>
Reset Cycle Counter	Resets cycle counter registers to zero.	B8h	Idle	{NVB bit in Status Register=1 until copy complete (10ms, typ)}
Increment Cycle Counter	Increments the value in the cycle counter register.	B5h	Idle	{NVB bit in Status Register=1 until copy complete (10ms, typ)}
Convert T	Initiates temperature conversion.	D2h	Idle	{TB bit in Status Register=1 until conversion complete}

MEMORY FUNCTION EXAMPLE Table 2

Example: Bus Master writes 24 bytes of data to DS2434 scratchpad, then copies to it to NV1.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480–960 µs)
RX	Presence	Presence pulse
TX	17h	Issue "write scratchpad" command
TX	00h	Start address
TX	<24 bytes>	Write 24 bytes of data to scratchpad
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	11h	Issue "read scratchpad" command
TX	00h	Start address
RX	<24 data bytes>	Read scratchpad data and verify
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	22h	Issue "copy SP1 to NV1" command
RX	<busy indicator>	Wait until NVB in status register=0 (10 ms typical)
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

MEMORY FUNCTION EXAMPLE Table 3

Example: Bus Master initiates temperature conversion, then reads temperature.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480–960 µs)
RX	Presence	Presence pulse
TX	D2h	Issue "convert T" command
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	B2h	Issue "read registers" command; begin loop
TX	62h	Status register address
RX	<1 data byte>	Read status register and loop until TB=0
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	B2h	Issue "read registers" command
TX	61h	Temperature register address
RX	<1 data byte>	Read temperature register
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

1–WIRE BUS SYSTEM

The DS2434 1–wire bus is a system which has a single bus master and one slave. The DS2434 behaves as a slave. The DS2434 is not able to be multidropped, unlike other 1–wire devices from Dallas Semiconductor.

The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1–wire signaling (signal types and timing).

HARDWARE CONFIGURATION

The 1–wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1–wire bus must have open drain or 3–state outputs. The 1–wire port of the DS2434 is open drain with an internal circuit equivalent to that shown in Figure 5. The 1–wire bus requires a pull–up resistor of approximately 5KΩ.

The idle state for the 1–wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 480 µs, all components on the bus will be reset.

TRANSACTION SEQUENCE

The protocol for accessing the DS2434 via the 1–wire port is as follows:

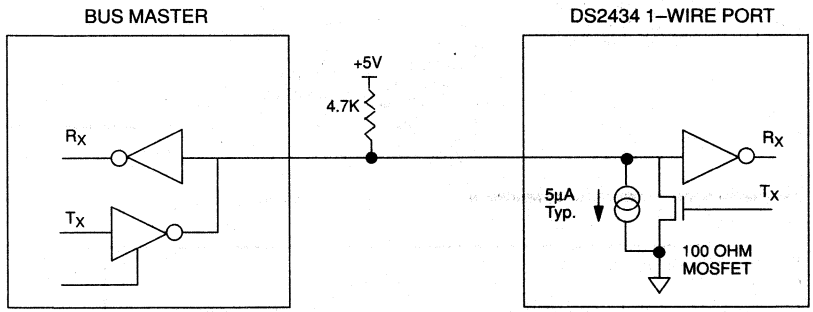
- Initialization
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1–wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS2434 is on the bus and is ready to operate. For more details, see the "1–Wire Signaling" section.

HARDWARE CONFIGURATION Figure 4



I/O SIGNALING

The DS2434 requires strict protocols to insure data integrity. The protocol consists of several types of signaling on one line: reset pulse, presence pulse, write 0, write 1, read 0, and read 1. All of these signals, with the exception of the presence pulse, are initiated by the bus master.

The initialization sequence required to begin any communication with the DS2434 is shown in Figure 5. A reset pulse followed by a presence pulse indicates the DS2434 is ready to send or receive data given the correct memory function command.

The bus master transmits (TX) a reset pulse (a low signal for a minimum of 480 µs). The bus master then releases the line and goes into a receive mode (RX). The 1–wire bus is pulled to a high state via the 5K pull–up resistor. After detecting the rising edge on the I/O pin, the DS2434 waits 15–60 µs and then transmits the presence pulse (a low signal for 60–240 µs).

READ/WRITE TIME SLOTS

DS2434 data is read and written through the use of time slots to manipulate bits and a command word to specify the transaction.

Write Time Slots

A write time slot is initiated when the host pulls the data line from a high logic level to a low logic level. There are two types of write time slots: Write One time slots and Write Zero time slots. All write time slots must be a minimum of 60 µs in duration with a minimum of a 1 µs recovery time between individual write cycles.

The DS2434 samples the I/O line in a window of 15 µs to 60 µs after the I/O line falls. If the line is high, a Write One occurs. If the line is low, a Write Zero occurs (see Figure 6).

For the host to generate a Write One time slot, the data line must be pulled to a logic low level and then released, allowing the data line to pull up to a high level within 15 µs after the start of the write time slot.

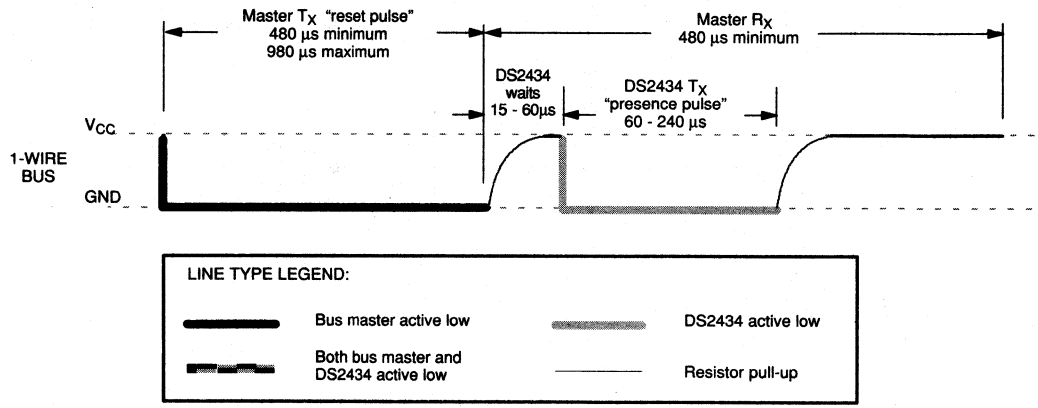
For the host to generate a Write Zero time slot, the data line must be pulled to a logic low level and remain low for the duration of the write time slot.

Read Time Slots

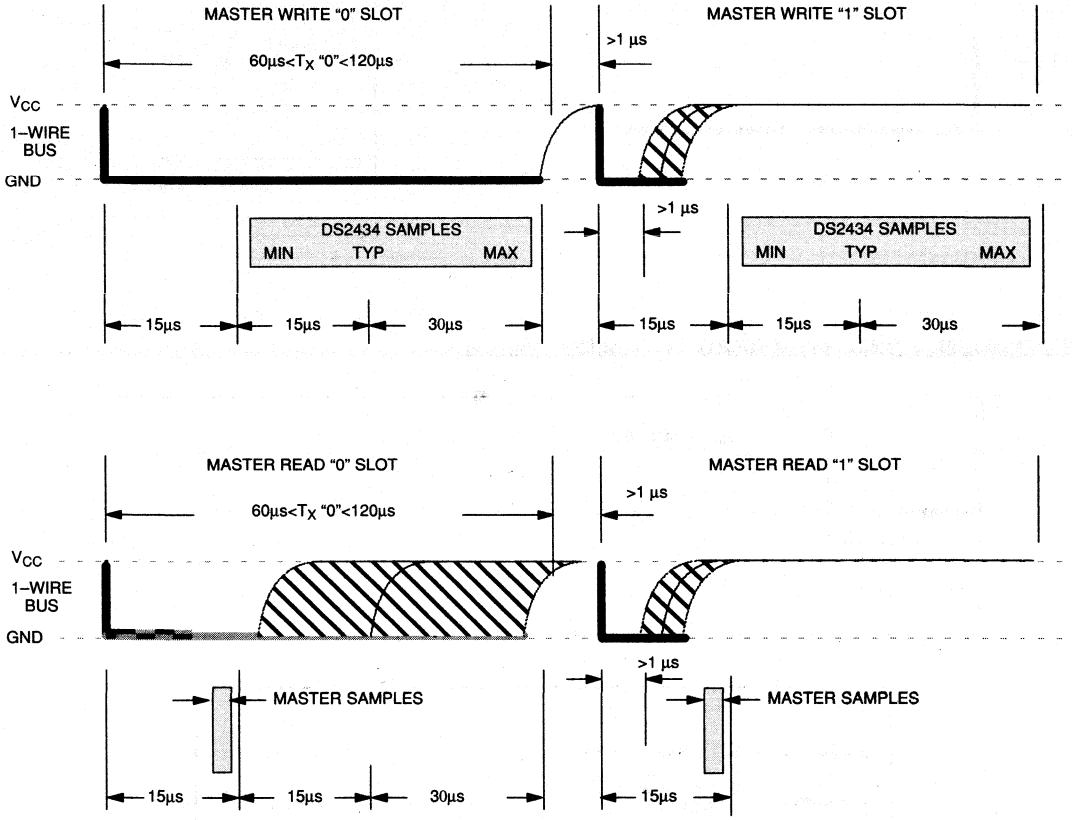
The host generates read time slots when data is to be read from the DS2434. A read time slot is initiated when the host pulls the data line from a logic high level to logic low level. The data line must remain at a low logic level for a minimum of 1 µs; output data from the DS2434 is then valid for the next 14 µs maximum. The host therefore must stop driving the I/O pin low in order to read its state 15 µs from the start of the read slot (see Figure 6). By the end of the read time slot, the I/O pin will pull back high via the external pull–up resistor. All read time slots must be a minimum of 60 µs in duration with a minimum of a 1 µs recovery time between individual read slots.

Figure 7 shows that the sum of T_{INIT}, T_{RC}, and T_{SAMPLE} must be less than 15 µs. Figure 9 shows that system timing margin is maximized by keeping T_{INIT} and T_{RC} as small as possible and by locating the master sample time towards the end of the 15 µs period.

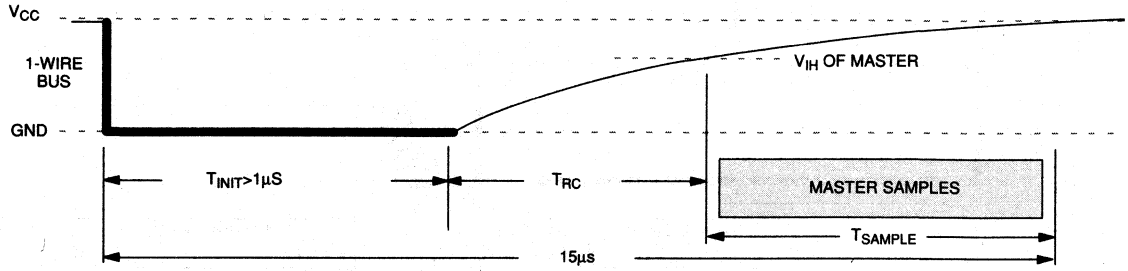
INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 5



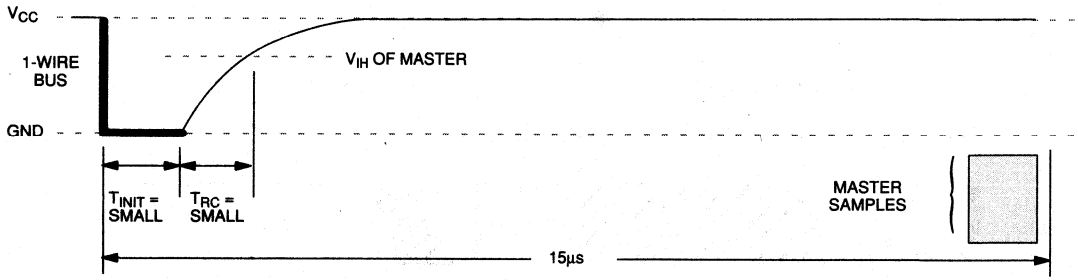
READ/WRITE TIMING DIAGRAM Figure 6

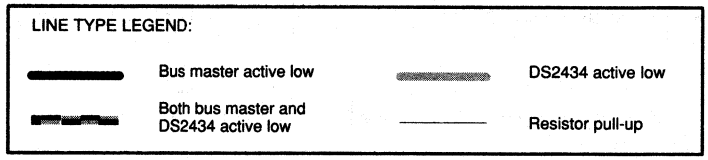


DETAILED MASTER READ "1" TIMING Figure 7



RECOMMENDED MASTER READ "1" TIMING Figure 8





ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	–40°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C; V_{DD}=3.6V to 6.4V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	I/O Functions	2.5		6.4	V	
		NV Copy Functions	2.7		6.4		
		±½°C Accurate Temp. Conversions	3.6		6.4		1
Data Pin	$V_{I/O}$		–0.3		V_{CC}+0.3	V	

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{DD}=3.6V to 6.4V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Temperature Accuracy (=T_{ACTUAL} – $T_{MEASURED}$)		T_A=0°C to 70°C			±½	°C	
		T_A=–40°C to 0°C and +70°C to +85°C			±1		
Input Logic High	V_{IH}		2.2		V_{CC}+0.3	V	
Input Logic Low	V_{IL}		–0.3		+0.8	V	
Sink Current	I_L	$V_{I/O}$=0.4V	–4.0			mA	
Standby Current	I_Q				1	µA	
Active Current	I_{DD}				1.5	mA	2
Input Resistance	R_I			500		KΩ	2

NOTES:

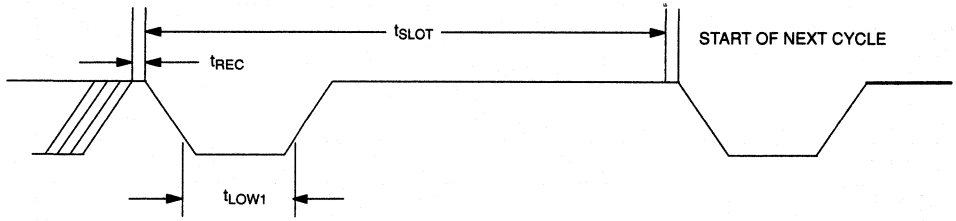
1. Temperature conversion will work with ±2°C accuracy down to V_{DD}=2.7V.
2. I/O line in "hi–Z" state and $I_{I/O}$=0.

AC ELECTRICAL CHARACTERISTICS: 1–WIRE INTERFACE

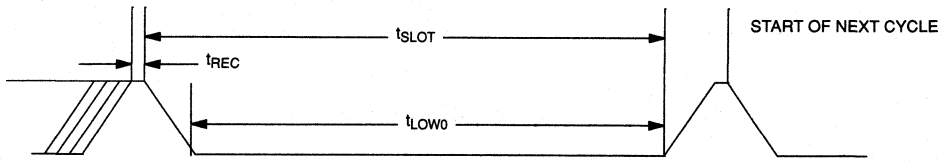
(–40°C to +85°C; V_{DD}=3.6V to 6.4V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Temperature Conversion Time	t_{CONV}		700	1000	ms	
Time Slot	t_{SLOT}	60		120	µs	
Recovery Time	t_{REC}	1			µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Read Data Valid	t_{RDV}			15	µs	
Reset Time High	t_{RSTH}	480			µs	
Reset Time Low	t_{RSTL}	480		960	µs	
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	
Capacitance	$C_{IN/OUT}$			25	pF	
NV Write Cycle	t_{WR}		10	50	ms	

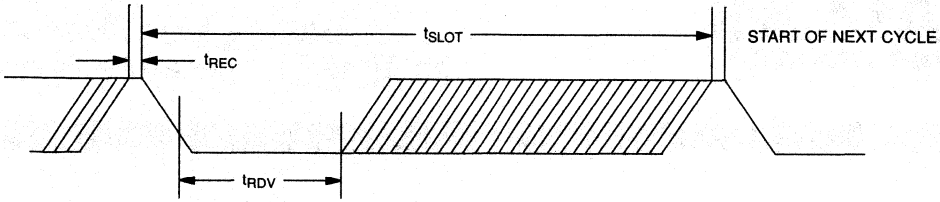
1–WIRE WRITE ONE TIME SLOT



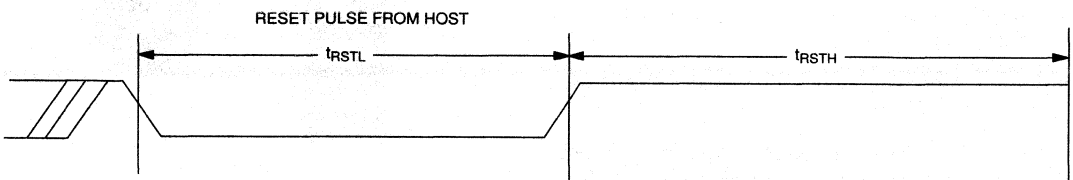
1–WIRE WRITE ZERO TIME SLOT



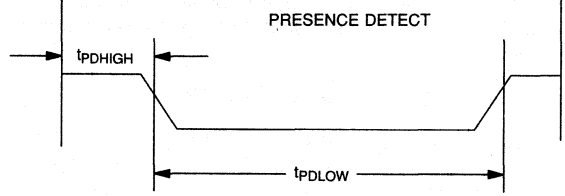
1-WIRE READ ZERO TIME SLOT



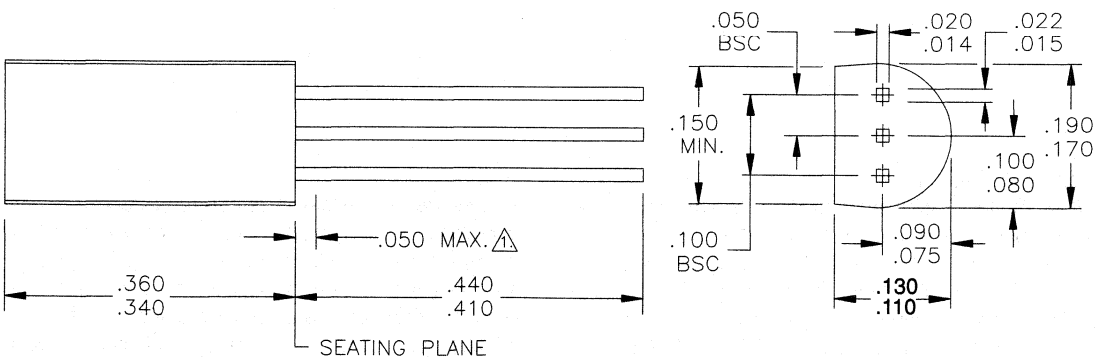
1-WIRE PRESENCE DETECT



1-WIRE RESET PULSE



PACKAGE DIAGRAM (PR–35)



PRELIMINARY

DALLAS SEMICONDUCTOR

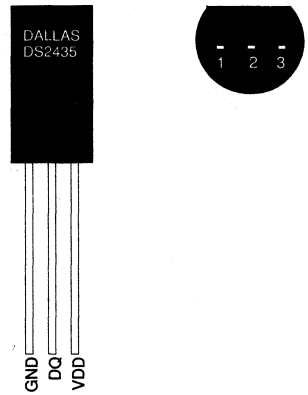
DS2435
Battery Identification Chip with Time/Temperature Histogram

FEATURES

- Provides unique ID number to battery packs
- Eliminates thermistors by sensing battery temperature on–chip
- Elapsed time counter provides indication of battery usage/storage time
- Time/Temperature histogram function provides essential information for determining battery self–discharge
- 256–bit nonvolatile user memory available for storage of user data such as gas gauge and manufacturing information.
- Operating range of –40°C to +85°C
- Applications include portable computers, portable/ cellular phones, consumer electronics, and hand held instrumentation.

PACKAGE OUTLINE

PR–35 PACKAGE



PIN DESCRIPTION

GND	–	Ground
DQ	–	Data In/Out
V_{DD}	–	Supply Voltage

DESCRIPTION

The DS2435 Battery Identification Chip provides a convenient method of tagging and identifying battery packs by manufacturer, chemistry, or other identifying parameters. The DS2435 allows the battery pack to be coded with a unique identification number, and also store information regarding the battery life and charge/discharge characteristics in its nonvolatile memory.

The DS2435 also performs the essential function of monitoring battery temperature, without the need for a thermistor in the battery pack. A time/temperature histogram function stores the amount of time that the battery has been in up to eight temperature bands, allowing more accurate self–discharge calculations to be carried out by the user for determining remaining battery capacity. In addition, the on–board elapsed time counter provides a method of determining the amount of time that a battery pack has been in storage, to allow more accurate self–discharge determination.

Information is sent to/from the DS2435 over a 1–wire interface, so that battery packs need only have three output connectors; power, ground, and the 1–wire interface.

DETAILED PIN DESCRIPTION

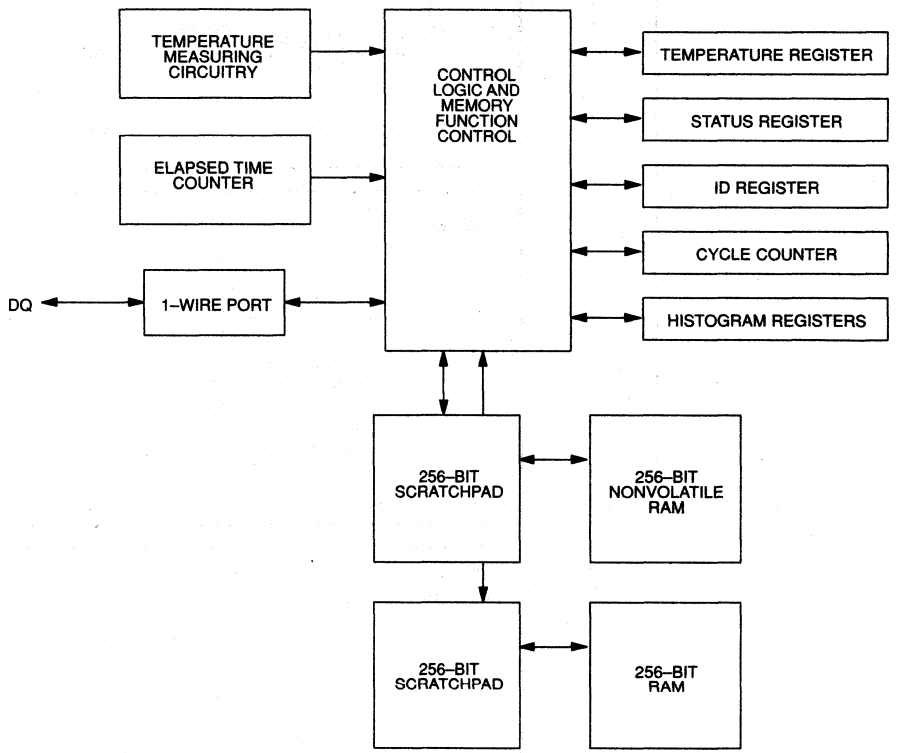
PIN	SYMBOL	DESCRIPTION
1	GND	**Ground pin.**
2	DQ	**Data Input/Output pin** for 1–wire communication port.
3	V_{DD}	**Supply pin** – input power supply.

OVERVIEW

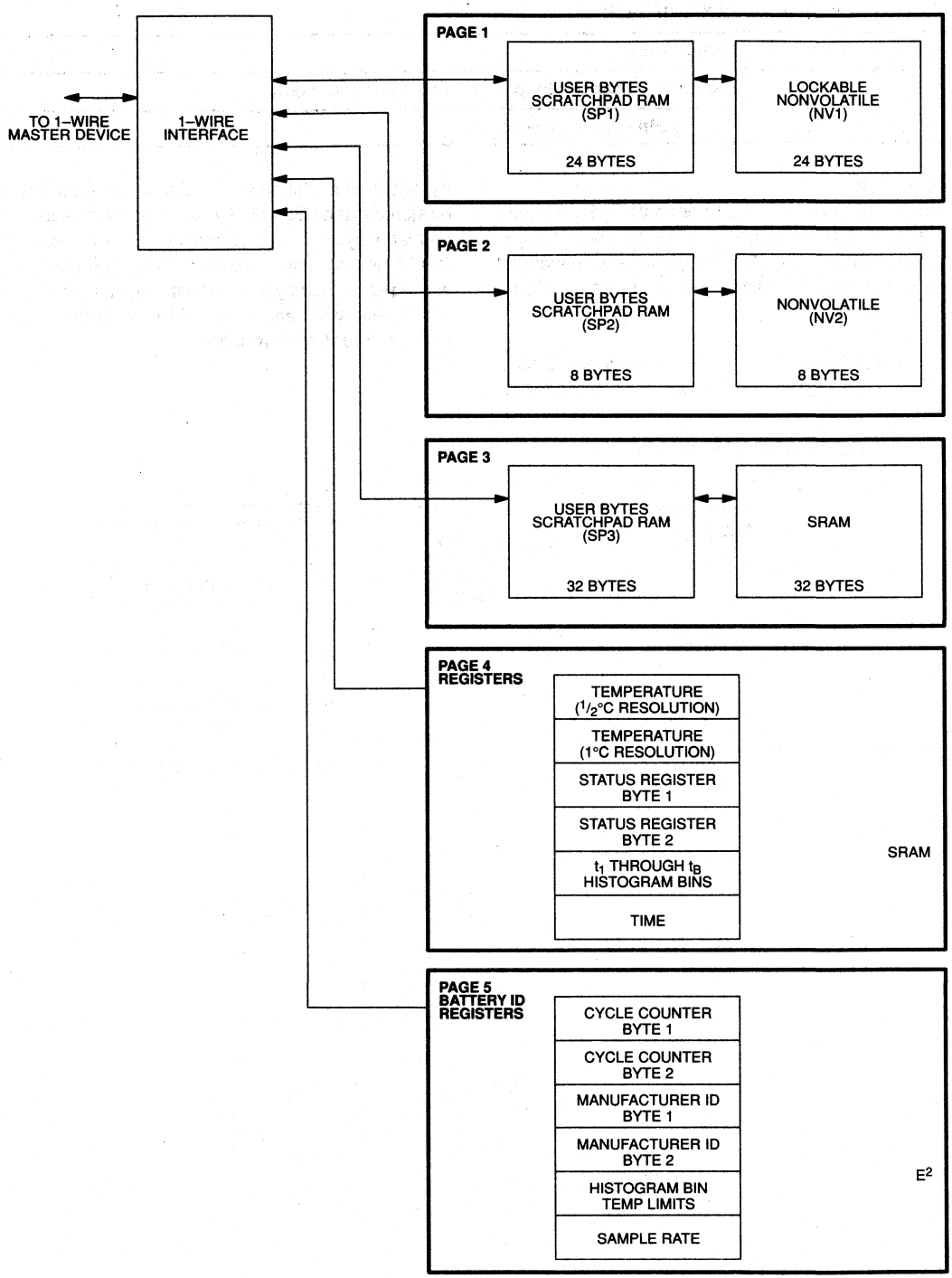
The DS2435 has six major components: 1) Scratchpad Memory, 2) Nonvolatile Memory, 3) On–board SRAM, 4) Temperature Sensor, 5) ID Register, and 6) elapsed time counter. All data is read and written least significant bit first.

Access to the DS2435 is over a 1–wire interface. Charging parameters and other data such as battery chemistry, gas gauge information, and other user data would be stored in the DS2435, allowing this information to be permanently stored in the battery pack. Nonvolatile (E^2) RAM holds information even if the battery goes dead; as long as the battery remains within typical charge/discharge operating range, the SRAM provides battery–backed storage of information.

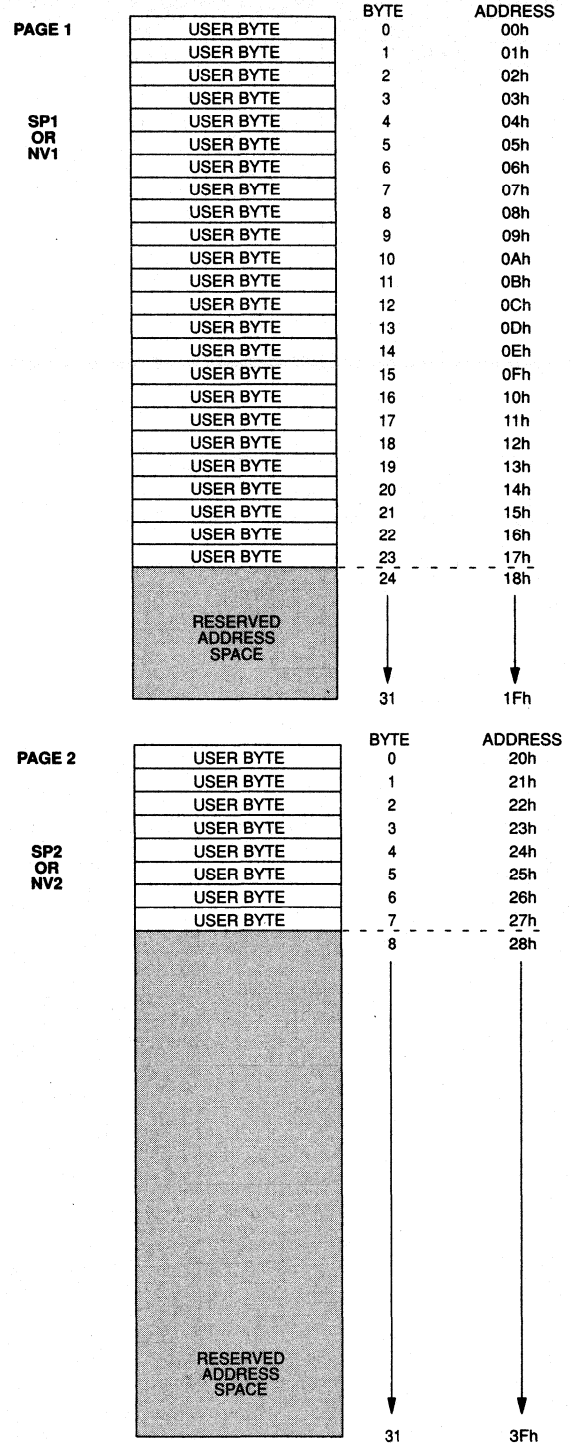
DS2435 BLOCK DIAGRAM Figure 1



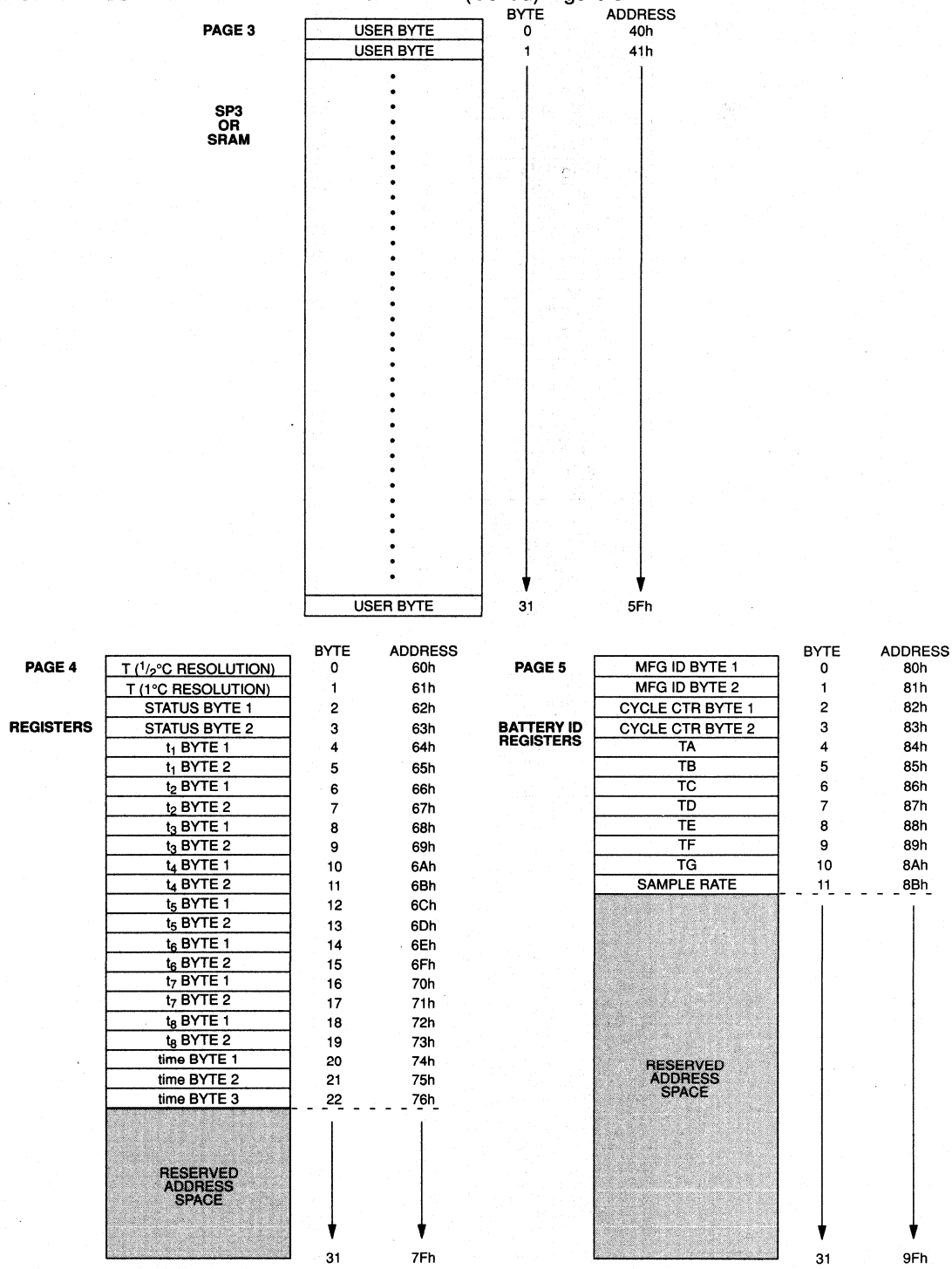
DS2435 MEMORY PARTITIONING Figure 2



DS2435 ADDRESSABLE RAM MEMORY MAP Figure 3



DS2435 ADDRESSABLE RAM MEMORY MAP (Cont'd) Figure 3



OVERVIEW – TIME/TEMPERATURE HISTOGRAM

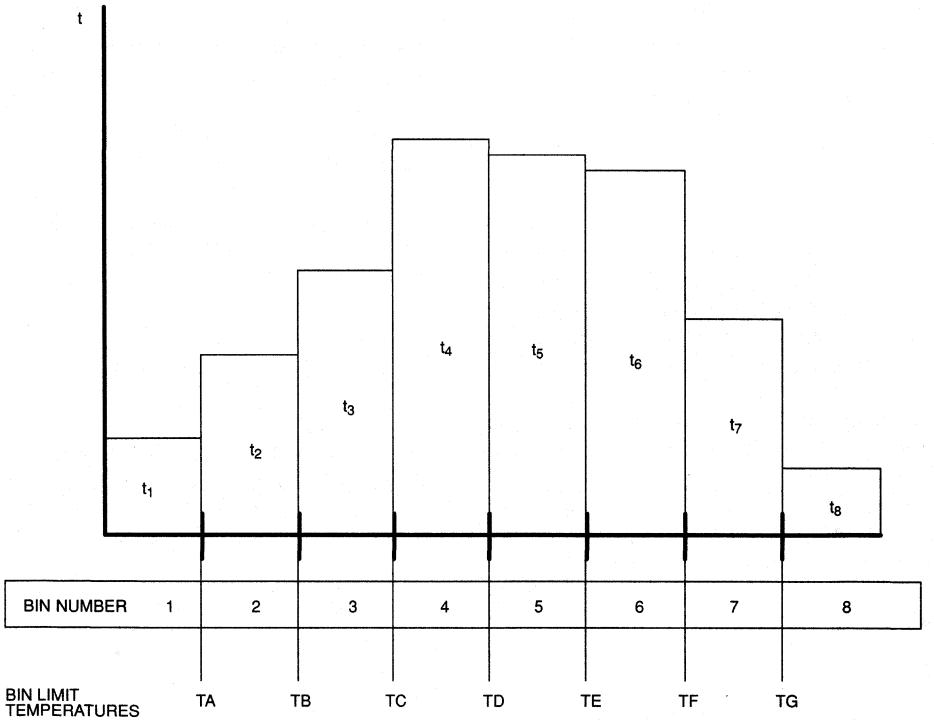
Periods of storage are normal for most battery applications. During this storage time, little or no current is actually drawn from the battery; however, batteries will lose capacity during this storage time due to parasitic side reactions in the cell, as well as other electrochemical mechanisms. This loss of capacity is termed self–discharge.

Since self–discharge is the result of electrochemical reactions, its rate is dependent upon the cell temperature. Knowing the time spent in certain temperature ranges during the storage time of the battery, these temperature effects may be factored into a calculation of self–discharge for the battery, thereby allowing a more accurate determination of retained battery capacity.

The DS2435 measures, tabulates and stores this information in the battery pack. The DS2435 periodically measures the battery temperature, and updates the appropriate temperature "bin" of the time/temperature histogram with the time spent in that temperature range. The resulting histogram data would appear graphically as shown in Figure 4.

The DS2435 allows for eight temperature ranges, or bins, to be specified by fixing the values of the bin limits, TA through TG. Once specified, the time spent in each of the bins (bin 1 being anything less than TA, bin 2 being temperatures between TA and TB, etc., and bin 8 being anything above TG) is recorded (t_1 being the time spent in bin 1, t_2 the time spent in bin 2, etc.). Using this information and data from the battery manufacturer regarding retained capacity, the actual battery capacity remaining may be closely approximated by the user.

TIME/TEMPERATURE HISTOGRAM Figure 4



MEMORY

The DS2435's memory is divided into five pages, each page filling 32 bytes of address space. Not all of the available addresses are used, however. Refer to the memory map of Figure 3 to see actual addresses which are available for use.

The first three pages of memory consist of a scratchpad RAM and then either a nonvolatile RAM (pages 1 and 2) or SRAM (page 3). The scratchpads help insure data integrity when communicating over the 1–wire bus. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command will transfer the data to the RAM (NV or SRAM). This process insures data integrity when modifying the memory.

The fourth page of memory consists of registers which contain the measured temperature value, time/temperature histogram registers, elapsed time counter, and status registers for the device; these registers are made from SRAM cells.

The fifth page of memory holds the ID number for the device, the cycle count registers and the histogram bin limits in E^2 RAM, making these registers nonvolatile under all power conditions.

PAGE 1

The first page of memory has 24 bytes. It consists of a scratchpad RAM and a nonvolatile (E^2) RAM. These 24 bytes may be used to store any data the user wishes; such as battery chemistry descriptors, manufacturing lot codes, gas gauge information, etc.

The nonvolatile portion of this page may be locked to prevent data stored here from being changed inadvertently.

Both the nonvolatile and the scratchpad portions are organized identically, as shown in the memory map of Figure 3. In this page, these two portions are referred to as NV1 and SP1, respectively.

PAGE 2

The second page of memory has 8 bytes. It consists of a scratchpad RAM and a nonvolatile (E^2) RAM. These eight bytes may be used to store any data the user wishes, such as battery chemistry descriptors, manufacturing lot codes, gas gauge information, etc.

PAGE 3

The third page of memory has a full 32 bytes. It consists of a scratchpad RAM and an SRAM. This address space may be used to store any data the user wishes, provided that, should the battery go dead and power to the DS2435 is lost, this data may also be lost without serious repercussions. Data which must remain even if power to the DS2435 is lost should be placed in either Page 1 or Page 2.

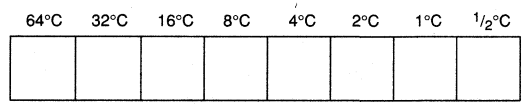
This section of memory may be used to store gas gauge and self discharge information. If the battery dies, and this information is lost, it is moot because the user can easily determine that the battery is dead.

PAGE 4

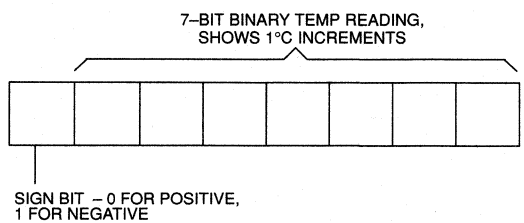
The fourth page of memory is used by the DS2435 to store the converted value of battery temperature, the time/temperature histogram data, and the elapsed time counter. A two–byte status register is also provided.

TEMPERATURE REGISTERS (60h–61h)

The DS2435 can measure temperature without external components. The resulting temperature measurement is placed into two temperature registers. These registers are SRAM, and therefore will hold the values placed in them until the battery voltage falls below the minimum V_{DD} specified. The first register, at address 60h, provides $^1/_2$°C resolution for temperatures between 0°C and 127 $^1/_2$°C, formatted as follows:



The second register, at address 61h, provides 1°C resolution over the –40°C to +85°C range, formatted as follows in the binary two's complement coding as shown in Table 1:



TEMPERATURE/DATA RELATIONSHIPS

Table 1

TEMPERATURE	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
+85°C	01010101	55h
+25°C	00011001	19h
1°C	00000001	01h
0°C	00000000	00h
–1°C	11111111	FFh
–25°C	11100111	E7h
–40°C	11011000	D8h

STATUS/CONTROL REGISTER (62h–63h)

The status register is a two byte register at addresses 62h and 63h (consisting of SRAM). Address 62h is the least significant byte of the status register, and is currently the only address with defined status bits; the other byte at address 63h is reserved for future use. The status register is formatted as follows:

STATUS REGISTER

							LSB	
X	X	X	X	X	LOCK	NVB	TB	62h
X	X	X	X	X	X	X	X	63h

where

X = Don't Care

TB = Temperature Busy flag. "1" = temperature conversion in progress; "0" = temperature conversion complete, valid data in temperature register.

NVB = Nonvolatile memory busy flag. "1" = Copy from scratchpad to NVRAM in progress, "0" = nonvolatile memory is not busy. A copy to NVRAM may take from 2 ms to 10 ms (taking longer at lower supply voltages).

LOCK = "1" indicates that NV1 is locked; "0" indicates that NV1 is unlocked.

t_1–t_8 REGISTERS (64h–73h)

These registers hold the accumulated time values for the time/temperature histogram. t_1 corresponds to the time spent in histogram bin 1, t_2 the time spent in bin 2, etc., where the bins are defined by the limits set in TA–TG as shown in Figure 4. The format for the time value stored in these two–byte registers depends upon the SAMPLE RATE, and is defined in the paragraph describing the SAMPLE RATE parameter.

t REGISTER (74n–76h)

This three–byte register is the elapsed time counter, formatted as follows:

ELAPSED TIME COUNTER

2^{23} min	2^{22} min	2^{21} min	2^{20} min	2^{19} min	2^{18} min	2^{17} min	2^{16} min	74h
32768 min	16384 min	8192 min	4096 min	2048 min	1024 min	512 min	256 min	75h
128 min	64 min	32 min	16 min	8 min	4 min	2 min	1 min	76h

The elapsed time counter has an LSB value of 1 minute; the total time which the counter can accommodate is 2^{24} minutes, or 31.92 years.

PAGE 5

The fifth page of memory holds the battery manufacturer ID number, a two–byte counter for counting the number of battery charge/discharge cycles, histogram bin limits, and sample rate.

ID REGISTER (80h and 81h)

The ID Register is a 16–bit ROM register that can contain a unique identification code, if purchased from Dallas Semiconductor. This ID number is programmed by Dallas Semiconductor, is unchangeable, and is unique to each customer. This ID number may be used to assure that batteries containing a DS2435 have the same manufacturer ID number as a charger configured to operate with that battery pack. This feature may be used to prevent charging of batteries for which the charging circuit has not been designed.

CYCLE COUNTER (82h and 83h)

The cycle counter register gives an indication of the number of charge/discharge cycles the battery pack has been through. This nonvolatile (E^2) register is incremented by the user through the use of a protocol to the DS2435, and is reset by another protocol. The counter is a straight binary counter, formatted as follows:

CYCLE COUNTER

MSB

32768	16384	8192	4096	2048	1024	512	256

65h

LSB

128	64	32	16	8	4	2	0

64h

TA–TG REGISTERS (84h–8Ah)

These registers define the boundaries for the temperature bins in the time/temperature histogram, as shown in Figure 4. These temperature values are expressed in the same temperature format as shown in Table 1. These limits therefore may be positive or negative values, expressed with 1°C resolution.

SAMPLE RATE (8Bh)

This register defines the periodic interval at which the DS2435 will take a temperature measurement for updating the histogram data. Note that this does not affect the actual time needed to perform a temperature conversion using the Convert T protocol; this sample rate refers only to the periodic interval at which histogram data is updated.

The sample rate is expressed in hours, as follows:

SAMPLE RATE

LSB

X	X	X	X	1	1/2	1/4	1/8

This value must be 1/8, 1/4, 1/2, or 1 (i.e., only one bit may be set in this register).

The interval specified in this register determines the LSB value for the time/temperature histogram registers, as shown in Figure 5. Examples of time expressions for a given sample rate are shown in Table 2.

HISTOGRAM REGISTER DATA GIVEN FOR SAMPLE RATE Figure 5

SAMPLE RATE	DATA STRUCTURE – NUMBERS EXPRESS HOURS															
																LSB
1/8	4096	2048	1024	512	256	128	64	32	16	8	4	2	1	.	1/2	1/4	1/8
1/4	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1	.	1/2	1/4
1/2	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1	.	1/2
1	32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1	.

EXAMPLE CODES FOR 771 HOURS, 22.5 MINUTES WITH DIFFERENT SAMPLE RATES Table 2

SAMPLE RATE	t_X BYTE 1	t_X BYTE 2
1/8	00011000	00011011
1/4	00001100	00001101
1/2	00000110	00000110
1	00000011	00000011

MEMORY FUNCTION COMMANDS

The protocols necessary for accessing the DS2435 are described in this section. These are summarized in Table 3, and examples of memory functions are provided in Tables 4 and 5.

PAGE 1 THROUGH PAGE 3 COMMANDS

Read Scratchpad [11h]

This command reads the contents of the scratchpad RAM on the DS2435. This command is followed by a start byte address. After issuing this command and providing the start address, the user may begin reading the data. The user may read data through the end of the scratchpad space (address 5Fh), with any reserved data bits reading all logic 1's and after which the data read will be a repeat of address 5FH.

Write Scratchpad [17h]

This command writes to the scratchpad RAM on the DS2435. This command is followed by a start byte address. After issuing this command and providing the start address, the user may begin writing data to the DS2435 scratchpad at the starting byte address.

Copy SP1 to NV1 [22h]

This command copies the entire contents (24 bytes) of Scratchpad 1 (SP1) to its corresponding nonvolatile memory (NV1). The nonvolatile RAM memory of the DS2435 cannot be written to directly by the bus master; however, the scratchpad RAM may be copied to the nonvolatile RAM. This prevents accidental overwriting of the nonvolatile RAM, and allows the data to be written first to the scratchpad, where it can be read back and verified before copying to the nonvolatile RAM. This command does not use a start address; the entire contents of the scratchpad will be copied to the nonvolatile RAM. The NVB bit will be set when the copy is in progress. NV1 is made with E^2 type memory cells that will accept at least 50000 changes.

Copy SP2 to NV2 [25h]

This command copies the entire contents (8 bytes) of SP2 (user bytes) to its corresponding nonvolatile memory (NV2). This command does not use a start address; the entire contents of SP2 will be copied to NV2. The NVB bit will be set when the copy is in progress. NV2 is made with E^2 type memory cells that will accept at least 50000 changes.

Copy SP3 to SRAM [28h]

This command copies the entire contents (32 bytes) of SP3 to its corresponding SRAM. This command does not use a start address; the entire contents of SP3 will be copied to the SRAM.

Copy NV1 to SP1 [71h]

This command copies the entire contents (24 bytes) of NV1 to its corresponding scratchpad RAM (SP1). This command does not use a start address; the entire contents of NV1 will be copied to SP1. The nonvolatile RAM memory of the DS2435 cannot be read directly by the bus master; however, the nonvolatile RAM may be copied to the scratchpad RAM.

Copy NV2 to SP2 [77h]

This command copies the entire contents (8 bytes) of NV2 (user bytes) to its corresponding scratchpad RAM (SP2). This command does not use a start address; the entire contents of NV2 will be copied to SP2. The nonvolatile RAM memory of the DS2435 cannot be read directly by the bus master; however, the nonvolatile RAM may be copied to the scratchpad RAM.

Copy SRAM to SP3 [7Ah]
This command copies the entire contents (32 bytes) of SRAM to its corresponding scratchpad RAM (SP3). This command does not use a start address; the entire contents of SRAM will be copied to SP3.The SRAM memory of the DS2435 cannot be read directly by the bus master; however, the SRAM may be copied to the scratchpad RAM.

Lock NV1 [43h]
This command prevents copying SP1 to NV1. This is done as an added measure of data security, preventing data from being changed inadvertently. NV1 may be copied up into SP1 while the part is locked. This allows NV1 to be read at any time. However, NV1 cannot be written to through a Copy SP1 to NV1 command without first unlocking the DS2435.

Unlock NV1 [44h]
This command unlocks NV1, to allow copying SP1 into NV1. This is done as an added measure of data security, preventing data from being changed inadvertently.

PAGE 4 AND 5 COMMANDS

Convert T [D2h]
This command instructs the DS2435 to initiate a temperature conversion cycle. This sets the TB flag. When the temperature conversion is done, the TB flag is reset and the current temperature value is placed in the temperature register. While a temperature conversion is taking place, all other memory functions are still available for use.

Reset Histogram [E1h]
This command resets the accumulated time in all of the histogram temperature registers to zero. This command does not use a start address; no further data is required.

Set Clock [E6h]
This command sets the elapsed time counter to a preset value. This command is followed by three bytes of data, which will be stored at addresses 74h–76h. The transfer of this 3–byte value will occur after reception of the 24th bit following the protocol, at which time the elapsed time counter will begin incrementing the counter registers in 1 minute increments.

Write Registers [EFh]
This command allows writing directly to the TA–TG registers and the sample rate register. This command is followed by a start byte address. After issuing this command and providing the start address, the user may begin writing the data.

Read Registers [B2h]
This command reads the contents of the registers in Page 4 and 5. This command is followed by a start byte address. After issuing this command and providing the start address, the user may begin reading the data. The user may read data through the end of the register space (through address 76h in Page 4, address 8Bh in Page 5), after which the data read will be all logic 1's.

Increment Cycle [B5h]
This command increments the value in the cycle counter register. This command does not use a start address; no further data is required.

Reset Cycle Counter [B8h]
This command is used to reset the cycle counter register to zero, if desired.

DS2435 COMMAND SET Table 3

INSTRUCTION	DESCRIPTION	PROTOCOL	1–WIRE BUS MASTER STATUS AFTER ISSUING PROTOCOL	1–WIRE BUS DATA AFTER ISSUING PROTOCOL
PAGE 1 through PAGE 3 Memory Commands				
Read Scratchpad	Reads bytes from DS2435 Scratchpad.	11h <addr (00h–5Fh)>	RX	<read data>
Write Scratchpad	Writes bytes to DS2435 Scratchpad.	17h <addr 00h–5Fh)>	TX	<write data>
Copy SP1 to NV1	Copies entire contents of SP1 to NV1.	22h	Idle	{NVB bit in Status Register=1 until copy complete (2–5ms, typ)}
Copy SP2 to NV2	Copies entire contents of SP2 to NV2.	25h	Idle	{NVB bit in Status Register=1 until copy complete (2–5ms, typ)}
Copy SP3 to SRAM	Copies entire contents of SP3 to SRAM.	28h	Idle	Idle
Copy NV1 to SP1	Copies entire contents of NV1 to SP1.	71h	Idle	Idle
Copy NV2 to SP2	Copies entire contents of NV2 to SP2.	77h	Idle	Idle
Copy SRAM to SP3	Copies entire contents of SRAM to SP3.	7Ah	Idle	Idle
Lock NV1	Locks 24 bytes of SP1 and NV1 from reading and writing.	43h	Idle	{NVB bit in Status Register=1 until copy complete (2–5ms, typ)}
Unlock NV1	Unlocks 24 bytes of SP1 and NV1 for reading and writing.	44h	Idle	{NVB bit in Status Register=1 until copy complete (2–5ms, typ)}
PAGE 4 and PAGE 5 Register Commands				
Read Registers	Reads bytes from Temperature, Status and ID Registers.	B2h <addr (60h–76h, 80h–8Bh)>	RX	<read data>
Write Register	Write to TA–TG and Sample Rate Registers	EFh <addr 84h–8Bh>		
Reset Cycle Counter	Resets cycle counter registers to zero.	B8h	Idle	{NVB bit in Status Register=1 until copy complete (2–5ms, typ)}
Increment Cycle Counter	Increments the value in the cycle counter register.	B5h	Idle	{NVB bit in Status Register=1 until copy complete (2–5ms, typ)}
Reset Historgram	Resets all histogram registers to zero	E1h	Idle	Idle
Set Clock	Presets a value for elapsed time counter and begins timing.	E6h	TX	<3 bytes>
Convert T	Initiates temperature conversion.	D2h	Idle	{TB bit in Status Register=1 until conversion complete}

MEMORY FUNCTION EXAMPLE Table 4
Example: Bus Master writes 24 bytes of data to DS2435 scratchpad, then copies to it to NV1.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480–960 µs)
RX	Presence	Presence pulse
TX	17h	Issue "write scratchpad" command
TX	00h	Start address
TX	<24 bytes>	Write 24 bytes of data to scratchpad
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	11h	Issue "read scratchpad" command
TX	00h	Start address
RX	<24 data bytes>	Read scratchpad data and verify
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	22h	Issue "copy SP1 to NV1" command
RX	<busy indicator>	Wait until NVB in status register=1 (2–5 ms typical)
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

MEMORY FUNCTION EXAMPLE Table 5
Example: Bus Master initiates temperature conversion, then reads temperature.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480–960 µs)
RX	Presence	Presence pulse
TX	D2h	Issue "convert T" command
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	B2h	Issue "read registers" command; begin loop
TX	62h	Status register address
RX	<1 data byte>	Read status register and loop until TB=0
TX	Reset	Reset pulse
RX	Presence	Presence pulse
TX	B2h	Issue "read registers" command
TX	61h	Temperature register address
RX	<1 data byte>	Read temperature register
TX	Reset	Reset pulse
RX	Presence	Presence pulse, done

1–WIRE BUS SYSTEM

The DS2435 1–wire bus is a system which has a single bus master and one slave. The DS2435 behaves as a slave. The DS2435 is not able to be multidropped, unlike other 1–wire devices from Dallas Semiconductor.

The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1–wire signaling (signal types and timing).

HARDWARE CONFIGURATION

The 1–wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1–wire bus must have open drain or 3–state outputs. The 1–wire port of the DS2435 is open drain with an internal circuit equivalent to that shown in Figure 6. The 1–wire bus requires a pull–up resistor of approximately 5KΩ.

The idle state for the 1–wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 480 µs, all components on the bus will be reset.

TRANSACTION SEQUENCE

The protocol for accessing the DS2435 via the 1–wire port is as follows:

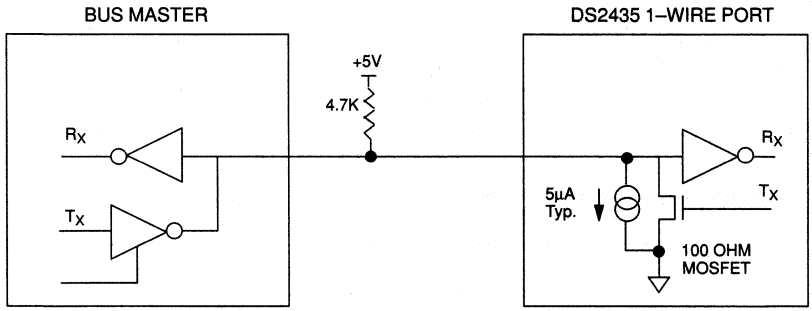
- Initialization
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1–wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS2435 is on the bus and is ready to operate. For more details, see the "I/O Signaling" section.

HARDWARE CONFIGURATION Figure 6



I/O SIGNALING

The DS2435 requires strict protocols to insure data integrity. The protocol consists of several types of signaling on one line: reset pulse, presence pulse, write 0, write 1, read 0, and read 1. All of these signals, with the exception of the presence pulse, are initiated by the bus master.

The initialization sequence required to begin any communication with the DS2435 is shown in Figure 7. A reset pulse followed by a presence pulse indicates the DS2435 is ready to send or receive data given the correct memory function command.

The bus master transmits (TX) a reset pulse (a low signal for a minimum of 480 µs). The bus master then releases the line and goes into a receive mode (RX). The 1–wire bus is pulled to a high state via the 5K pull–up resistor. After detecting the rising edge on the I/O pin, the DS2435 waits 15–60 µs and then transmits the presence pulse (a low signal for 60–240 µs).

READ/WRITE TIME SLOTS

DS2435 data is read and written through the use of time slots to manipulate bits and a command word to specify the transaction.

Write Time Slots

A write time slot is initiated when the host pulls the data line from a high logic level to a low logic level. There are two types of write time slots: Write One time slots and Write Zero time slots. All write time slots must be a minimum of 60 µs in duration with a minimum of a 1 µs recovery time between individual write cycles.

The DS2435 samples the I/O line in a window of 15 µs to 60 µs after the I/O line falls. If the line is high, a Write One occurs. If the line is low, a Write Zero occurs (see Figure 6).

For the host to generate a Write One time slot, the data line must be pulled to a logic low level and then released, allowing the data line to pull up to a high level within 15 µs after the start of the write time slot.

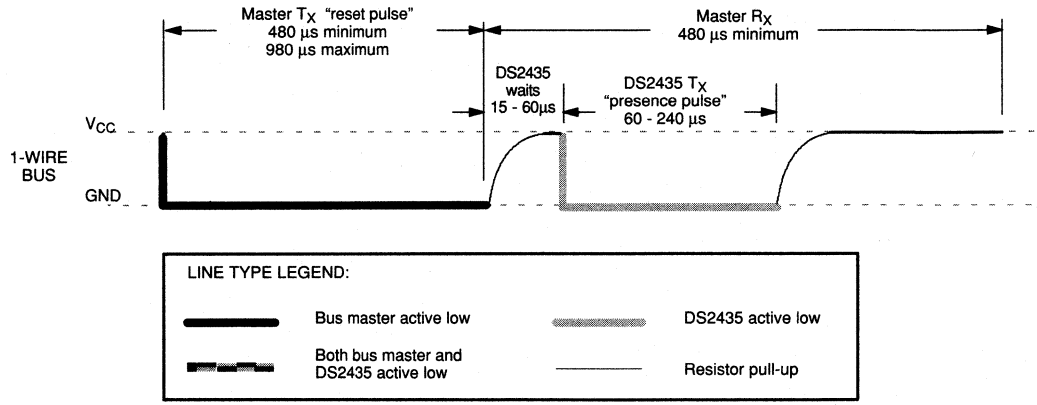
For the host to generate a Write Zero time slot, the data line must be pulled to a logic low level and remain low for the duration of the write time slot.

Read Time Slots

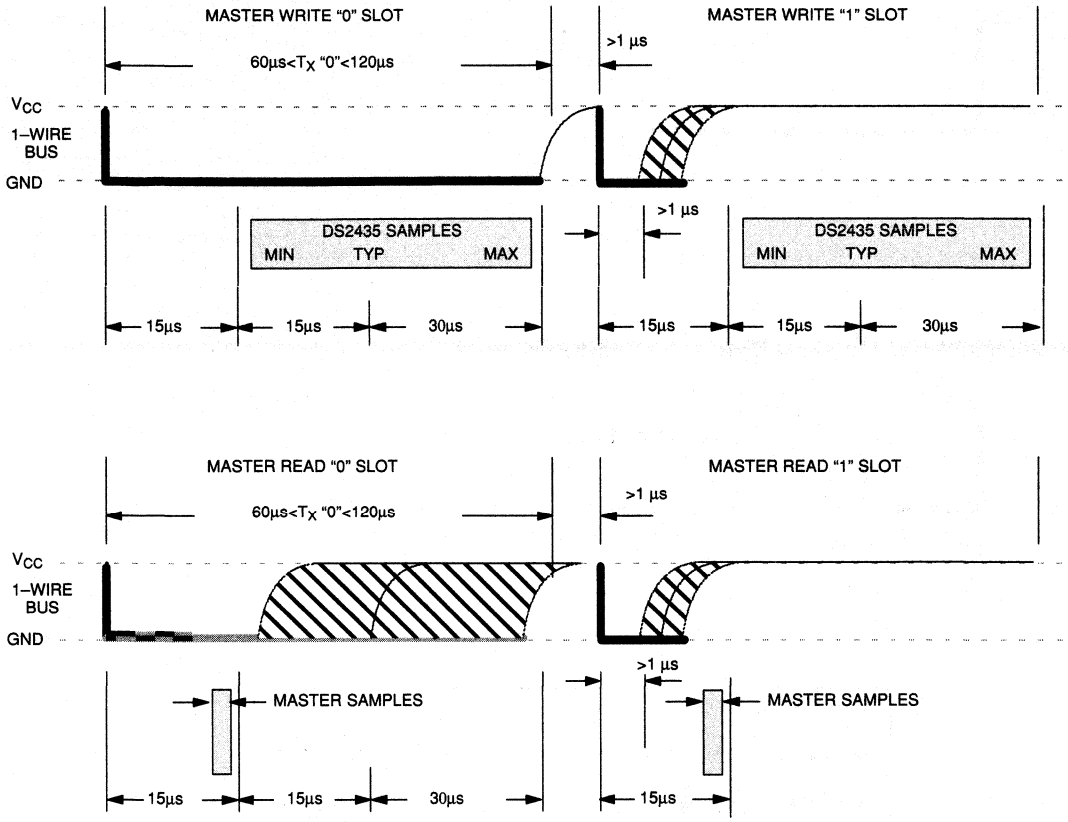
The host generates read time slots when data is to be read from the DS2435. A read time slot is initiated when the host pulls the data line from a logic high level to logic low level. The data line must remain at a low logic level for a minimum of 1 µs; output data from the DS2435 is then valid for the next 14 µs maximum. The host therefore must stop driving the I/O pin low in order to read its state 15 µs from the start of the read slot (see Figure 8). By the end of the read time slot, the I/O pin will pull back high via the external pull–up resistor. All read time slots must be a minimum of 60 µs in duration with a minimum of a 1 µs recovery time between individual read slots.

Figure 9 shows that the sum of T_{INIT}, T_{RC}, and T_{SAMPLE} must be less than 15 µs. Figure 10 shows that system timing margin is maximized by keeping T_{INIT} and T_{RC} as small as possible and by locating the master sample time towards the end of the 15 µs period.

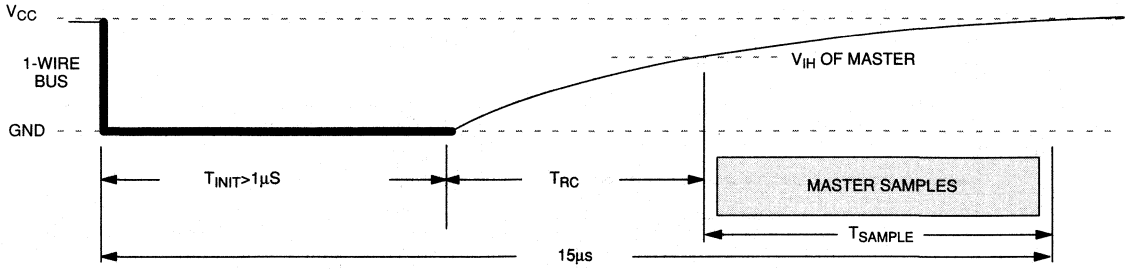
INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 7



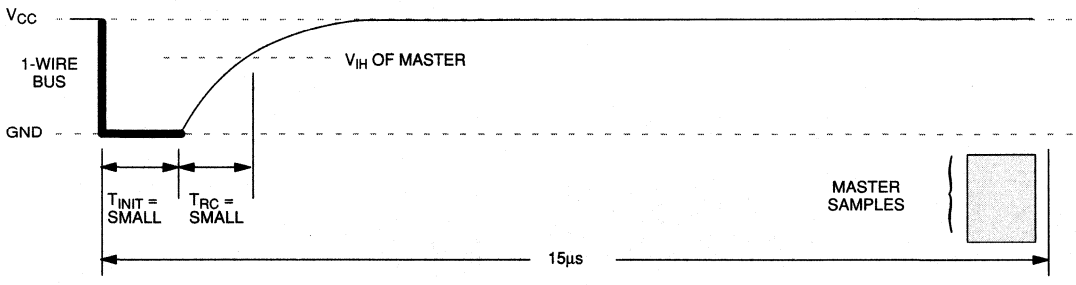
READ/WRITE TIMING DIAGRAM Figure 8

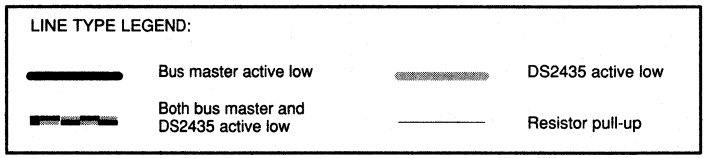


DETAILED MASTER READ "1" TIMING Figure 9



RECOMMENDED MASTER READ "1" TIMING Figure 10





ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	–40°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C; V_{DD}=3.6V to 6.4V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	I/O Functions	2.5		6.4	V	
		NV Copy Functions	2.7		6.4		
		±1/2°C Accurate Temp. Conversions	3.6		6.4		1
Data Pin	$V_{I/O}$		–0.3		V_{CC}+0.3	V	

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{DD}=3.6V to 6.4V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Temperature Accuracy (=T_{ACTUAL} – $T_{MEASURED}$)		T_A=0°C to 70°C			±1/2	°C	
		T_A=–40°C to 0°C and +70°C to +85°C			±1		
Input Logic High	V_{IH}		2.2		V_{CC}+0.3	V	
Input Logic Low	V_{IL}		–0.3		+0.8	V	
Sink Current	I_L	$V_{I/O}$=0.4V	–4.0			mA	
Standby Current	I_Q	Clock Running			10	µA	
Active Current	I_{DD}	Temp Conversions			1.5	mA	
Input Resistance	R_I			500		KΩ	2

NOTES:

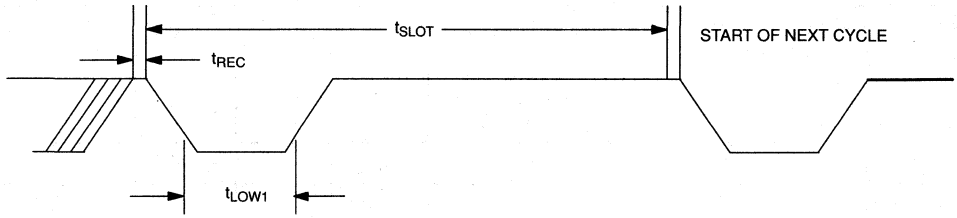
1. Temperature conversion will work with ±2°C accuracy down to V_{DD}=2.7V.
2. I/O line in "hi–Z" state and $I_{I/O}$=0.

AC ELECTRICAL CHARACTERISTICS: 1–WIRE INTERFACE

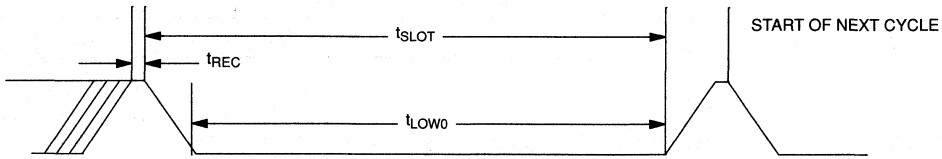
(–40°C to +85°C; V_{DD}=3.6V to 6.4V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Temperature Conversion Time	t_{CONV}		700	1000	ms	
Time Slot	t_{SLOT}	60		120	µs	
Recovery Time	t_{REC}	1			µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Read Data Valid	t_{RDV}			15	µs	
Reset Time High	t_{RSTH}	480			µs	
Reset Time Low	t_{RSTL}	480		960	µs	
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	
Capacitance	$C_{IN/OUT}$			25	pF	
Timer Accuracy				±10	%	

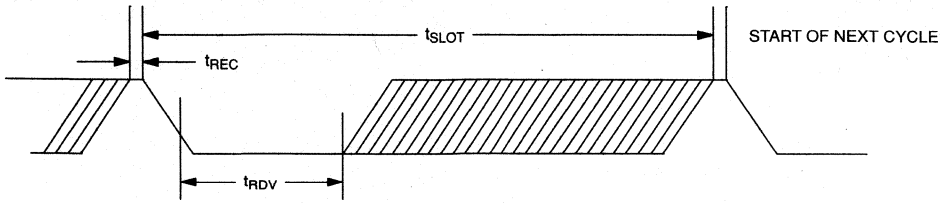
1–WIRE WRITE ONE TIME SLOT



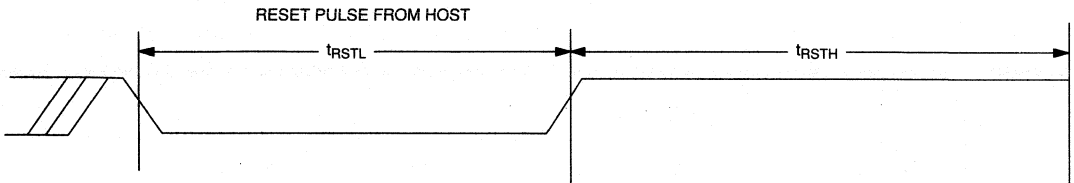
1–WIRE WRITE ZERO TIME SLOT



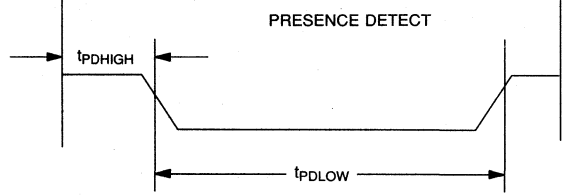
1-WIRE READ ZERO TIME SLOT



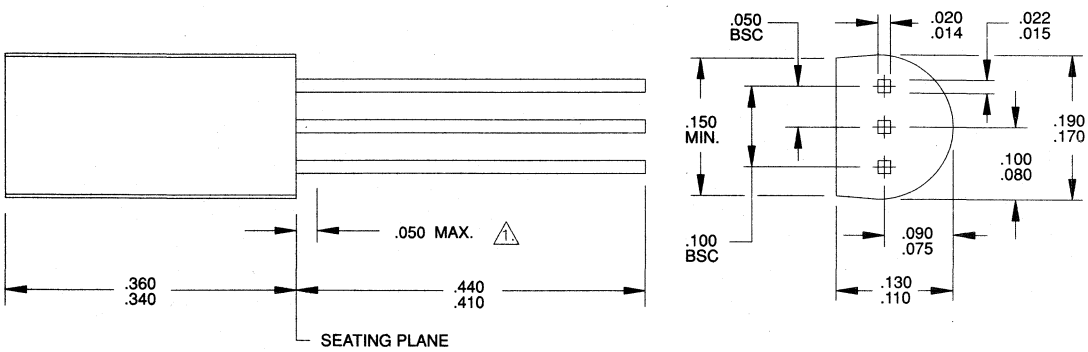
1-WIRE PRESENCE DETECT



1-WIRE RESET PULSE



PACKAGE DIAGRAM



CPU SUPERVISORS

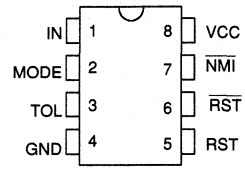
DALLAS SEMICONDUCTOR

DS1231/S
Power Monitor Chip

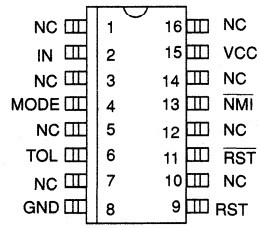
FEATURES

- Warns processor of an impending power failure
- Provides time for an orderly shutdown
- Prevents processor from destroying nonvolatile memory during power transients
- Automatically restarts processor after power is restored
- Suitable for linear or switching power supplies
- Adjusts to hold time of the power supply
- Supplies necessary signals for processor interface
- Accurate 5% or 10% V_{CC} monitoring
- Replaces power-up reset circuitry
- No external capacitors required
- Optional 16-pin SOIC surface mount package

PIN ASSIGNMENT



DS1231 8–Pin DIP
(300 MIL)
See Mech. Drawing
Pg. 480



DS1231S 16–Pin SOIC
(300 MIL)
See Mech. Drawing
Pg. 484

PIN DESCRIPTION

IN	–	Input
MODE	–	Selects input pin characteristics
TOL	–	Selects 5% or 10% V_{CC} detect
GND	–	Ground
RST	–	Reset (Active High)
$\overline{RST}$	–	Reset (Active Low, open drain)
$\overline{NMI}$	–	Non–Maskable Interrupt
V_{CC}	–	+5V Supply
NC	–	No Connections

DESCRIPTION

The DS1231 Power Monitor Chip uses a precise temperature-compensated reference circuit which provides an orderly shutdown and an automatic restart of a processor-based system. A signal warning of an impending power failure is generated well before regulated DC voltages go out of specification by monitoring high voltage inputs to the power supply regulators. If line isolation is required a UL-approved opto-isolator can be directly interfaced to the DS1231. The time for processor shutdown is directly proportional to the available hold-up time of the power supply. Just before the hold-up time is exhausted, the Power Monitor unconditionally halts the processor to prevent spurious cycles by enabling Reset as V_{CC} falls below a selectable 5 or 10 percent threshold. When power returns, the processor is held inactive until well after power conditions have stabilized, safeguarding any nonvolatile memory in the system from inadvertent data changes.

OPERATION

The DS1231 Power Monitor detects out-of-tolerance power supply conditions and warns a processor-based system of impending power failure. The main elements of the DS1231 are illustrated in Figure 1. As shown, the DS1231 actually has two comparators, one for monitoring the input (Pin 1) and one for monitoring V_{CC} (Pin 8). The V_{CC} comparator outputs the signals RST (Pin 5) and $\overline{RST}$ (Pin 6) when V_{CC} falls below a preset trip level as defined by TOL (Pin 3).

When TOL is connected to ground, the RST and $\overline{RST}$ signals will become active as V_{CC} goes below 4.75 volts. When TOL is connected to V_{CC}, the RST and $\overline{RST}$ signals become active as V_{CC} goes below 4.5 volts. The RST and $\overline{RST}$ signals are excellent control signals for a microprocessor, as processing is stopped at the last possible moments of valid V_{CC}. On power-up, RST and $\overline{RST}$ are kept active for a minimum of 150 ms to allow the power supply to stabilize (see Figure 2).

The comparator monitoring the input pin produces the $\overline{NMI}$ signal (Pin 7) when the input threshold voltage (V_{TP}) falls to a level as determined by Mode (Pin 2). When the Mode pin is connected to V_{CC}, detection occurs at V_{TP}-. In this mode Pin 1 is an extremely high impedance input allowing for a simple resistor voltage divider network to interface with high voltage signals. When the Mode pin is connected to ground, detection occurs at V_{TP}+. In this mode Pin 1 sources 30 µA of current allowing for connection to switched inputs, such as a UL-approved opto-isolator. The flexibility of the input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time allotted between $\overline{NMI}$ and $\overline{RST}$. On power-up, $\overline{NMI}$ is released as soon as the input threshold voltage (V_{TP}) is achieved and V_{CC} is within nominal limits. In both modes of operation the input pin has hysteresis for noise immunity (Figure 3).

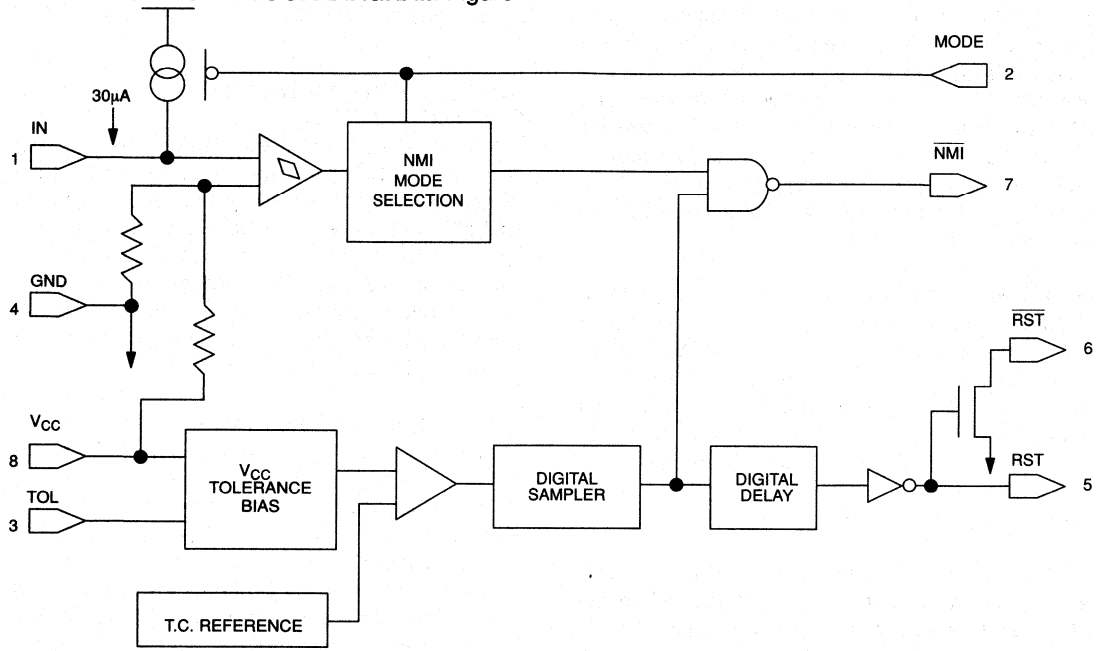
APPLICATION – MODE PIN CONNECTED TO V_{CC}

When the Mode pin is connected to V_{CC}, pin 1 is a high impedance input. The voltage sense point and the level of voltage at the sense point are dependent upon the application (Figure 4). The sense point may be developed from the AC power line by rectifying and filtering the AC. Alternatively, a DC voltage level may be selected which is closer to the AC power input than the regulated +5-volt supply, so that ample time is provided for warning before regulation is lost.

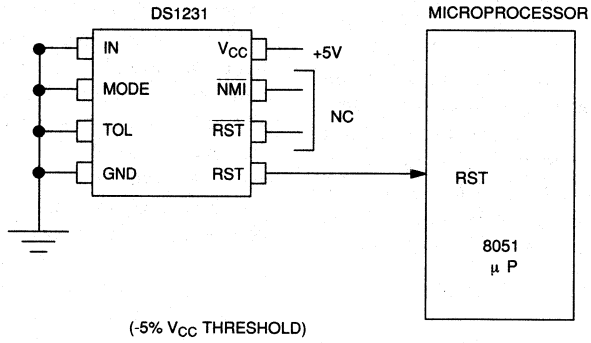
Proper operation of the DS1231 requires a maximum voltage of 5 volts at the input (Pin 1), which must be derived from the maximum voltage at the sense point. This is accomplished with a simple voltage divider network of R1 and R2. Since the IN trip point V_{TP}- is 2.3 volts (using the -20 device), and the maximum allowable voltage on pin 1 is 5 volts, the dynamic range of voltage at the sense point is set by the ratio of 2.3/5.0=.46 min. This ratio determines the maximum deviation between the maximum voltage at the sense point and the actual voltage which will generate $\overline{NMI}$.

Having established the desired ratio, and confirming that the ratio is greater than .46 and less than 1, the proper values for R1 and R2 can be determined by the equation as shown in Figure 4. A simple approach to solving this equation is to select a value for R2 which is high enough impedance to keep power consumption low, and solve for R1. Figure 5 illustrates how the DS1231 can be interfaced to the AC power line when the mode pin is connected to V_{CC}.

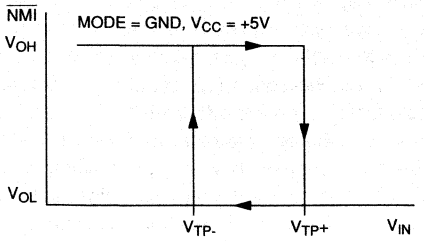
POWER MONITOR BLOCK DIAGRAM Figure 1



POWER-UP RESET Figure 2

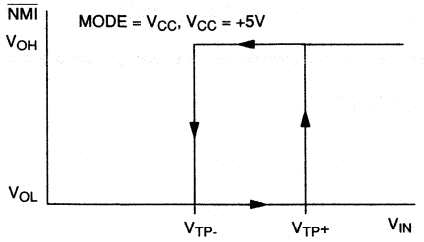


INPUT PIN HYSTERESIS Figure 3

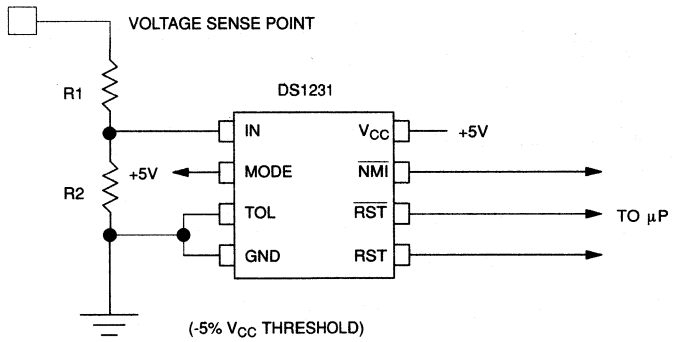


	–20	–35	–50
V_{TP-}	2.3	2.15	2.0
V_{TP+}	2.5	2.5	2.5

NOTE: HYSTERESIS TOLERANCE IS ±60 mV



APPLICATION WITH MODE PIN CONNECTED TO V_{CC} Figure 4



$$V\ SENSE = \frac{R1 + R2}{R2} \times 2.3 \qquad V\ MAX = \frac{V\ SENSE}{VTP -} \times 5.0$$

EXAMPLE: V SENSE = 8 VOLTS AT TRIP POINT AND A MAXIMUM VOLTAGE OF 17.5V WITH R2 = 10K

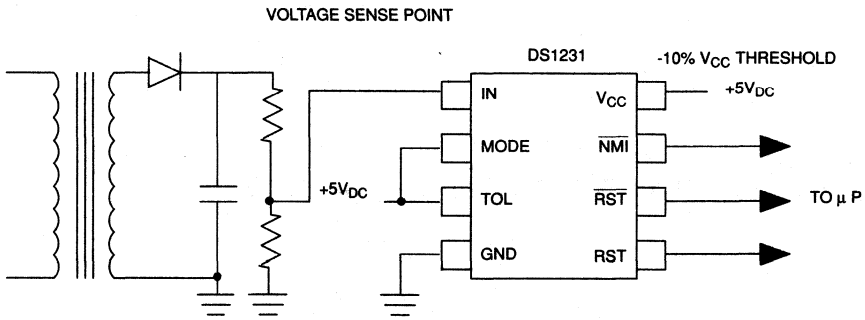
$$THEN\ 8 = \frac{R1 + 10K}{10K} \times 2.3 \qquad R1 = 25K$$

NOTE: $\overline{RST}$ requires a pull–up resister.

APPLICATION – MODE PIN CONNECTED TO GROUND

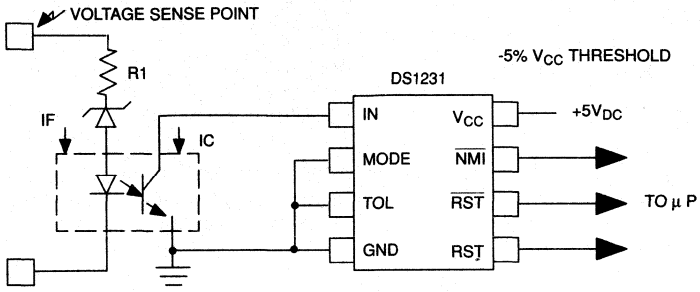
When the Mode pin is connected to ground, pin 1 is a current source of 30 µA with a V_{TP+} of 2.5 volts. Pin 1 is held below the trip point by a switching device like an opto-isolator as shown in Figure 6. Determination of the sense point has the same criteria as discussed in the previous application. However, determining component values is significantly different. In this mode, the maximum dynamic range of the sense point versus desired trip voltage is primarily determined by the selection of a zener diode. As an example, if the maximum voltage at the sense point is 200V and the desired trip point is 150V, then a zener diode of 150V will approximately set the trip point. This is particularly true if power consumption on the high voltage side of the opto-isolator is not an issue. However, if power consumption is a concern, then it is desirable to make the value of R1 high. As the value of R1 increases, the effect of the LED current in the opto-isolator starts to affect the IN trip point. This can be seen from the equation shown in Figure 6. R1 must also be low enough to allow the opto-isolator to sink the 30 µA of collector current required by pin 1 and still have enough resistance to keep the maximum current through the opto-isolator's LED within data sheet limits. Figure 7 illustrates how the DS1231 can be interfaced to the AC power line when the mode pin is grounded.

AC VOLTAGE MONITOR WITH TRANSFORMER ISOLATION Figure 5



NOTE: $\overline{RST}$ requires a pull–up resister.

APPLICATION WITH MODE PIN GROUNDED Figure 6



$$\text{VOLTAGE SENSE POINT (TRIP VALUE)} = VZ + \frac{IC}{CTR} \times R1$$

$$CTR = \frac{IC}{IF}$$

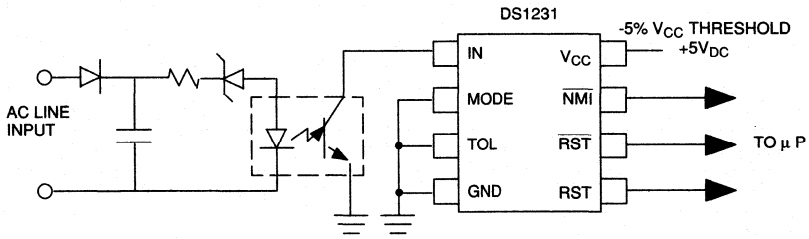
CTR = CURRENT TRANSFER RATIO
VZ = ZENNER VOLTAGE

EXAMPLE: CTR = 0.2 IC = 30 μA IF = 150 μA
VOLTAGE SENSE POINT = 105 AND
VZ = 100 VOLTS

$$\text{THEN } 105 = 100 + \frac{30}{0.2} \times R1 \qquad R1 = 33K$$

NOTE: $\overline{RST}$ requires a pull–up resister.

AC VOLTAGE MONITOR WITH OPTO-ISOLATION Figure 7



NOTE: $\overline{RST}$ requires a pull–up resister.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	-0.5V to +7.0V
Voltage on I/O Relative to Ground	-0.5V to V_{CC} + 0.5V
Operating Temperature	0°C to 70°C
Operating Temperature (Industrial Version)	–40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input Pin 1	V_{IN}			V_{CC}	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Low Level @ RST	V_{OL}			0.4	V	1
Output Voltage @ –500 µA	V_{OH}	V_{CC}–0.5V	V_{CC}–0.1V		V	1, 6
Input Leakage	I_{IL}	-10		+10	µA	2
Output Current @2.4V	I_{OH}	1.0	2.0		mA	5
Output Current @0.4V	I_{OL}	2.0	3.0		mA	
Operating Current	I_{CC}		0.5	2.0	mA	3
Input Pin 1 (Mode=GND)	I_C	15	25	50	µA	
Input Pin 1 (Mode=V_{CC})	I_C			0.1	µA	
IN Trip Piont (Mode=GND)	V_{TP}	See Figure 3				1
IN Trip Point (Mode=V_{CC})	V_{TP}					1
V_{CC} Trip Point (TOL=GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL=V_{CC})	V_{CCTP}	4.25	4.37	4.49	V	1

CAPACITANCE

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

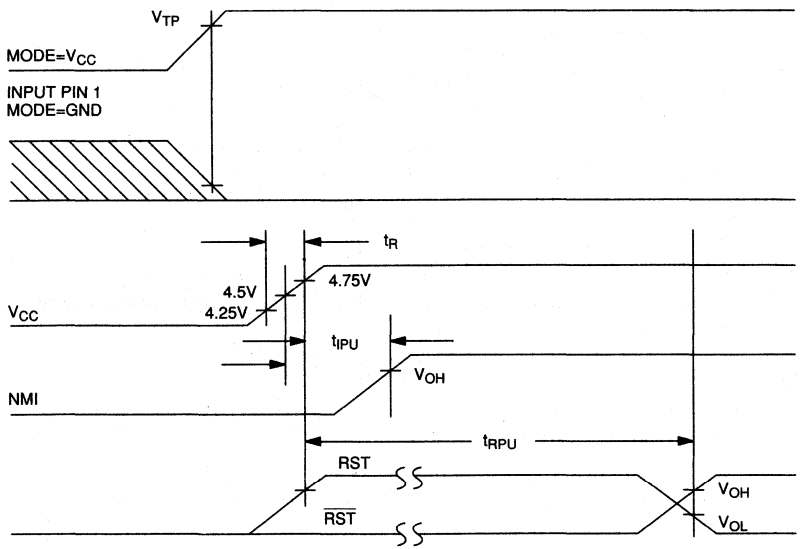
($0°C$ to $70°C$; $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{TP} to $\overline{NMI}$ Delay	t_{IPD}			1.1	µs	
V_{CC} Slew Rate 4.75-4.25V	t_F	300			µs	
V_{CC} Detect to RST and $\overline{RST}$	t_{RPD}			100	ns	
V_{CC} Detect to $\overline{NMI}$	t_{IPU}			200	µs	4
V_{CC} Detect to RST and $\overline{RST}$	t_{RPU}	150	500	1000	ms	4
V_{CC} Slew Rate 4.25-4.75V	t_R	0			ns	

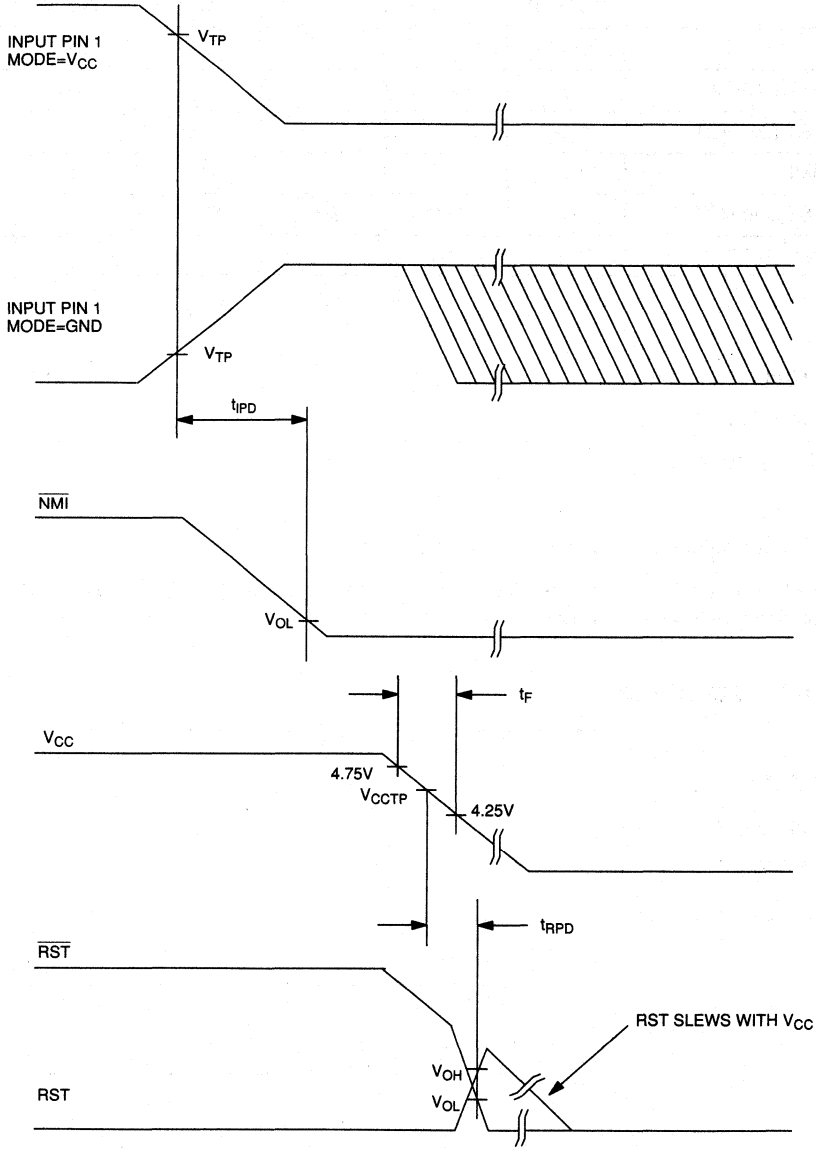
NOTES:

1. All voltages referenced to ground.
2. V_{CC} = +5.0 volts with outputs open.
3. Measured with outputs open.
4. t_R = 5 µs.
5. $\overline{RST}$ is an open drain output and requires a pull–up resister.
6. RST remains within 0.5V of V_{CC} on power–down until V_{CC} drops below 2.0V. $\overline{RST}$ remains within 0.5V of GND on power–down until V_{CC} drops below 2.0V.

TIMING DIAGRAM: POWER-UP



TIMING DIAGRAM: POWER-DOWN



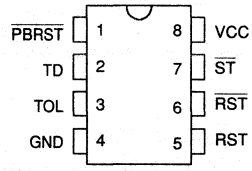
DALLAS SEMICONDUCTOR

DS1232
MicroMonitor Chip

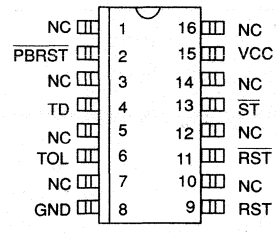
FEATURES

- Halts and restarts an out-of-control microprocessor
- Holds microprocessor in check during power transients
- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Accurate 5% or 10% microprocessor power supply monitoring
- Eliminates the need for discrete components
- Space-saving, 8-pin mini-DIP
- Optional 16-pin SOIC surface mount package
- Industrial temperature -40°C to +85°C available, designated N

PIN ASSIGNMENT



DS1232 8-Pin DIP
(300 Mil)
See Mech. Drawing
Pg. 480



DS1232S 16-Pin SOIC
(300 Mil)
See Mech. Drawing
Pg. 484

PIN DESCRIPTION

$\overline{PBRST}$	–	Pushbutton Reset Input
TD	–	Time Delay Set
TOL	–	Selects 5% or 10% V_{CC} Detect
GND	–	Ground
RST	–	Reset Output (Active High)
$\overline{RST}$	–	Reset Output (Active Low, open drain)
$\overline{ST}$	–	Strobe Input
V_{CC}	–	+5 Volt Power
NC	–	No Connections

DESCRIPTION

The DS1232 MicroMonitor Chip monitors three vital conditions for a microprocessor: power supply, software execution, and external override. First, a precision temperature-compensated reference and comparator circuit monitors the status of V_{CC}. When an out-of-tolerance condition occurs, an internal power fail signal is generated which forces reset to the active state. When V_{CC} returns to an in-tolerance condition, the reset signals are kept in the active state for a minimum of 250 ms to allow the power supply and processor to stabilize.

The second function the DS1232 performs is pushbutton reset control. The DS1232 debounces the pushbutton input and guarantees an active reset pulse width of 250 ms minimum. The third function is a watchdog timer. The DS1232 has an internal timer that forces the reset signals to the active state if the strobe input is not driven low prior to time-out. The watchdog timer function can be set to operate on time-out settings of approximately 150 ms, 600 ms, and 1.2 seconds.

OPERATION - POWER MONITOR

The DS1232 detects out-of-tolerance power supply conditions and warns a processor-based system of impending power failure. When V_{CC} falls below a preset level as defined by TOL (Pin 3), the V_{CC} comparator outputs the signals RST (Pin 5) and $\overline{RST}$ (Pin 6). When TOL is connected to ground, the RST and $\overline{RST}$ signals become active as V_{CC} falls below 4.75 volts. When TOL is connected to V_{CC}, the RST and $\overline{RST}$ signals become active as V_{CC} falls below 4.5 volts. The RST and $\overline{RST}$ are excellent control signals for a microprocessor, as processing is stopped at the last possible moments of valid V_{CC}. On power-up, RST and $\overline{RST}$ are kept active for a minimum of 250 ms to allow the power supply and processor to stabilize.

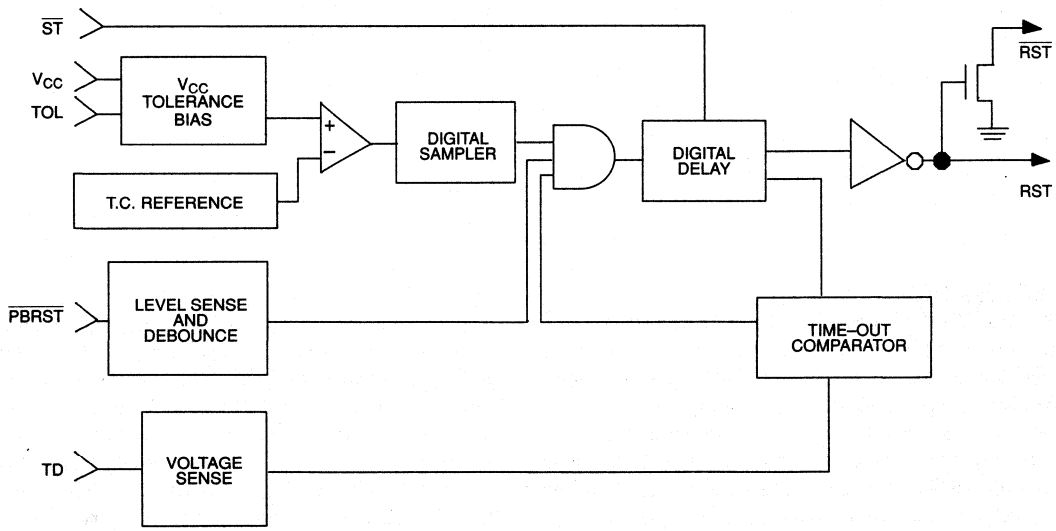
OPERATION - PUSHBUTTON RESET

The DS1232 provides an input pin for direct connection to a pushbutton (Figure 2). The pushbutton reset input requires an active low signal. Internally, this input is debounced and timed such that RST and $\overline{RST}$ signals of at least 250 ms minimum are generated. The 250 ms delay starts as the pushbutton reset input is released from low level.

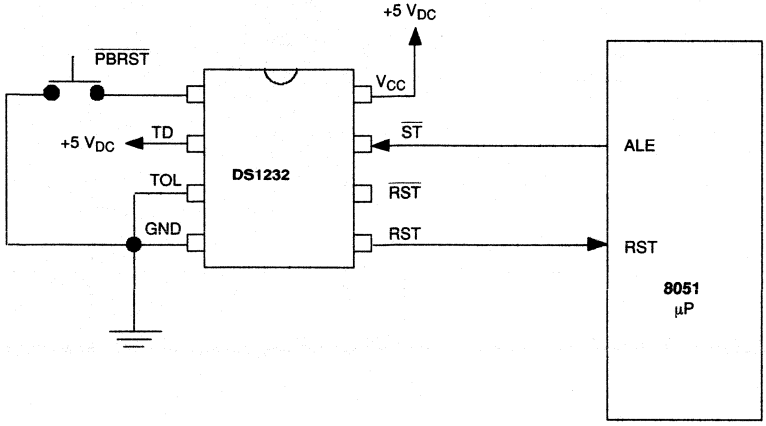
OPERATION - WATCHDOG TIMER

A watchdog timer function forces RST and $\overline{RST}$ signals to the active state when the $\overline{ST}$ input is not stimulated for a predetermined time period. The time period is set by the TD input to be typically 150 ms with TD connected to ground, 600 ms with TD left unconnected, and 1.2 seconds with TD connected to V_{CC}. The watchdog timer starts timing out from the set time period as soon as RST and $\overline{RST}$ are inactive. If a high-to-low transition occurs on the $\overline{ST}$ input pin prior to time-out, the watchdog timer is reset and begins to time-out again. If the watchdog timer is allowed to time-out, then the RST and $\overline{RST}$ signals are driven to the active state for 250 ms minimum. The $\overline{ST}$ input can be derived from microprocessor address signals, data signals, and/or control signals. When the microprocessor is functioning normally, these signals would, as a matter of routine, cause the watchdog to be reset prior to time-out. To guarantee that the watchdog timer does not time-out, a high-to-low transition must occur at or less than the minimum shown in Table 1. A typical circuit example is shown in Figure 3.

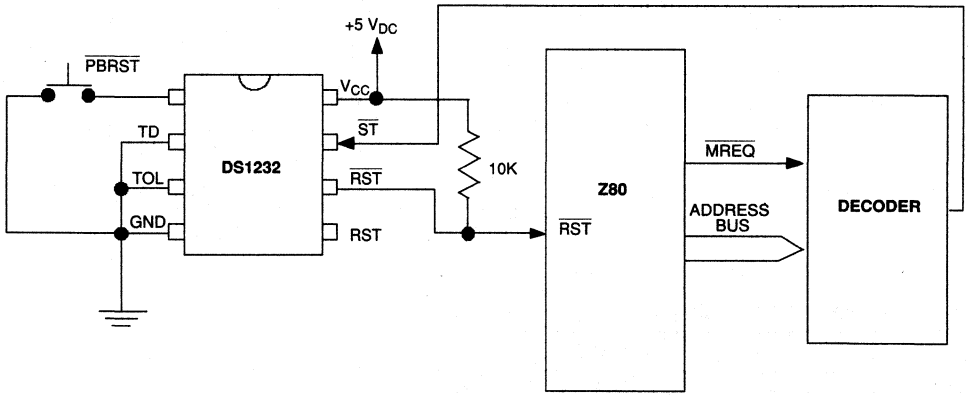
MICROMONITOR BLOCK DIAGRAM Figure 1



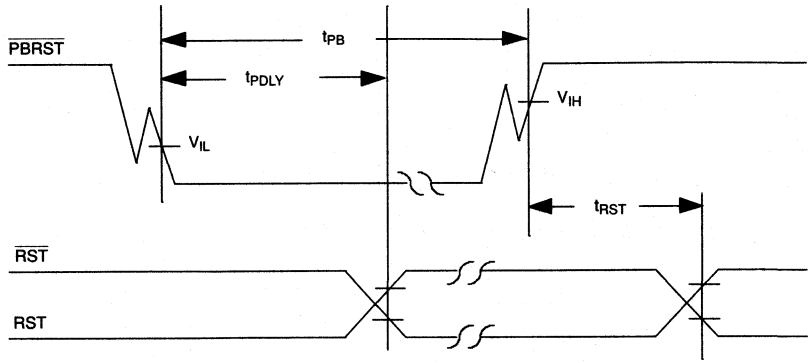
PUSHBUTTON RESET Figure 2



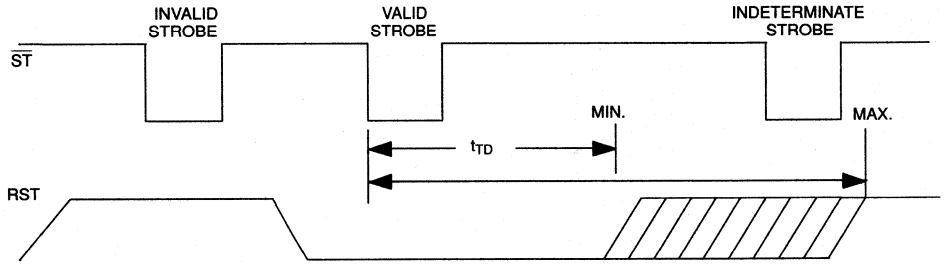
WATCHDOG TIMER Figure 3



TIMING DIAGRAM: PUSHBUTTON RESET Figure 4



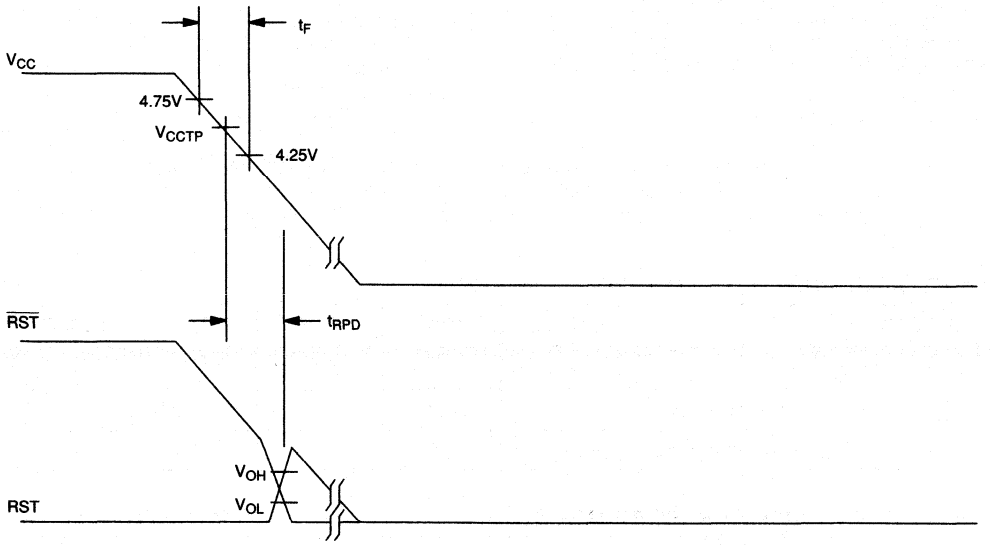
TIMING DIAGRAM: STROBE INPUT Figure 5



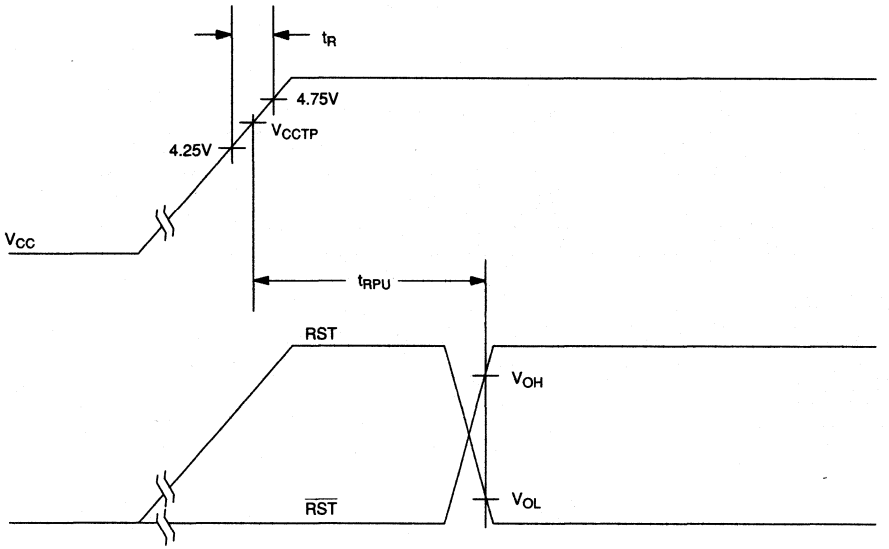
WATCHDOG TIMEOUTS Table 1

TD PIN	TIME-OUT		
	MIN	TYP	MAX
GND	62.5 ms	150 ms	250 ms
Float	250 ms	600 ms	1000 ms
V_{CC}	500 ms	1200 ms	2000 ms

TIMING DIAGRAM: POWER DOWN Figure 6



TIMING DIAGRAM: POWER UP Figure 7



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	-0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	0°C to 70°C
Operating Temperature (Industrial Version)	–40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
$\overline{ST}$ and $\overline{PBRST}$ Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	1
$\overline{ST}$ and $\overline{PBRST}$ Input Low Level	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1.0		+1.0	µA	3
Output Current @ 2.4V	I_{OH}	-8	-10		mA	5
Output Current @ 0.4V	I_{OL}	8	10		mA	
Low Level @ RST	V_{OL}			0.4	V	1
Output Voltage @ -500 µA	V_{OH}	V_{CC} -0.5V	V_{CC} -0.1V		V	1, 7
Operating Current	I_{CC}		0.5	2.0	mA	2
V_{CC} Trip Point (TOL = GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL = V_{CC})	V_{CCTP}	4.25	4.37	4.49	V	1

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{PBRST}$ = V_{IL}	t_{PB}	20			ms	
RESET Active Time	t_{RST}	250	610	1000	ms	
$\overline{ST}$ Pulse Width	t_{ST}	20			ns	6, 8
V_{CC} Fail Detect to RST and $\overline{RST}$	t_{RPD}	40	100	175	µs	
V_{CC} Slew Rate 4.75V to 4.25V	t_F	300			µs	
V_{CC} Detect to RST and $\overline{RST}$ Transition	t_{RPU}	250	610	1000	ms	4
V_{CC} Slew Rate 4.25V to 4.75V	t_R	0	5		µs	
$\overline{PBRST}$ Stable Low to RST and $\overline{RST}$	t_{PDLY}			20	ms	

NOTES:

1. All voltages referenced to ground.
2. Measured with outputs open.
3. $\overline{PBRST}$ is internally pulled up to V_{CC} with an internal impedance of 10K typical.
4. t_R = 5 µs.
5. $\overline{RST}$ is an open drain output.
6. Must not exceed t_{TD} minimum. See Table 1.
7. RST remains within 0.5V of V_{CC} on power-down until V_{CC} drops below 2.0V. $\overline{RST}$ remains within 0.5V of GND on power-down until V_{CC} drops below 2.0V.
8. Watchdog can not be disabled. It must be strobed to avoid resets.

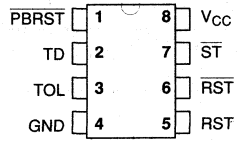
DALLAS SEMICONDUCTOR

DS1232LP/LPS
Low Power MicroMonitor Chip

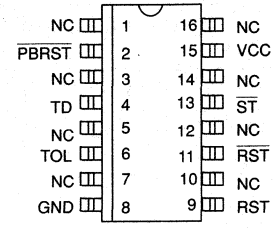
FEATURES

- Super low-power version of DS1232
- 50 µA quiescent current
- Halts and restarts an out-of-control microprocessor
- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Accurate 5% or 10% microprocessor power supply monitoring
- 8-pin DIP or 8-pin SOIC package
- Optional 16-pin SOIC package available
- Industrial temperature -40°C to +85°C available, designated N

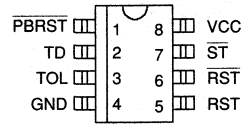
PIN ASSIGNMENT



DS1232LP 8-Pin DIP
(300 Mil)
See Mech. Drawing
Pg. 480



DS1232LPS 16-Pin SOIC
(300 Mil)
See Mech. Drawing
Pg 484



DS1232LPS-2 8-Pin SOIC
(150 Mil)
See Mech. Drawing
Pg 483

PIN DESCRIPTION

$\overline{PBRST}$	–	Pushbutton Reset Input
TD	–	Time Delay Set
TOL	–	Selects 5% or 10% V_{CC} Detect
GND	–	Ground
RST	–	Reset Output (Active High)
$\overline{RST}$	–	Reset Output (Active Low, open drain)
$\overline{ST}$	–	Strobe Input
V_{CC}	–	+5 Volt Power

DESCRIPTION

The DS1232LP/LPS Low Power MicroMonitor Chip monitors three vital conditions for a microprocessor: power supply, software execution, and external override. First, a precision temperature-compensated reference and comparator circuit monitors the status of V_{CC}. When an out-of-tolerance condition occurs, an internal power fail signal is generated which forces reset to the active state. When V_{CC} returns to an in-tolerance condition, the reset signals are kept in the active state for a minimum of 250 ms to allow the power supply and processor to stabilize.

The second function the DS1232LP/LPS performs is pushbutton reset control. The DS1232LP/LPS debounces the pushbutton input and guarantees an active reset pulse width of 250 ms minimum. The third function is a watchdog timer. The DS1232LP/LPS has an internal timer that forces the reset signals to the active state if

the strobe input is not driven low prior to time-out. The watchdog timer function can be set to operate on time-out settings of approximately 150 ms, 600 ms, and 1.2 seconds.

OPERATION - POWER MONITOR

The DS1232LP/LPS detects out-of-tolerance power supply conditions and warns a processor-based system of impending power failure. When V_{CC} falls below a preset level as defined by TOL, the V_{CC} comparator outputs the signals RST and $\overline{RST}$. When TOL is connected to ground, the RST and $\overline{RST}$ signals become active as V_{CC} falls below 4.75 volts. When TOL is connected to V_{CC}, the RST and $\overline{RST}$ signals become active as V_{CC} falls below 4.5 volts. The RST and $\overline{RST}$ are excellent control signals for a microprocessor, as processing is stopped at the last possible moments of valid V_{CC}. On power-up, RST and $\overline{RST}$ are kept active for a minimum of 250 ms to allow the power supply and processor to stabilize.

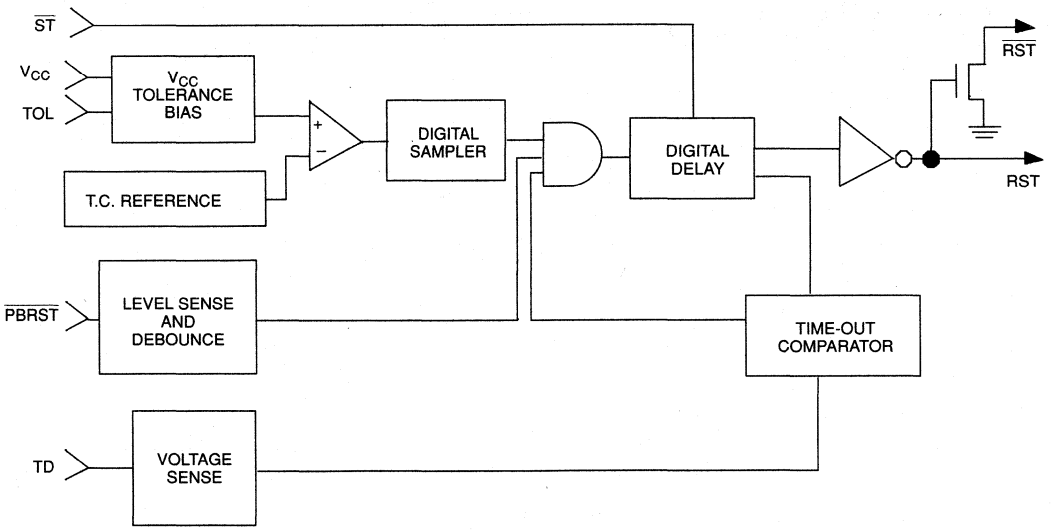
OPERATION - PUSHBUTTON RESET

The DS1232LP/LPS provides an input pin for direct connection to a pushbutton (Figure 1). The pushbutton reset input requires an active low signal. Internally, this input is debounced and timed such that RST and $\overline{RST}$ signals of at least 250 ms minimum are generated. The 250 ms delay starts as the pushbutton reset input is released from low level.

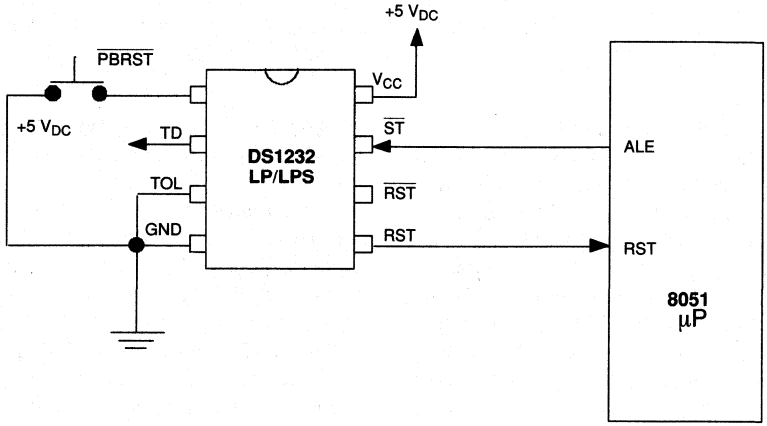
OPERATION - WATCHDOG TIMER

The watchdog timer function forces RST and $\overline{RST}$ signals to the active state when the $\overline{ST}$ input is not stimulated for a predetermined time period. The time period is set by the TD input to be typically 150 ms with TD connected to ground, 600 ms with TD left unconnected, and 1.2 seconds with TD connected to V_{CC}. The watchdog timer starts timing out from the set time period as soon as RST and $\overline{RST}$ are inactive. If a high-to-low transition occurs on the $\overline{ST}$ input pin prior to time-out, the watchdog timer is reset and begins to time-out again. If the watchdog timer is allowed to time-out, then the RST and $\overline{RST}$ signals are driven to the active state for 250 ms minimum. The $\overline{ST}$ input can be derived from microprocessor address signals, data signals, and/or control signals. When the microprocessor is functioning normally, these signals would, as a matter of routine, cause the watchdog to be reset prior to time-out. To guarantee that the watchdog timer does not time-out, a high-to-low transition must occur at or less than the minimum shown in Table 1. A typical circuit example is shown in Figure 2.

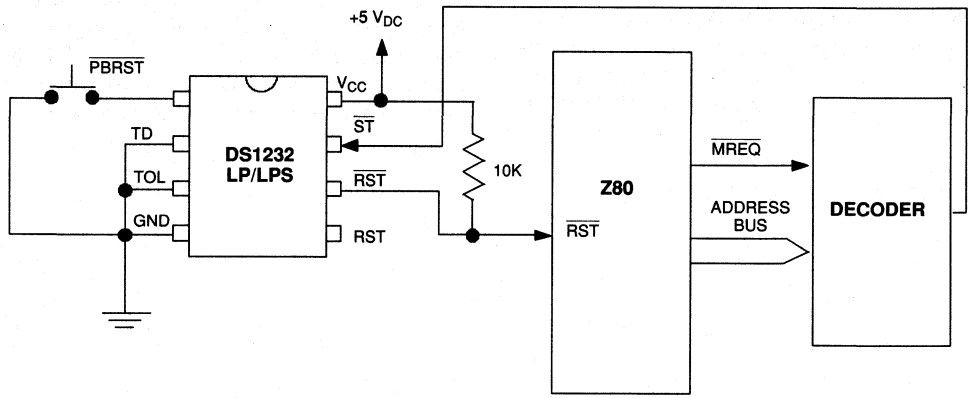
MICROMONITOR BLOCK DIAGRAM



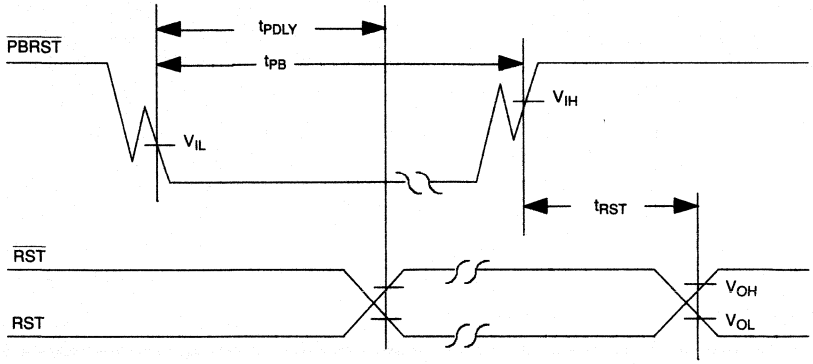
PUSHBUTTON RESET Figure 1



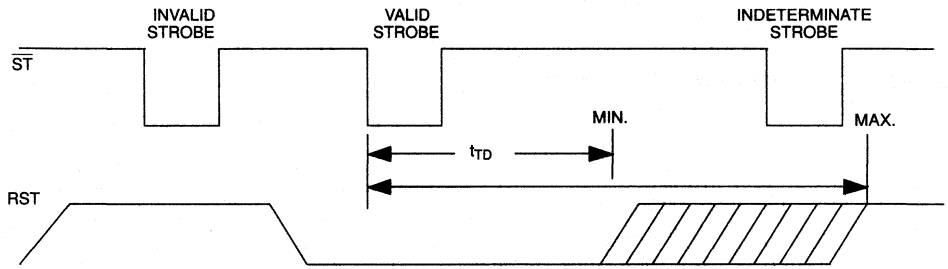
WATCHDOG TIMER Figure 2



TIMING DIAGRAM: PUSHBUTTON RESET Figure 3



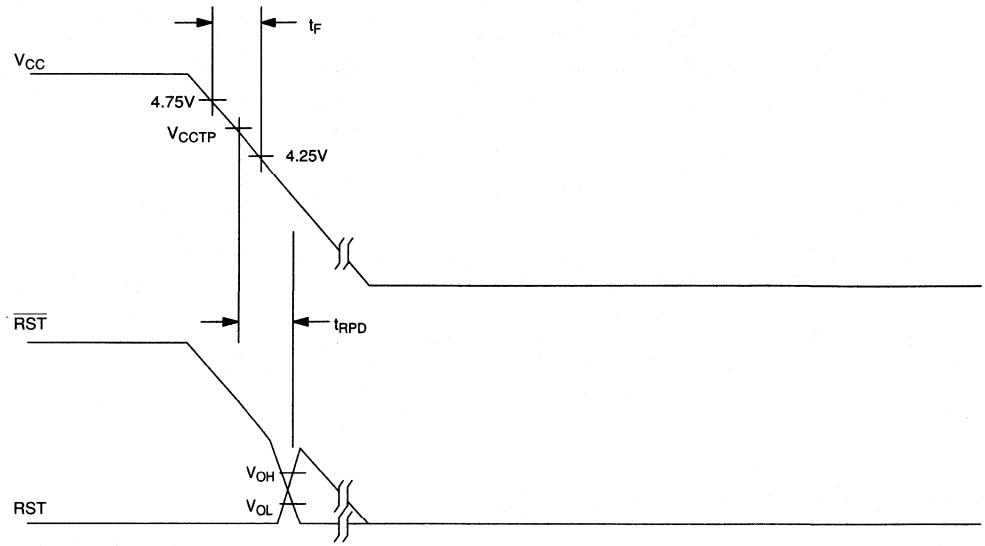
TIMING DIAGRAM: STROBE INPUT Figure 4



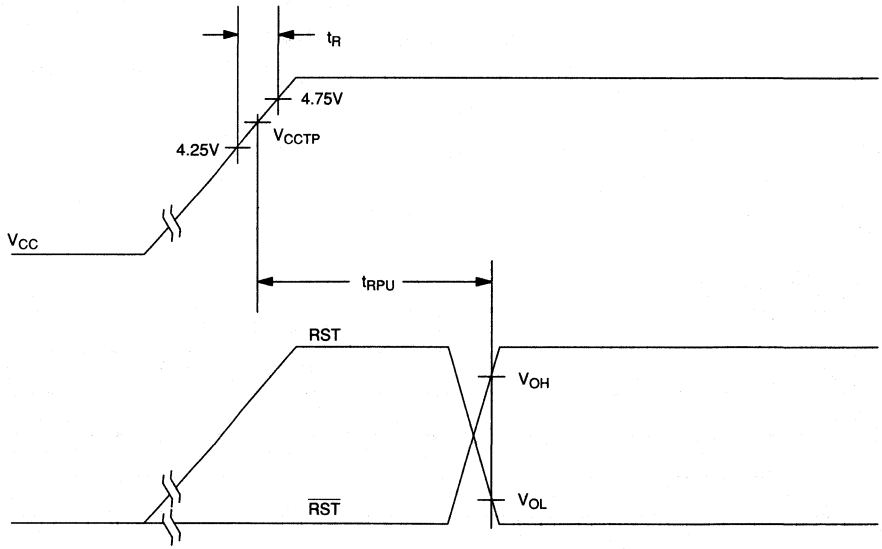
WATCHDOG TIME-OUTS Table 1

TD	TIME-OUT		
	MIN	TYP	MAX
GND	62.5 ms	150 ms	250 ms
Float	250 ms	600 ms	1000 ms
V_{CC}	500 ms	1200 ms	2000 ms

TIMING DIAGRAM: POWER DOWN Figure 5



TIMING DIAGRAM: POWER UP Figure 6



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	-0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	0°C to 70°C
Operating Temperature (Industrial Version)	–40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
$\overline{ST}$ and $\overline{PBRST}$ Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	1
$\overline{ST}$ and $\overline{PBRST}$ Input Low Level	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1.0		+1.0	µA	3
Output Current @ 2.4V	I_{OH}	-8	-10		mA	5
Output Current @ 0.4V	I_{OL}	10			mA	
Low Level @ RST	V_{OL}			0.4	V	1
Output Voltage @ -500 uA	V_{OH}	V_{CC} -0.5V	V_{CC} -0.1V		V	1, 7
Operating Current (CMOS)	I_{CC1}			50	µA	2
Operating Current (TTL)	I_{CC2}		200	500	µA	8
V_{CC} Trip Point (TOL = GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL = V_{CC})	V_{CCTP}	4.25	4.37	4.49	V	1

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{PBRST}$ = V_{IL}	t_{PB}	20			ms	
RESET Active Time	t_{RST}	250	610	1000	ms	
$\overline{ST}$ Pulse Width	t_{ST}	20			ns	6, 9
V_{CC} Fail Detect to RST and $\overline{RST}$	t_{RPD}		50	175	µs	
V_{CC} Slew Rate 4.75V to 4.25V	t_F	300			µs	
V_{CC} Detect to RST and $\overline{RST}$ Inactive	t_{RPU}	250	610	1000	ms	4
V_{CC} Slew Rate 4.25V to 4.75V	t_R	0			ns	
$\overline{PBRST}$ Stable Low to $\overline{RST}$ and RST	t_{PDLY}			20	ms	

NOTES:

1. All voltages referenced to ground.
2. Measured with outputs open and $\overline{ST}$ and $\overline{PBRST}$ within 0.5V of supply rails.
3. $\overline{PBRST}$ is internally pulled up to V_{CC} with an internal impedance of 40K typical.
4. t_R = 5 µs.
5. $\overline{RST}$ is an open drain output.
6. Must not exceed t_{TD} minimum. See Table 1.
7. RST remains within 0.5V of V_{CC} on power-down until V_{CC} drops below 2.0V. $\overline{RST}$ remains within 0.5V of GND on power-down until V_{CC} drops below 2.0V.
8. Measured with outputs open and $\overline{ST}$ and $\overline{PBRST}$ at TTL levels.
9. Watchdog can not be disabled. It must be strobed to avoid resets.

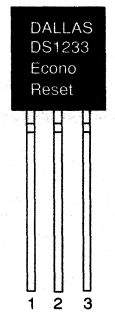
DALLAS SEMICONDUCTOR

DS1233
5V EconoReset

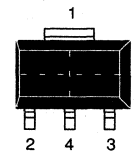
FEATURES

- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Internal circuitry debounces pushbutton switch
- Maintains reset for 350 ms after V_{CC} returns to an in-tolerance condition or pushbutton released
- Accurate 5%, 10% or 15% microprocessor 5V power supply monitoring
- Reduces need for discrete components
- Precision temperature-compensated voltage reference and voltage sensor
- Low-cost TO-92 package or surface mount SOT-223 package
- Internal 5KΩ pull-up resistor
- Operating temperature of –40°C to +85°C

PIN ASSIGNMENT



TO-92 Package
See Mech. Drawing
Pg. 486



SOT-223 Package
See Mech. Drawing
Pg. 490

PIN DESCRIPTION

PIN 1	GROUND
PIN 2	$\overline{\text{RESET}}$
PIN 3	V_{CC}
PIN 4	GROUND (SOT–223 ONLY)

DESCRIPTION

The DS1233 EconoReset monitors two vital conditions for a microprocessor: power supply and external override. A precision temperature compensated reference and comparator circuit are used to monitor the status of the power supply (V_{CC}). When an out-of-tolerance condition is detected, an internal power fail signal is generated which forces reset to the active state. When V_{CC} returns to an in-tolerance condition, the reset signal is kept in the active state for approximately 350 ms to allow the power supply and processor to stabilize. The second function of the DS1233 is pushbutton reset control. The DS1233 debounces a pushbutton closure and will generate a 350 ms reset pulse upon release.

OPERATION - POWER MONITOR

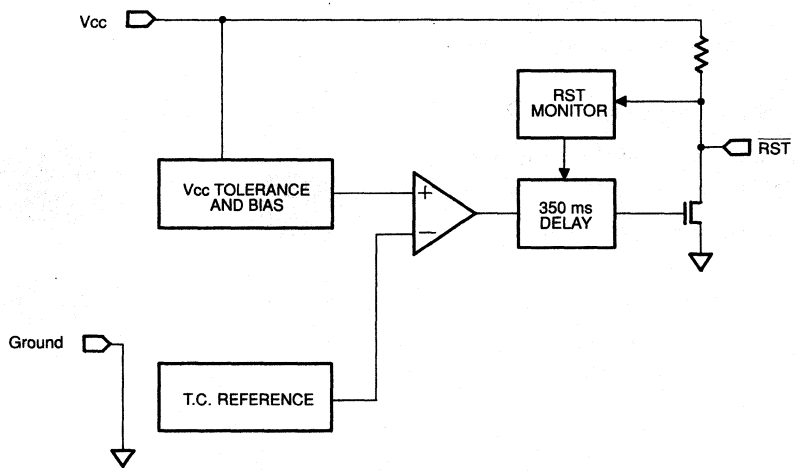
The DS1233 provides the functions of detecting out-of-tolerance power supply conditions and warning a processor-based system of impending power failure. When V_{CC} is detected as out-of-tolerance, as defined by the tolerance of the part selected, the $\overline{RST}$ signal is asserted. On power-up, $\overline{RST}$ is kept active for approximately 350 ms after the power supply has reached the selected tolerance. This allows the power supply and microprocessor to stabilize before $\overline{RST}$ is released.

OPERATION - PUSHBUTTON RESET

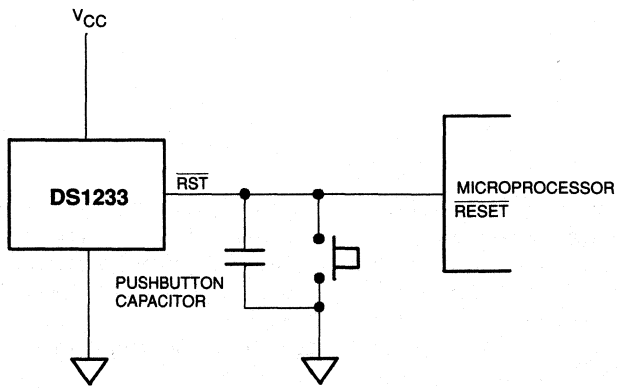
The DS1233 provides for a pushbutton switch to be connected to the $\overline{RST}$ output pin. When the DS1233 is not in a reset cycle, it continuously monitors the $\overline{RST}$ signal for a low going edge. If an edge is detected, the DS1233 will debounce the switch by pulling the $\overline{RST}$ line low. After the internal timer has expired, the DS1233 will continue to monitor the $\overline{RST}$ line. If the line is still low, the DS1233 will continue to monitor the line looking for a rising edge. Upon detecting a release, the DS1233 will force the $\overline{RST}$ line low and hold it low for 350 ms.

NOTE: For proper operation with an external pushbutton, a capacitor between 100 pF and 0.01 µF must be connected between $\overline{RST}$ and ground. In applications where additional reset current is required, a minimum capacitance of 500 pF should be used, along with a parallel external pull-up resistor of 1KΩ minimum.

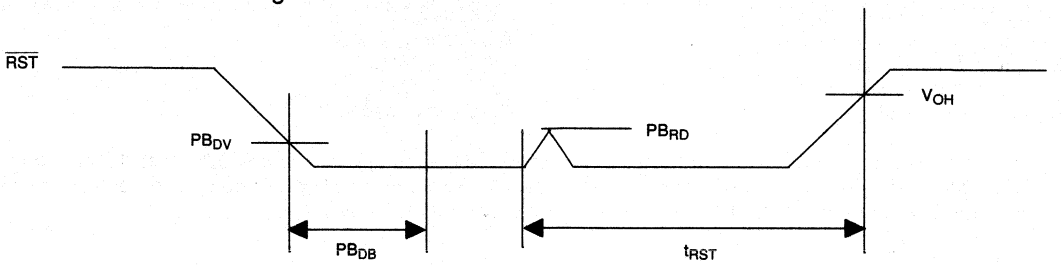
BLOCK DIAGRAM Figure 1



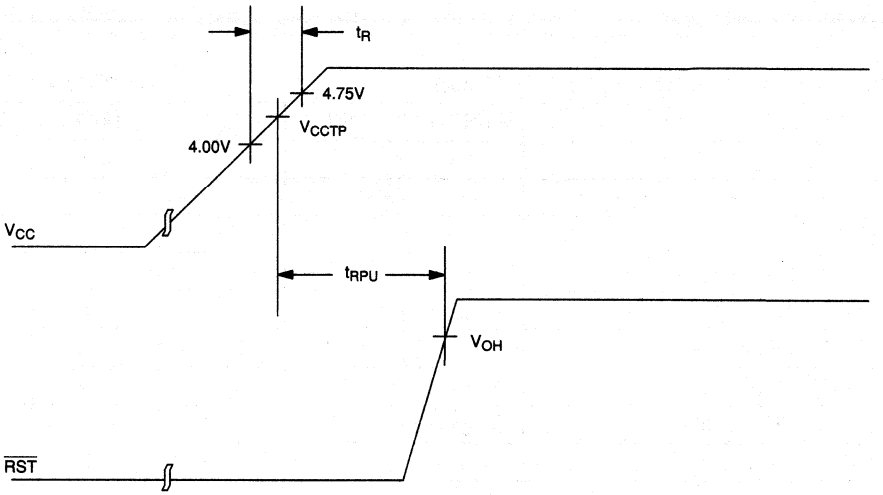
APPLICATION EXAMPLE Figure 2



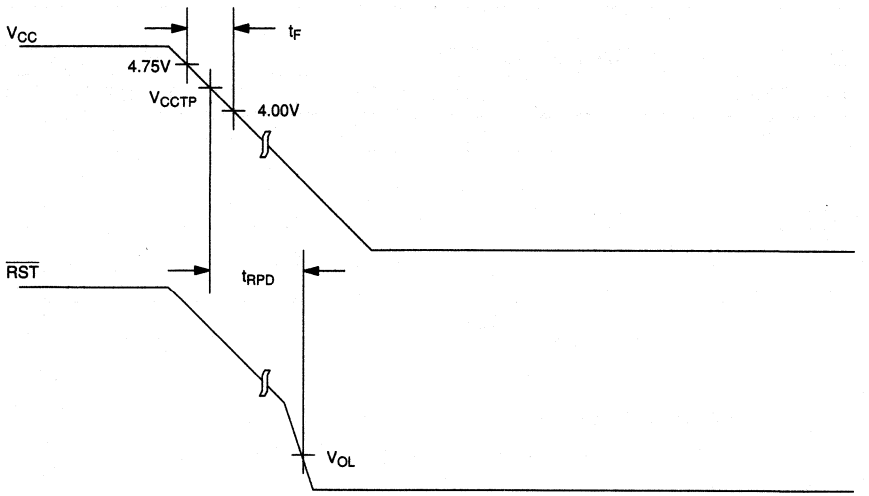
PUSHBUTTON RESET Figure 3



POWER UP Figure 4



POWER DOWN Figure 5



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	-0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	–40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	1.2	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Low Level @ $\overline{RST}$	V_{OL}			0.4	V	1
Output Voltage @ –500 µA	V_{OH}	V_{CC}–0.5V	V_{CC}–0.1V		V	1
Output Current @ 2.4V	I_{OH}		350		µA	
Output Current @ 0.4V	I_{OL}	+10			mA	
Operating Current	I_{CC}			50	µA	
V_{CC} Trip Point 5%	V_{CCTP0}	4.50	4.625	4.75	V	1
V_{CC} Trip Point 10%	V_{CCTP1}	4.25	4.375	4.49	V	1
V_{CC} Trip Point 15%	V_{CCTP2}	4.0	4.125	4.24	V	1
Output Capacitance	C_{OUT}			10	pF	
Pushbutton Detect	PB_{DV}	1.8		3.3	V	1
Pushbutton Release	PB_{RD}		0.3	0.8	V	1,2
Internal Pull-Up Resistor	R_P	3.75	5	6.25	KΩ	

AC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Active Time	t_{RST}	250	350	450	ms	
V_{CC} Detect to $\overline{RST}$	t_{RPD}			100	ns	
V_{CC} Slew Rate (4.75V - 4.00V)	t_F	300			µs	
V_{CC} Slew Rate (4.00V - 4.75V)	t_R	0			ns	
Pushbutton Debounce	PB_{DB}	250	350	450	ms	
V_{CC} detect to RST	t_{RPU}	250	350	450	ms	

NOTES:

1. All voltages are referenced to ground.
2. With a 100 pF to 0.01 µF capacitor connected from $\overline{RST}$ to ground.

ECONORESET SELECTION GUIDE

		VCC TRIP POINT			PUSHBUTTON DETECT		
		MIN	TYP	MAX	MIN	TYP	MAX
5V	DS1233-15	4.0	4.125	4.24	2.4	–	3.3
	DS1233-10	4.25	4.375	4.49	2.4	–	3.3
	DS1233-5	4.5	4.625	4.75	2.4	–	3.3
	DS1233D–15	4.0	4.125	4.24	N/A		N/A
	DS1233D–10	4.25	4.375	4.49	N/A		N/A
	DS1233D–5	4.5	4.625	4.75	N/A		N/A
	DS1833–15	4.0	4.125	4.24	N/A		N/A
	DS1833–10	4.25	4.375	4.49	N/A		N/A
	DS1833–5	4.5	4.625	4.75	N/A		N/A
3.3V	DS1233A-15	2.64	2.72	2.80	1.8	–	3.0
	DS1233A-10	2.8	2.88	2.97	1.8	–	3.0

PRELIMINARY

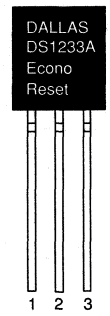
DALLAS SEMICONDUCTOR

DS1233A
3.3V EconoReset

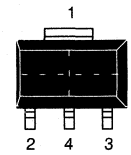
FEATURES

- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Internal circuitry debounces pushbutton switch
- Maintains reset for 350 ms after V_{CC} returns to an in-tolerance condition or pushbutton released
- Accurate 10% or 15% microprocessor 3.3V power supply monitoring
- Reduces need for discrete components
- Precision temperature-compensated voltage reference and voltage sensor
- Low-cost TO-92 package or surface mount SOT-223 package
- Internal 5KΩ pull-up resistor
- Operating temperature of –40°C to +85°C

PIN ASSIGNMENT



TO-92 Package
See Mech. Drawing
Pg. 486



SOT-223 Package
See Mech. Drawing
Pg. 490

PIN DESCRIPTION

PIN 1	GROUND
PIN 2	$\overline{\text{RESET}}$
PIN 3	V_{CC}
PIN 4	GROUND (SOT–223 ONLY)

DESCRIPTION

The DS1233A EconoReset monitors two vital conditions for a microprocessor: power supply and external override. A precision temperature compensated reference and comparator circuit are used to monitor the status of the power supply (V_{CC}). When an out-of-tolerance condition is detected, an internal power fail signal is generated which forces reset to the active state. When V_{CC} returns to an in-tolerance condition, the reset signal is kept in the active state for approximately 350 ms to allow the power supply and processor to stabilize. The second function of the DS1233A is pushbutton reset control. The DS1233A debounces a pushbutton closure and will generate a 350 ms reset pulse upon release.

OPERATION – POWER MONITOR

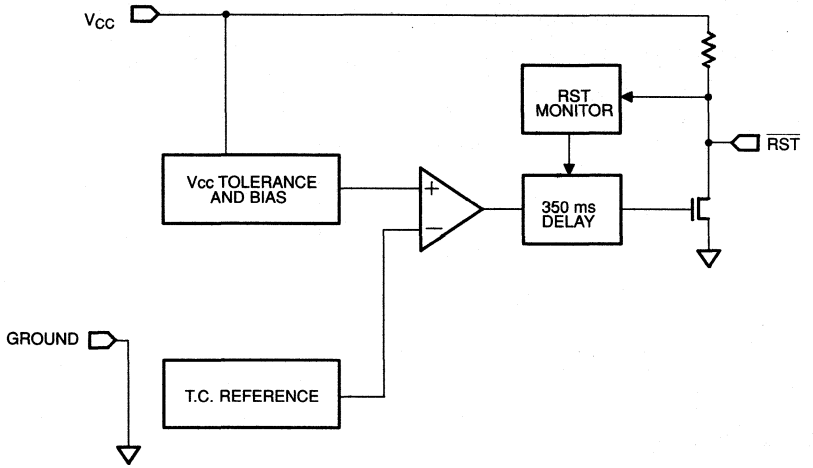
The DS1233A provides the functions of detecting out-of-tolerance power supply conditions and warning a processor-based system of impending power failure. When V_{CC} is detected as out-of-tolerance, as defined by the tolerance of the part selected, the $\overline{RST}$ signal is asserted. On power-up, $\overline{RST}$ is kept active for approximately 350 ms after the power supply has reached the selected tolerance. This allows the power supply and microprocessor to stabilize before $\overline{RST}$ is released.

OPERATION – PUSHBUTTON RESET

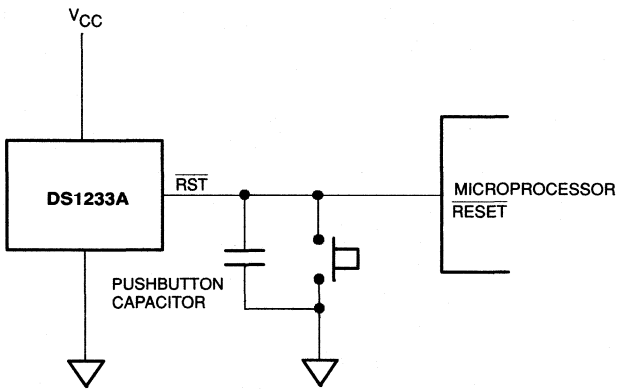
The DS1233A provides for a pushbutton switch to be connected to the $\overline{RST}$ output pin. When the DS1233A is not in a reset cycle, it continuously monitors the $\overline{RST}$ signal for a low going edge. If an edge is detected, the DS1233A will debounce the switch by pulling the $\overline{RST}$ line low. After the internal timer has expired, the DS1233A will continue to monitor the $\overline{RST}$ line. If the line is still low, the DS1233A will continue to monitor the line looking for a rising edge. Upon detecting a release, the DS1233A will force the $\overline{RST}$ line low and hold it low for 350 ms.

NOTE: For proper operation with an external pushbutton, a capacitor between 100 pF and 0.01 µF must be connected between $\overline{RST}$ and ground. In applications where additional reset current is required, a minimum capacitance of 500 pF should be used, along with a parallel external pull-up resistor of 1KΩ minimum.

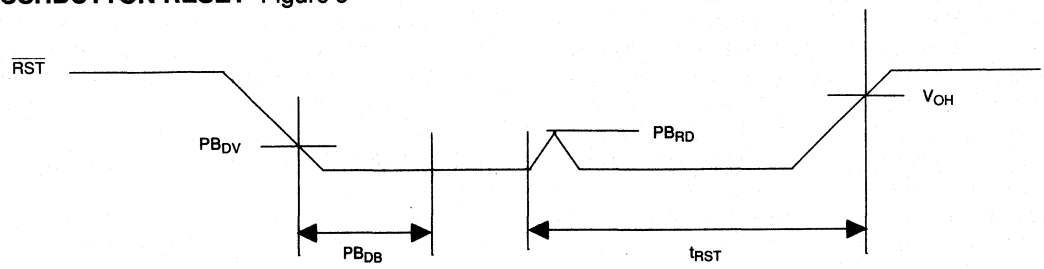
BLOCK DIAGRAM Figure 1



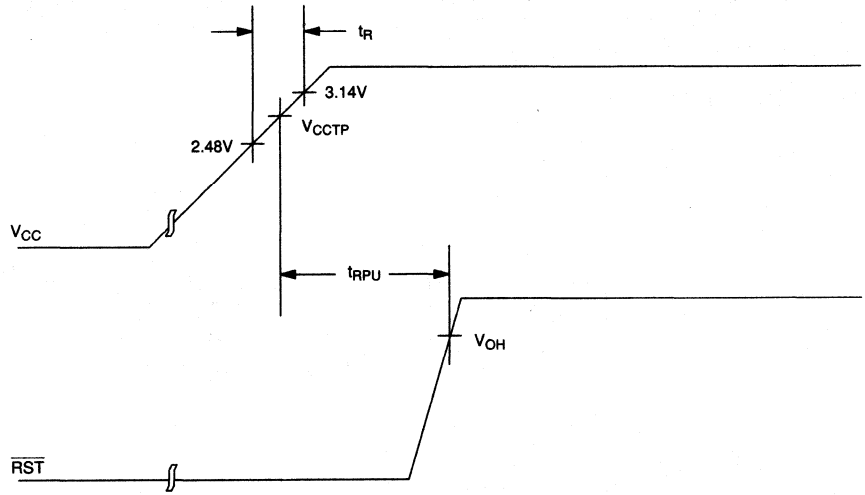
APPLICATION EXAMPLE Figure 2



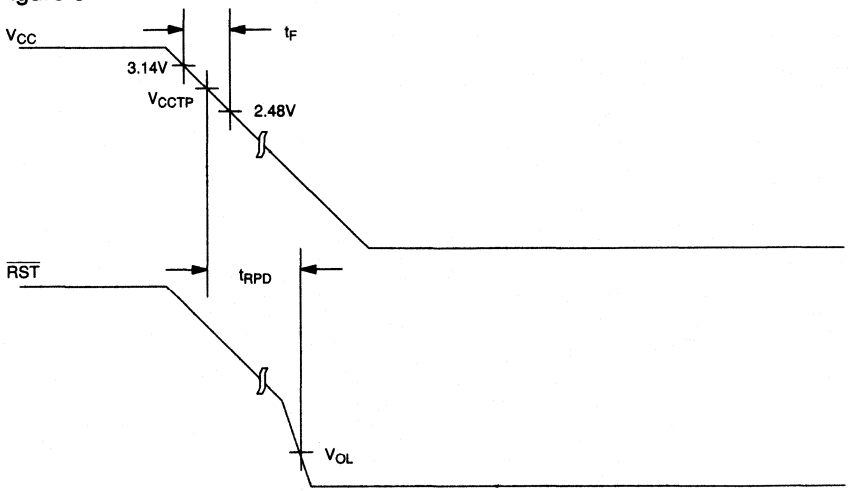
PUSHBUTTON RESET Figure 3



POWER UP Figure 4



POWER DOWN Figure 5



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	–0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	–40°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	1.2	3.3	5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{DD} = 3.3V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Low Level @ $\overline{RST}$	V_{OL}			0.4	V	1
Output Voltage @ –500 µA	V_{OH}	V_{CC}–0.5V	V_{CC}–0.1V		V	1
Output Current @ 2.4V	I_{OH}		350		µA	
Output Current @ 0.4V	I_{OL}	+10			mA	
Operating Current	I_{CC}			50	µA	
V_{CC} Trip Point 10%	V_{CCTP1}	2.80	2.88	2.97	V	1
V_{CC} Trip Point 15%	V_{CCTP2}	2.64	2.72	2.80	V	1
Output Capacitance	C_{OUT}			10	pF	
Pushbutton Detect	PB_{DV}	.8		2.0	V	1
Pushbutton Release	PB_{RD}		0.3	0.8	V	1,2
Internal Pull-Up Resistor	R_P	3.75	5	6.25	KΩ	

AC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC} = 3.3V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Active Time	t_{RST}	250	350	450	ms	
V_{CC} Detect to $\overline{RST}$	t_{RPD}			100	ns	
V_{CC} Slew Rate (2.85V – 2.3V)	t_F	300			µs	
V_{CC} Slew Rate (2.3V – 2.85V)	t_R	0			ns	
Pushbutton Debounce	PB_{DB}	250	350	450	ms	
V_{CC} detect to RST	t_{RPU}	250	350	450	ms	

NOTES:

1. All voltages are referenced to ground.
2. With a 100 pF to 0.01 µF capacitor connected from $\overline{RST}$ to ground.

ECONORESET SELECTION GUIDE

		VCC TRIP POINT			PUSHBUTTON DETECT		
		MIN	TYP	MAX	MIN	TYP	MAX
5V	DS1233-15	4.0	4.125	4.24	2.4	–	3.3
	DS1233-10	4.25	4.375	4.49	2.4	–	3.3
	DS1233-5	4.5	4.625	4.75	2.4	–	3.3
	DS1233D–15	4.0	4.125	4.24	N/A		N/A
	DS1233D–10	4.25	4.375	4.49	N/A		N/A
	DS1233D–5	4.5	4.625	4.75	N/A		N/A
	DS1833–15	4.0	4.125	4.24	N/A		N/A
	DS1833–10	4.25	4.375	4.49	N/A		N/A
	DS1833–5	4.5	4.625	4.75	N/A		N/A
3.3V	DS1233A-15	2.64	2.72	2.80	1.8	–	3.0
	DS1233A-10	2.8	2.88	2.97	1.8	–	3.0

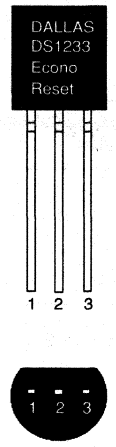
DALLAS SEMICONDUCTOR

DS1233D
5V EconoReset

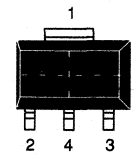
FEATURES

- Automatically restarts microprocessor after power failure
- Maintains reset for 350 ms after V_{CC} returns to an in-tolerance condition
- Accurate 5%, 10% or 15% microprocessor 5V power supply monitoring
- Reduces need for discrete components
- Precision temperature-compensated voltage reference and voltage sensor
- Low-cost TO-92 package or surface mount SOT-223 package
- Internal 5 KΩ pull-up resistor
- Compatible with Motorola 68XXX series and HC16 Microprocessors
- Operating temperature of –40°C to +85°C

PIN ASSIGNMENT



TO-92 Package
See Mech. Drawing
Pg. 486



SOT-223 Package
See Mech. Drawing
Pg. 490

PIN DESCRIPTION

PIN 1	GROUND
PIN 2	$\overline{\text{RESET}}$
PIN 3	V_{CC}
PIN 4	GROUND (SOT–223 ONLY)

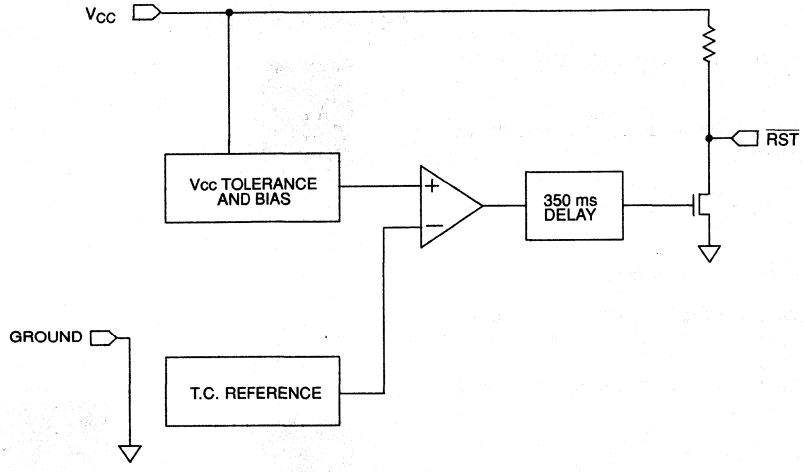
DESCRIPTION

The DS1233D EconoReset uses a precision temperature compensated reference and comparator circuit to monitor the status of the power supply (V_{CC}). When an out-of-tolerance condition is detected, an internal power fail signal is generated which forces reset to the active state. When V_{CC} returns to an in-tolerance condition, the reset signal is kept in the active state for approximately 350 ms to allow the power supply and processor to stabilize.

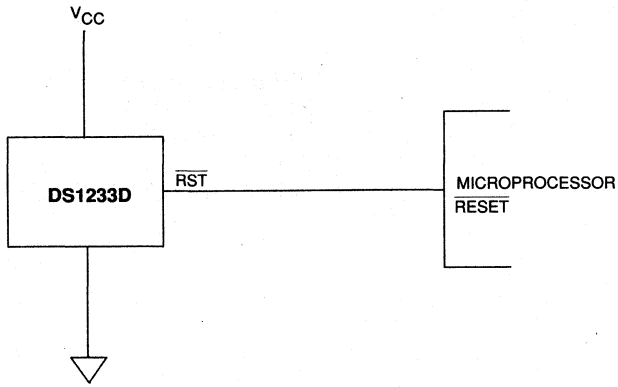
OPERATION - POWER MONITOR

The DS1233D provides the functions of detecting out-of-tolerance power supply conditions and warning a processor-based system of impending power failure. When V_{CC} is detected as out-of-tolerance, as defined by the tolerance of the part selected, the $\overline{RST}$ signal is asserted. On power-up, $\overline{RST}$ is kept active for approximately 350 ms after the power supply has reached the selected tolerance. This allows the power supply and microprocessor to stabilize before $\overline{RST}$ is released.

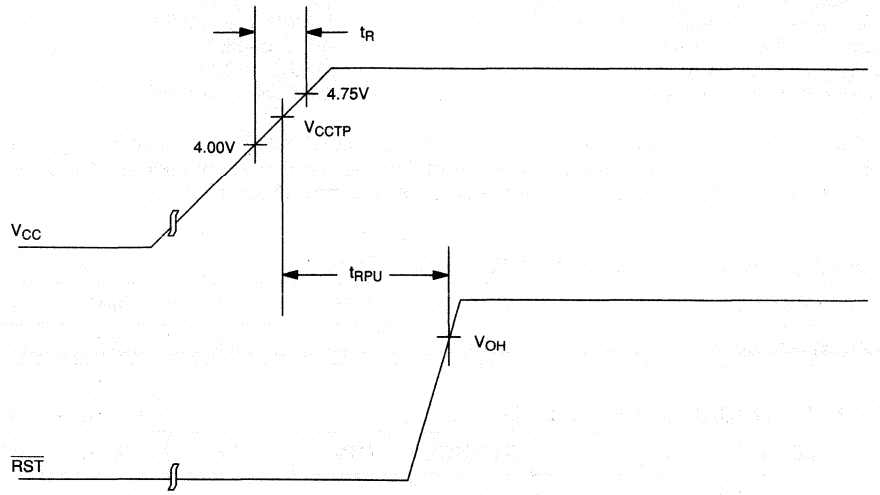
BLOCK DIAGRAM Figure 1



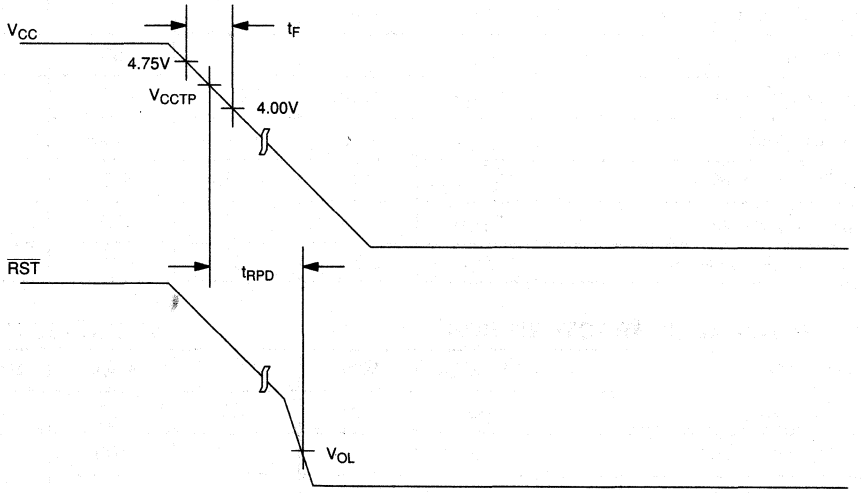
APPLICATION EXAMPLE Figure 2



POWER UP Figure 3



POWER DOWN Figure 4



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	-0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	–40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	1.2	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Low Level @ $\overline{RST}$	V_{OL}			0.4	V	1
Output Voltage @ –500 µA	V_{OH}	V_{CC}–0.5V	V_{CC}–0.1V		V	1
Output Current @ 2.4V	I_{OH}		350		µA	
Output Current @ 0.4V	I_{OL}	+10			mA	2
Operating Current	I_{CC}			50	µA	
V_{CC} Trip Point 5%	V_{CCTP1}	4.5	4.625	4.74	V	1
V_{CC} Trip Point 10%	V_{CCTP2}	4.25	4.375	4.49	V	1
V_{CC} Trip Point 15%	V_{CCTP3}	4.0	4.125	4.24	V	1
Output Capacitance	C_{OUT}			10	pF	
Internal Pull-Up Resistor	R_P	3.75	5	6.25	KΩ	

AC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Active Time	t_{RST}	250	350	450	ms	
V_{CC} Detect to $\overline{RST}$	t_{RPD}			100	ns	
V_{CC} Slew Rate (4.75V - 4.00V)	t_F	300			µs	
V_{CC} Slew Rate (4.00V - 4.75V)	t_R	0			ns	
V_{CC} detect to RST	t_{RPU}	250	350	450	ms	

NOTES:

1. All voltages are referenced to ground.
2. A 1KΩ external resistor may be required for proper operation of the microprocessor reset control circuit.

ECONORESET SELECTION GUIDE

		VCC TRIP POINT			PUSHBUTTON DETECT		
		MIN	TYP	MAX	MIN	TYP	MAX
5V	DS1233-15	4.0	4.125	4.24	2.4	–	3.3
	DS1233-10	4.25	4.375	4.49	2.4	–	3.3
	DS1233-5	4.5	4.625	4.75	2.4	–	3.3
	DS1233D–15	4.0	4.125	4.24	N/A		N/A
	DS1233D–10	4.25	4.375	4.49	N/A		N/A
	DS1233D–5	4.5	4.625	4.75	N/A		N/A
	DS1833–15	4.0	4.125	4.24	N/A		N/A
	DS1833–10	4.25	4.375	4.49	N/A		N/A
	DS1833–5	4.5	4.625	4.75	N/A		N/A
3.3V	DS1233A-15	2.64	2.72	2.80	1.8	–	3.0
	DS1233A-10	2.8	2.88	2.97	1.8	–	3.0

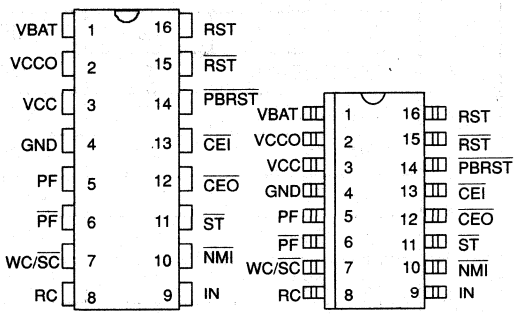
DALLAS SEMICONDUCTOR

DS1236
MicroManager Chip

FEATURES

- Holds microprocessor in check during power transients
- Halts and restarts an out-of-control microprocessor
- Monitors pushbutton for external override
- Warns microprocessor of an impending power failure
- Converts CMOS SRAM into nonvolatile memory
- Unconditionally write protects memory when power supply is out of tolerance
- Consumes less than 100 nA of battery current at 25°C
- Controls external power switch for high current applications
- Accurate 10% power supply monitoring
- Optional 5% power supply monitoring designated DS1236-5
- Provides orderly shutdown in nonvolatile microprocessor applications
- Supplies necessary control for low-power "stop mode" in battery operated hand-held applications
- Standard 16-pin DIP or space-saving 16-pin SOIC
- Optional industrial temperature range -40°C to +85°C

PIN ASSIGNMENT



16-Pin DIP (300 Mil.)
See Mech. Drawing
Pg. 480

16-Pin SOIC (300 Mil.)
See Mech. Drawing
Pg. 484

PIN DESCRIPTION

V_{BAT}	–	+3 Volt Battery Input
V_{CCO}	–	Switched SRAM Supply Output
V_{CC}	–	+5 Volt Power Supply Input
GND	–	Ground
PF	–	Power Fail (Active High)
$\overline{PF}$	–	Power Fail (Active Low)
WC/$\overline{SC}$	–	Wake-Up Control (Sleep)
RC	–	Reset Control
IN	–	Early Warning Input
$\overline{NMI}$	–	Non-Maskable Interrupt
$\overline{ST}$	–	Strobe Input
$\overline{CEO}$	–	Chip Enable Output
$\overline{CEI}$	–	Chip Enable Input
$\overline{PBRST}$	–	Pushbutton Reset Input
$\overline{RST}$	–	Reset Output (Active Low)
RST	–	Reset Output (Active High)

DESCRIPTION

The DS1236 MicroManager Chip provides all the necessary functions for power supply monitoring, reset control, and memory backup in microprocessor-based systems. A precise internal voltage reference and comparator circuit monitor power supply status. When an out-of-tolerance condition occurs, the microprocessor reset and power fail outputs are forced active, and static RAM control unconditionally write protects external memory. The DS1236 also provides early warning detection of a user-defined threshold by driving a non-maskable interrupt. External reset control is provided by a pushbutton reset input which is debounced and activates reset outputs. An internal watchdog timer can also force the reset outputs to the active state if the strobe input is not driven low prior to watchdog time-out. Reset control and wake-up/sleep control inputs also provide the necessary signals for orderly shutdown and start-up in battery backup and battery operated applications. A block diagram of the DS1236 is shown in Figure 1.

PIN DESCRIPTION

PIN NAME	DESCRIPTION
V_{BAT}	+3V battery input provides nonvolatile operation of control functions.
V_{CCO}	V_{CC} output for nonvolatile SRAM applications.
V_{CC}	+5V primary power input.
PF	Power fail indicator, active high, used for external power switching as shown in Figure 9.
$\overline{PF}$	Power fail indicator, active low.
WC/$\overline{SC}$	Wake-up and Sleep control. Invokes low-power mode.
RC	Reset control input. Determines reset output . Normally low for NMOS processors and high for battery-backed CMOS processors.
IN	Early warning power fail input. This voltage sense point can be tied (via resistor divider) to a user-selected voltage.
$\overline{NMI}$	Non-maskable interrupt. Used in conjunction with the IN pin to indicate an impending power failure.
$\overline{ST}$	Strobe input. A high-to-low transition will reset the watchdog timer, indicating that software is still in control.
$\overline{CEO}$	Chip enable output. Used with nonvolatile SRAM applications.
$\overline{CEI}$	Chip enable input.
$\overline{PBRST}$	Pushbutton reset input.
$\overline{RST}$	Active low reset output.
RST	Active high reset output.

PROCESSOR MODE

A distinction is often made between CMOS and NMOS processor systems. In a CMOS system, power consumption may be a concern, and nonvolatile operation is possible by battery backing both the SRAM and the CMOS processor. All resources would be maintained in the absence of V_{CC}. A power-down reset is not issued since the low-power mode of most CMOS processors (Stop) is terminated with a Reset. A pulsed interrupt ($\overline{NMI}$) is issued to allow the CMOS processor to invoke a sleep mode to save power. For this case, a power-on reset is desirable to wake up and initialize the processor. The CMOS mode is invoked by connecting RC to V_{CCO}.

An NMOS processor consumes more power, and consequently may not be battery backed. In this case, it is desirable to notify the processor of a power fail, then keep it in reset during the loss of V_{CC}. This avoids intermittent or aberrant operation. On power-up, the processor will continue to be reset until V_{CC} reaches an operational level to provide an orderly start. The NMOS mode is invoked by connecting RC to ground.

POWER MONITOR

The DS1236 employs a band gap voltage reference and a precision comparator to monitor the 5-volt supply (V_{CC}) in microprocessor-based systems. When an out-of-tolerance condition occurs, the RST and $\overline{RST}$ outputs are driven to the active state. Th e V_{CC} trip point (V_{CCTP}) is set for 10% operation so that the RST and $\overline{RST}$ outputs will become active as V_{CC} falls below 4.5 volts (4.37 typical). The V_{CCTP} for the 5% operation option (DS1236-5) is set for 4.75 volts (4.62 typical). The RST and $\overline{RST}$ signals are excellent for microprocessor reset control, as processing is stopped at the last possible moment of in-tolerance V_{CC}. On power-up, the RST and $\overline{RST}$ signals are held active for a minimum of 25 ms (100 ms typical) after V_{CCTP} is reached to allow the power supply and microprocessor to stabilize. Note: The operation described above is obtained with the reset control pin (RC) connected to GND (NMOS mode). Please review the reset control section for more information.

WATCHDOG TIMER

The DS1236 provides a watchdog timer function which forces the RST and $\overline{RST}$ signals to the active state when the strobe input ($\overline{ST}$) is not stimulated for a predetermined time period. This time period is 400 ms typically with a maximum time-out of 600 ms. The watchdog time-out period begins as soon as RST and $\overline{RST}$ are inactive. If a high-to-low transition occurs at the $\overline{ST}$ input prior to time-out, the watchdog timer is reset and begins to time out again. The $\overline{ST}$ input timing is shown in Figure 2. To guarantee the watchdog timer does not time out, a high-to-low transition on $\overline{ST}$ must occur at or less than 100 ms (minimum time-out) from a reset. If the watchdog timer is allowed to time out, the RST and $\overline{RST}$ outputs are driven to the active state for 25 ms minimum. The $\overline{ST}$ input can be derived from microprocessor address, data, and/or control signals. Under normal operating conditions, these signals would routinely reset the watchdog timer prior to time-out. If the watchdog timer is not required, two methods have been provided to disable it.

Permanently grounding the IN pin in the CMOS mode (RC=1) will disable the watchdog. In normal operation with RC=1, the watchdog is disabled as soon as the IN pin is below V_{TP}. With IN grounded, an $\overline{NMI}$ output will occur only at power-up, or when the $\overline{ST}$ pin is strobed. As shown in the Figure 3, a falling edge on $\overline{ST}$ will generate an $\overline{NMI}$ when IN is below V_{TP}. This allows the processor to verify that power is between V_{TP} and V_{CCTP}, as an $\overline{NMI}$ will be returned immediately after the $\overline{ST}$ strobe. The watchdog timer is not affected by the IN pin when in NMOS mode (RC=0).

If the $\overline{NMI}$ signal is required to monitor supply voltages, the watchdog may also be disabled by leaving the $\overline{ST}$ input open. Independent of the state of the RC pin, the watchdog is also disabled as soon as V_{CC} falls to V_{CCTP}.

PUSHBUTTON RESET

An input pin is provided on the DS1236 for direct connection to a pushbutton. The pushbutton reset input requires an active low signal. Internally, this input is pulled high by a 10K resistor whenever V_{CC} is greater than V_{BAT}. The $\overline{PBRST}$ pin is also debounced and timed such that the RST and $\overline{RST}$ outputs are driven to the active state for 25 ms minimum. This 25 ms delay begins as the pushbutton is released from a low level. A typical example of the power monitor, watchdog timer, and pushbutton reset connections are shown in Figure 4. The $\overline{PBRST}$ input is disabled whenever the IN pin voltage level is less than V_{TP} and the reset control (RC) is tied high (CMOS mode). The $\overline{PBRST}$ input is also disabled whenever V_{CC} is below V_{BAT}. Timing of the $\overline{PBRST}$-generated RST is illustrated in Figure 5.

NON-MASKABLE INTERRUPT

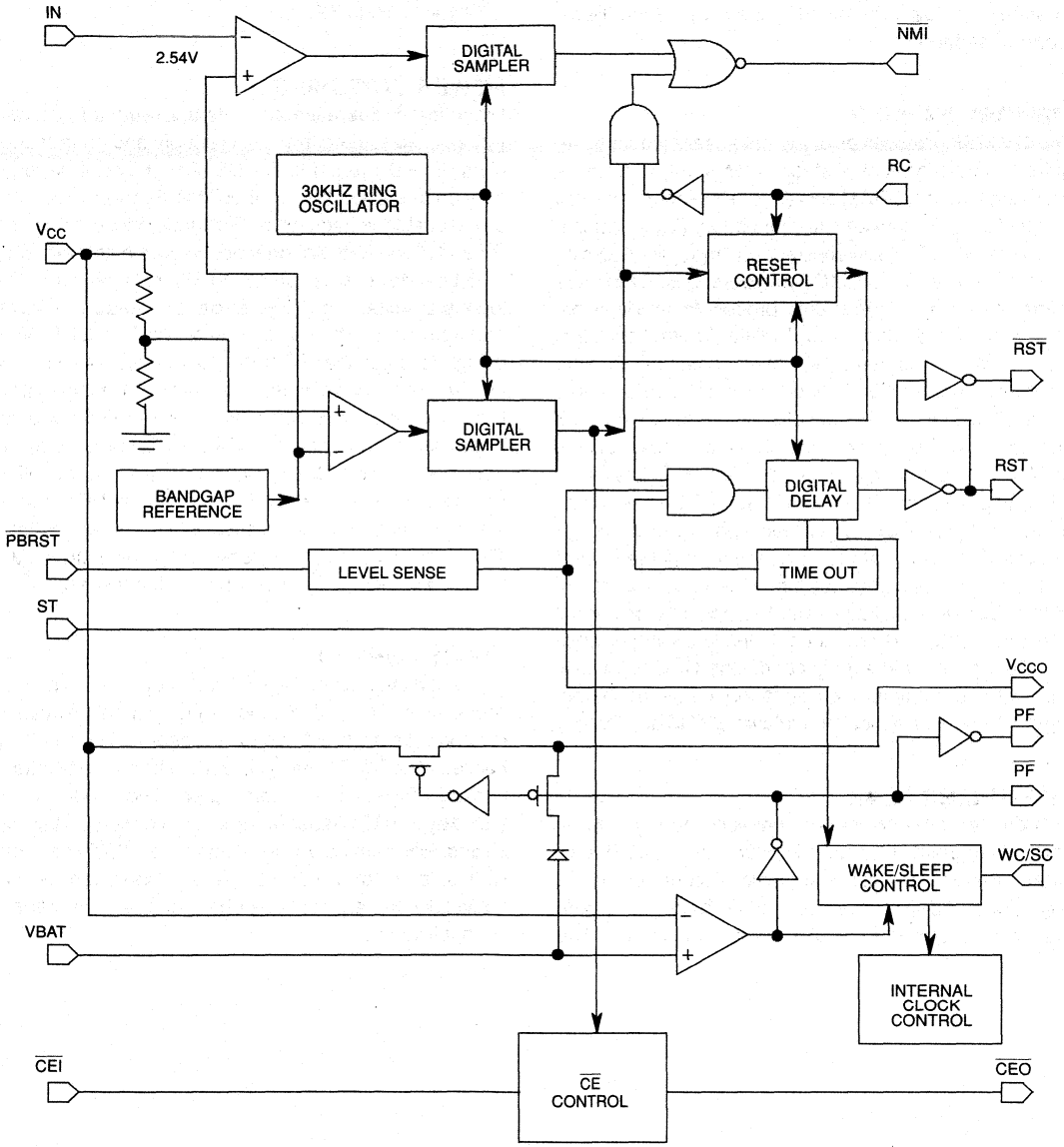
The DS1236 generates a non-maskable interrupt $\overline{NMI}$ for early warning of power failure to a microprocessor. A precision comparator monitors the voltage level at the IN pin relative to a reference generated by the internal band gap. The IN pin is a high impedance input allowing for a user-defined sense point. An external resistor voltage divider network (Figure 6) is used to interface with high voltage signals. This sense point may be derived from the regulated 5-volt supply or from a higher DC voltage level closer to the main system power input. Since the IN trip point V_{TP} is 2.54 volts, the proper values for R1 and R2 can be determined by the equation as shown in Figure 6. Proper operation of the DS1236 requires that the voltage at the IN pin be limited to V_{IN}. Therefore, the maximum allowable voltage at the supply being monitored (V_{MAX}) can also be derived as shown in Figure 6. A simple approach to solving this equation is to select a value for R2 high enough to keep power consumption low, and solve for R1. The flexibility of the IN input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time for microprocessor shut-down between $\overline{NMI}$ and RST or $\overline{RST}$.

When the supply being monitored decays to the voltage sense point, the DS1236 pulses the $\overline{NMI}$ output to the active state for a minimum of 200 µs. The $\overline{NMI}$ power fail detection circuitry also has built-in time domain hysteresis. That is, the monitored supply is sampled periodically at a rate determined by an internal ring oscillator running at approximately 30 KHz (33 µs/cycle). Three consecutive samplings of out-of-tolerance supply (below V_{SENSE}) must occur at the IN pin to activate $\overline{NMI}$. Therefore, the supply must be below the voltage sense point for approximately 100 µs or the comparator will reset. In this way, power supply noise is removed from the monitoring function, preventing false trips. During a power-up , any IN pin levels below V_{TP} are disabled from reaching the $\overline{NMI}$ pin until V_{CC} rises to V_{CCTP}. As a result, any potential $\overline{NMI}$ pulse will not be initiated until V_{CC} reaches V_{CCTP}.

Removal of an active low level on the $\overline{NMI}$ pin is controlled by either an internal time-out (when IN pin is less than V_{TP}) or by the subsequent rise of the IN pin above

V_{TP}. The initiation and removal of the $\overline{NMI}$ signal during power-up results in an $\overline{NMI}$ pulse of from 0 µs minimum to 500 µs maximum, depending on the relative voltage relationship between V_{CC} and the IN pin voltage. As an example, when the IN pin is tied to ground during power-up, the internal time-out will result in a pulse of 200 µs minimum to 500 µs maximum. In contrast, if the IN pin is tied to V_{CCO} during power-up, $\overline{NMI}$ will not produce a pulse on power-up. Note that a fast slewing power supply may cause the $\overline{NMI}$ to be virtually non-existent on power-up. This is of no consequence, however, since a RST will be active.

DS1236 FUNCTIONAL BLOCK DIAGRAM Figure 1



If the IN pin is connected to V_{CCO}, the $\overline{NMI}$ output will pulse low as V_{CC} decays to V_{CCTP} in the NMOS mode (RC=0). In the CMOS mode (RC=V_{CCO}) the power-down of V_{CC} out-of-tolerance at V_{CCTP} will not produce a pulse on the $\overline{NMI}$ pin. Given that any $\overline{NMI}$ pulse has been completed by the time V_{CC} decays to V_{CCTP}, the $\overline{NMI}$ pin will remain high. The $\overline{NMI}$ voltage will follow V_{CC} down until V_{CC} decays to V_{BAT}. Once V_{CC} decays to V_{BAT}, the $\overline{NMI}$ pin will either remain at V_{OHL} or enter tri-state mode as determined by the RC pin (see "Reset Control" section).

MEMORY BACKUP

The DS1236 provides all of the necessary functions required to battery back a static RAM. First, a switch is provided to direct SRAM power from the incoming 5 volt supply (V_{CC}) or from an external battery (V_{BAT}), whichever is greater. This switched supply (V_{CCO}) can also be used to battery back a CMOS microprocessor. For more information about nonvolatile processor applications, review the "Reset Control" and "Wake Control" sections. Second, the same power fail detection described in the power monitor section is used to hold the chip enable output ($\overline{CEO}$) to within 0.3 volts of V_{CC} or to within 0.7 volts of V_{BAT}. This write protection mechanism occurs as V_{CC} falls below V_{CCTP} as specified. If $\overline{CEI}$ is low at the time power fail detection occurs, $\overline{CEO}$ is held in its present state until $\overline{CEI}$ is returned high, or the period t_{CE} expires. This delay of write protection until the current memory cycle is completed prevents the corruption of data. If $\overline{CEO}$ is in an inactive state at the time of V_{CC} fail detection, $\overline{CEO}$ will be unconditionally disabled within t_{CF}. During nominal supply conditions $\overline{CEO}$ will follow $\overline{CEI}$ with a maximum propagation delay of 20 ns. Figure 7 shows a typical nonvolatile SRAM application.

FRESHNESS SEAL

In order to conserve battery capacity during storage and/or shipment of an end system, the DS1236 provides a freshness seal to electrically disconnect the battery. Figure 8 depicts the three pulses below ground on the IN pin required to invoke the freshness seal. The freshness seal will be disconnected and normal operation will begin when V_{CC} is cycled and reapplied to a level above V_{BAT}.

To prevent negative pulses associated with noise from setting the freshness mode in system applications, a series diode and resistor can be used to shunt noise to ground. During manufacturing, the freshness seal can still be set by holding TP2 at -3 volts while applying the 0 to -3 volt clock to TP1.

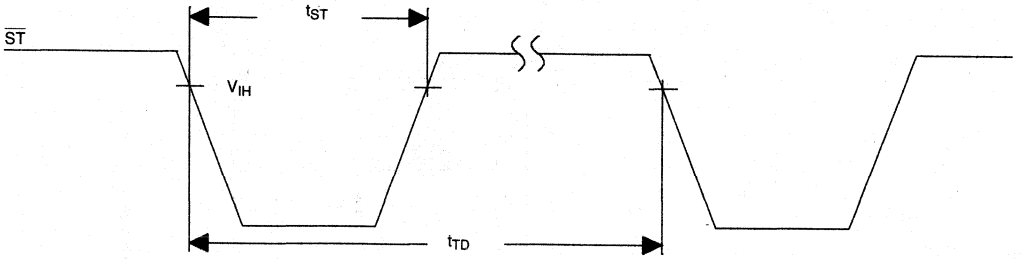
POWER SWITCHING

When larger operating currents are required in a battery-backed system, the 5-volt supply and battery supply switches internal to the DS1236 may not be large enough to support the required load through V_{CCO} with a reasonable voltage drop. For these applications, the PF and $\overline{PF}$ outputs are provided to gate external power switching devices. As shown in Figure 9, power to the load is switched from V_{CC} to battery on power-down, and from battery to V_{CC} on power- up. The DS1336 is designed to use the $\overline{PF}$ output to switch between V_{BAT} and V_{CC}. It provides better leakage and switchover performance than currently available discrete components. The transition threshold for PF and $\overline{PF}$ is set to the external battery voltage V_{BAT}, allowing a smooth transition between sources. The load applied to the PF pin from the external switch will be supplied by the battery. Therefore, if a discrete switch is used, this load should be taken into consideration when sizing the battery.

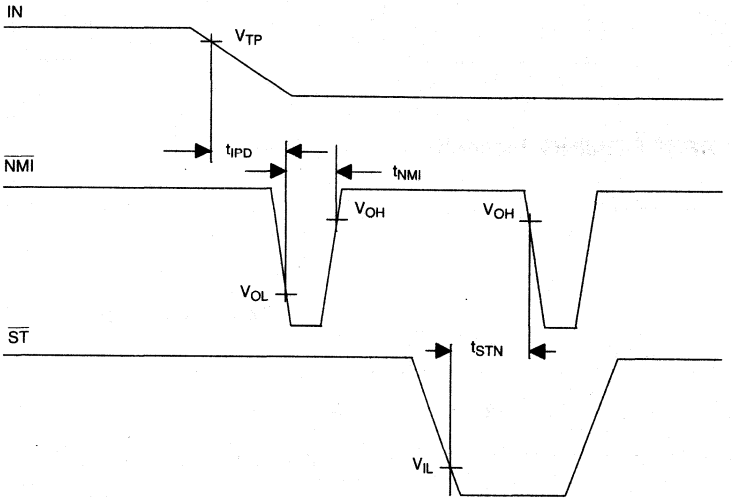
RESET CONTROL

As mentioned above, the DS1236 supports two modes of operation. The CMOS mode is used when the system incorporates a CMOS microprocessor which is battery backed. The NMOS mode is used when a non-battery backed processor is incorporated. The mode is selected by the RC (Reset Control) pin. The level of this pin distinguishes timing and level control on RST, $\overline{RST}$, and $\overline{NMI}$ outputs for volatile processor operation versus nonvolatile battery backup or battery-operated processor applications.

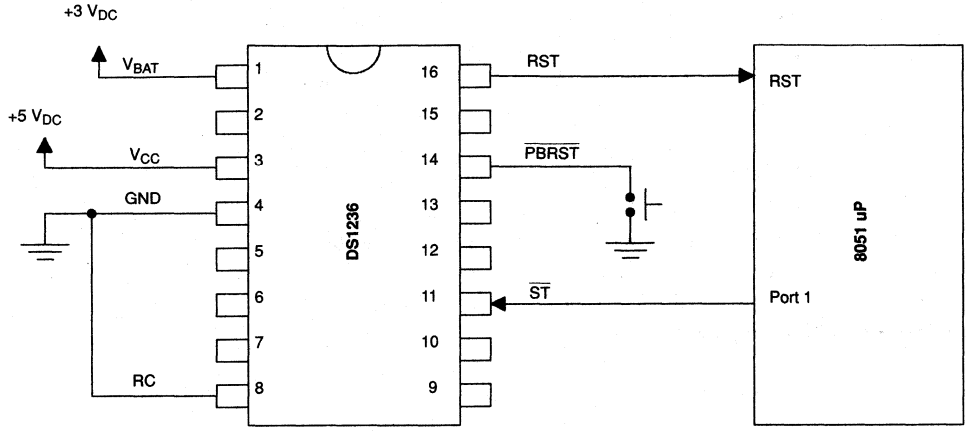
ST/INPUT TIMING Figure 2



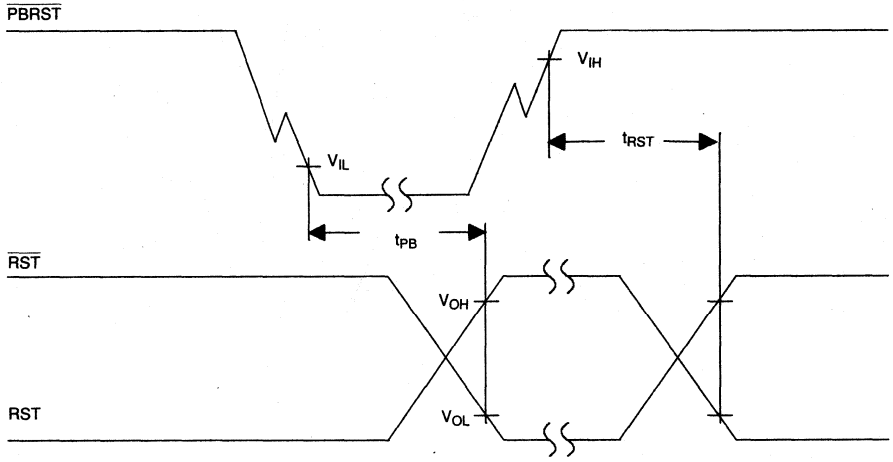
NMI/FROM ST/INPUT Figure 3



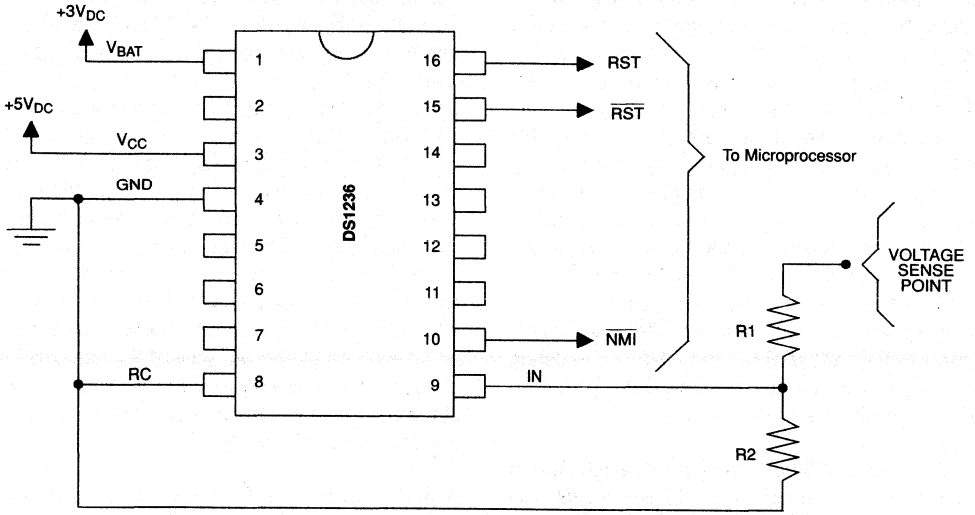
POWER MONITOR, WATCHDOG Figure 4



PUSH BUTTON RESET TIMING Figure 5



NON-MASKABLE INTERRUPT Figure 6



EXAMPLE 1: 5 VOLT SUPPLY, R2 = 10K OHM, V_{SENSE} = 4.80 VOLTS

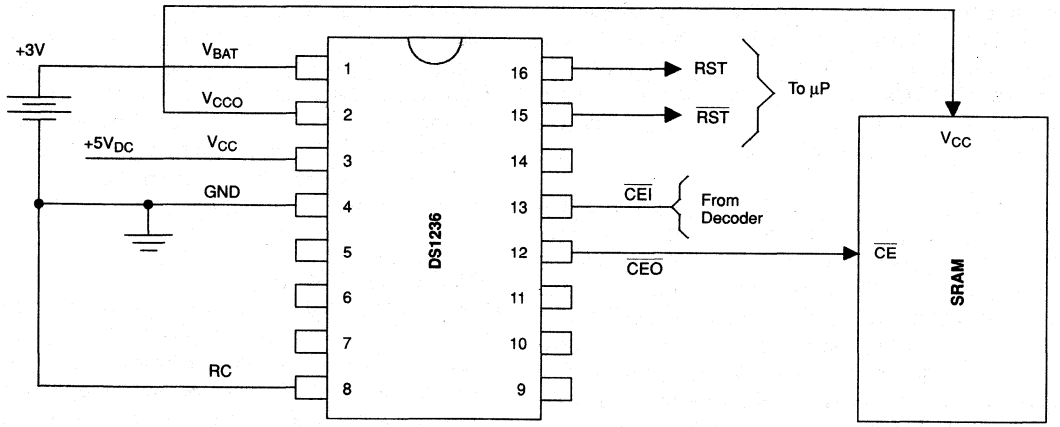
$$\therefore 4.80 = \frac{R1 + 10K}{10K} \times 2.54 \qquad R1 = 8.9K\ OHM$$

EXAMPLE 2: 12 VOLT SUPPLY, R2 = 10K OHM, V_{SENSE} = 9.00 VOLTS

$$\therefore 9.00 = \frac{R1 + 10K}{10K} \times 2.54 \qquad R1 = 25.4K\ OHM$$

$$V_{MAX} = \frac{9.00}{2.54} \times 5.00 = 17.7\ VOLTS$$

NONVOLATILE SRAM Figure 7



When the RC pin is tied to ground, the DS1236 is designed to interface with NMOS processors which do not have the microamp currents required during a battery backed mode. Grounding the RC pin does, however, continue to support nonvolatile backup of system SRAM memory. Nonvolatile systems incorporating NMOS processors generally require that only the SRAM memory and/or timekeeping functions be battery backed. When the processor is not battery backed (RC = 0), all signals connected from the processor to the DS1236 are disconnected from the backup battery supply, or grounded when system V_{CC} decays below V_{BAT}. In the NMOS processor system, the principal emphasis is placed on giving early warnings with $\overline{NMI}$, then providing a continuously active RST and $\overline{RST}$ signal during power-down while isolating the backup battery from the processor during a loss of V_{CC}.

During power-down, $\overline{NMI}$ will pulse low for a minimum of 200 µs, and then return high. If RC is tied low (NMOS mode), the voltage on $\overline{NMI}$ will follow V_{CC} until V_{CC} supply decays to V_{BAT}, at which point $\overline{NMI}$ will enter tri-state (see timing diagram). Also, upon V_{CC} out-of-tolerance at V_{CCTP}, the RST and $\overline{RST}$ outputs are driven active and RST will follow V_{CC} as the supply decays. On power-up, RST follows V_{CC} up, $\overline{RST}$ is held low, and both remain active for t_{RST} after valid V_{CC}. During a power-up from a V_{CC} voltage below V_{BAT}, any detected IN pin levels below V_{TP} are disabled from reaching the $\overline{NMI}$ pin until V_{CC} rises to V_{CCTP}. As a result, any potential $\overline{NMI}$ pulse will not be initiated until V_{CC} reaches V_{CCTP}. Removal of an active low level on the $\overline{NMI}$ pin is controlled by either an internal time-out (when the IN pin is less than V_{TP}), or by the subsequent rise of the IN pin above V_{TP}. The initiation and removal of the $\overline{NMI}$ signal results in an $\overline{NMI}$ pulse of 0 µs minimum to 500 µs maximum during power-up, depending on the relative voltage relationship between V_{CC} and the IN pin. As an example, when the IN pin is tied to ground, the internal time-out will result in a pulse of 200 µs minimum to 500 µs maximum. In contrast, if the IN pin is tied to V_{CCO}, $\overline{NMI}$ will not produce a pulse on power-up.

Connecting the RC pin to a high (V_{CCO}) invokes CMOS mode and provides nonvolatile support to both the system SRAM as well as a low power CMOS processor. When using CMOS microprocessors, it is possible to place the microprocessor into a very low- power mode termed the "stop" or "halt" mode. In this state the CMOS processor requires only microamp currents and is fully capable of being battery backed. This mode generally allows the CMOS microprocessor to maintain the contents of internal RAM as well as state control of I/O ports during battery backup. The processor can subsequently be restarted by any of several different signals. To maintain this low-power state, the DS1236 issues no $\overline{NMI}$ and/or reset signals to the processor until it is time to bring the processor back into full operation. To support the low-power processor battery backed mode (RC = 1), the DS1236 provides a pulsed $\overline{NMI}$ for early power failure warning. Waiting to initiate a Stop mode until after the $\overline{NMI}$ pin has returned high will guarantee the processor that no other active $\overline{NMI}$ or RST/$\overline{RST}$ will be issued by the DS1236 until one of two conditions occurs: 1) Voltage on the pin rises above V_{TP}, which activates the watchdog, or 2) V_{CC} cycles below then above V_{BAT}, which also results in an active RST and $\overline{RST}$. If V_{CC} does not fall below V_{CCTP}, the processor will be restarted by the reset derived from the watchdog timer as the IN pin rises above V_{TP}.

With the RC pin tied to V_{CCO}, RST and $\overline{RST}$ are not forced active as V_{CC} collapses to V_{CCTP}. The $\overline{RST}$ is held at a high level via the external battery as V_{CC} falls below battery potential. This mode of operation is intended for applications in which the processor is made nonvolatile with an external source, and allows the processor to power down into a Stop mode as signaled from $\overline{NMI}$ at an earlier voltage level. The $\overline{NMI}$ output pin will pulse low for t_{NMI} following a low voltage detect at the IN pin of V_{TP}. Following t_{NMI}, however, $\overline{NMI}$ will also be held at a high level (V_{BAT}) by the battery as V_{CC} decays below V_{BAT}. On power-up, RST and $\overline{RST}$ are held inactive until V_{CC} reaches V_{BAT}, then RST and $\overline{RST}$ are driven active for t_{RST}. If the IN pin falls below V_{TP} during an active reset, the reset outputs will be forced inactive by the $\overline{NMI}$ output. In addition, as long as the IN pin is less than V_{TP}, stimulation of the $\overline{ST}$ pin will result in additional $\overline{NMI}$ pulses. In this way, the $\overline{ST}$ pin can be used to allow the CMOS processor to determine if the supply voltage, as monitored by the IN pin, is above or below a selected operating value. This is illustrated in Figure 3. As discussed above, the RC pin determines the timing relationships and levels of several signals. The following section describes the power-up and power-down timing diagrams in more detail.

TIMING DIAGRAMS

This section provides a description of the timing diagrams shown in Figure 10, Figure 11, Figure 12, and Figure 13. These diagrams show the relative timing and levels in both the NMOS and the CMOS mode for power-up and down. Figure 10 illustrates the relationship for

power-down in CMOS mode. As V_{CC} falls, the IN pin voltage drops below V_{TP}. As a result, the processor is notified of an impending power failure via an active $\overline{NMI}$, which allows it to enter a sleep mode. As the power falls further, V_{CC} crosses V_{CCTP}, the power monitor trip point. Since the DS1236 is in CMOS mode, no reset is generated. The $\overline{RST}$ voltage will follow V_{CC} down, but will fall no further than V_{BAT}. At this time, $\overline{CEO}$ is brought high to write protect the RAM. When the V_{CC} reaches V_{BAT}, a power fail is issued via the PF and $\overline{PF}$ pins.

Figure 11 illustrates operation of the power-down sequence in NMOS mode. Once again, as power falls, an $\overline{NMI}$ is issued. This gives the processor time to save critical data in nonvolatile SRAM. When V_{CC} reaches V_{CCTP}, an active RST and $\overline{RST}$ are given. The RST voltage will follow V_{CC} as it falls. $\overline{CEO}$, PF, and $\overline{PF}$ will operate in a similar manner to CMOS mode. Notice that the $\overline{NMI}$ will tri-state to prevent a loss of battery power.

Figure 12 shows the power-up sequence for the NMOS mode. As V_{CC} slews above V_{BAT}, the PF and $\overline{PF}$ pins are deactivated. An active reset occurs as well as an $\overline{NMI}$. Although the $\overline{NMI}$ may be short due to slew rates, reset will be maintained for the standard t_{RST} time-out period. At a later time, if the IN pin falls below V_{TP}, a new $\overline{NMI}$ will occur. If the processor does not issue a $\overline{ST}$, a watchdog reset will also occur. The second $\overline{NMI}$ and RST are provided to illustrate these possibilities.

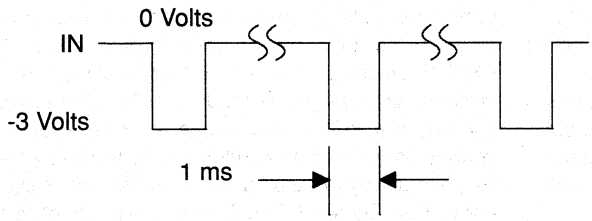
Figure 13 illustrates the power-up timing for CMOS mode. The principal difference is that the DS1236 issues a reset immediately in the NMOS mode. In CMOS mode, a reset is issued when IN rises above V_{TP}. Depending on the processor type, the $\overline{NMI}$ may terminate the Stop mode in the processor.

WAKE CONTROL/SLEEP CONTROL

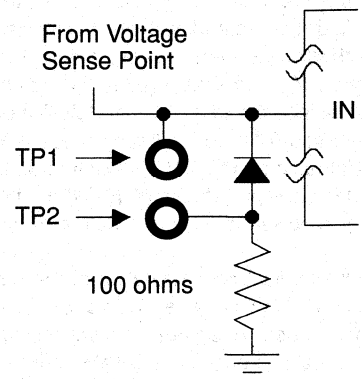
The Wake/Sleep Control input (WC/$\overline{SC}$) allows the processor to disable all comparators on the DS1236 before entering the Stop mode. This feature allows the DS1236, processor, and static RAM to maintain nonvolatility in the lowest power mode possible. The processor may invoke the sleep mode in battery-operated applications to conserve battery capacity when an absence of activity is detected. The operation of this signal is shown in Figure 14. The DS1236 may subsequently be restarted by a high-to-low transition on the $\overline{PBRST}$ input through human interface via a keyboard, touchpad, etc. The processor will then be restarted as the watchdog times out and drives RST and $\overline{RST}$ active. The DS1236 can also be started up by forcing the WC/$\overline{SC}$ pin high from an external source. Also, if the DS1236 is placed in a sleep mode by the processor and system power is lost, the DS1236 will wake up the next time V_{CC} rises above V_{BAT}. These possibilities are illustrated in Figure 15.

When the sleep mode is invoked during normal power-valid conditions, all operation on the DS1236 is disabled, thus leaving the $\overline{NMI}$, RST, and $\overline{RST}$ outputs disabled as well as the $\overline{ST}$ and IN inputs. However, a loss of power during a sleep mode will result in an active RST and $\overline{RST}$ when the RC pin is grounded (NMOS mode). If the RC pin is tied high, the RST and $\overline{RST}$ pins will remain inactive during power-down in a sleep mode. Removal of the sleep mode by the $\overline{PBRST}$ input is not affected by the IN pin threshold at V_{TP} when the RC pin is tied high (CMOS mode). Subsequent power-up of the V_{CC} supply with the RC pin tied high will activate the RST and $\overline{RST}$ outputs as the main supply rises above V_{BAT}. A high-to-low transition on the WC/$\overline{SC}$ pin must follow a high-to-low transition on the ST pin by t_{WC} to invoke a Sleep mode for the DS1236.

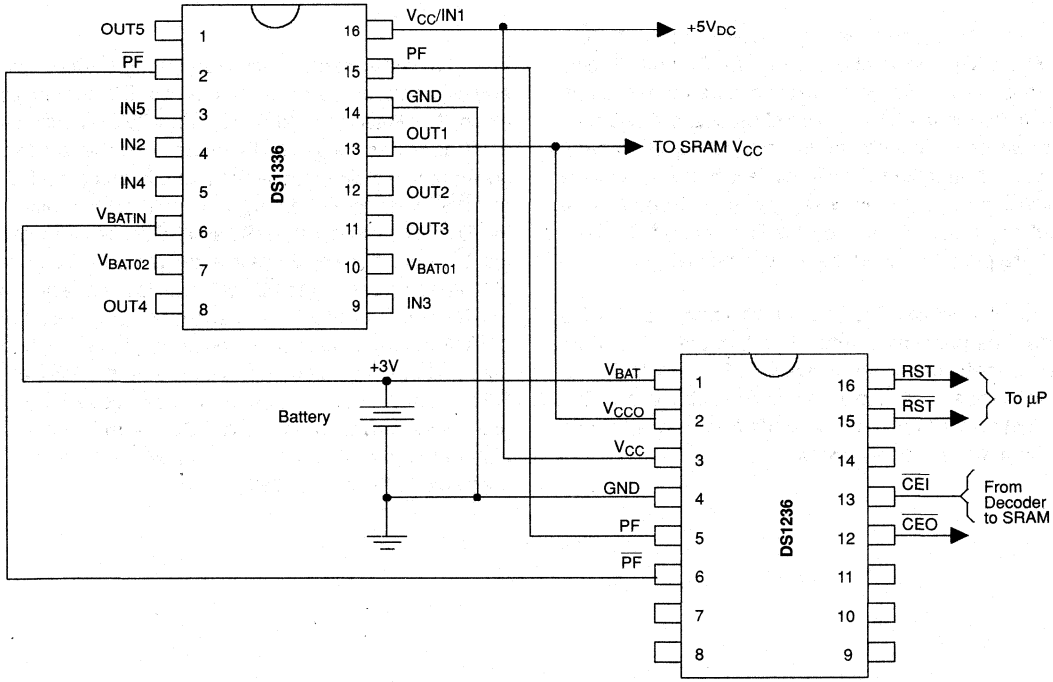
FRESHNESS SEAL Figure 8



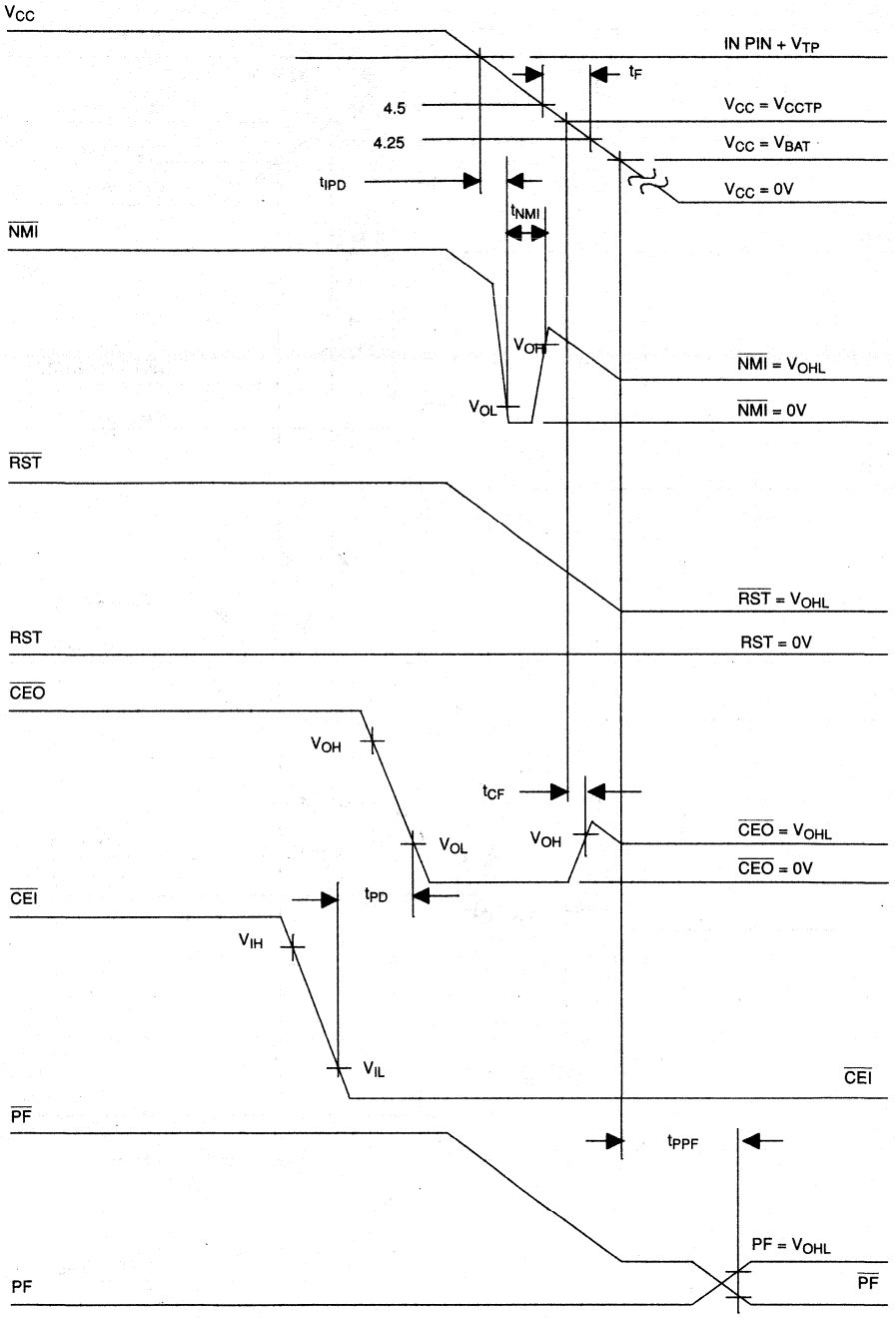
Note: This series of pulses must be applied during normal +5 volt operation.



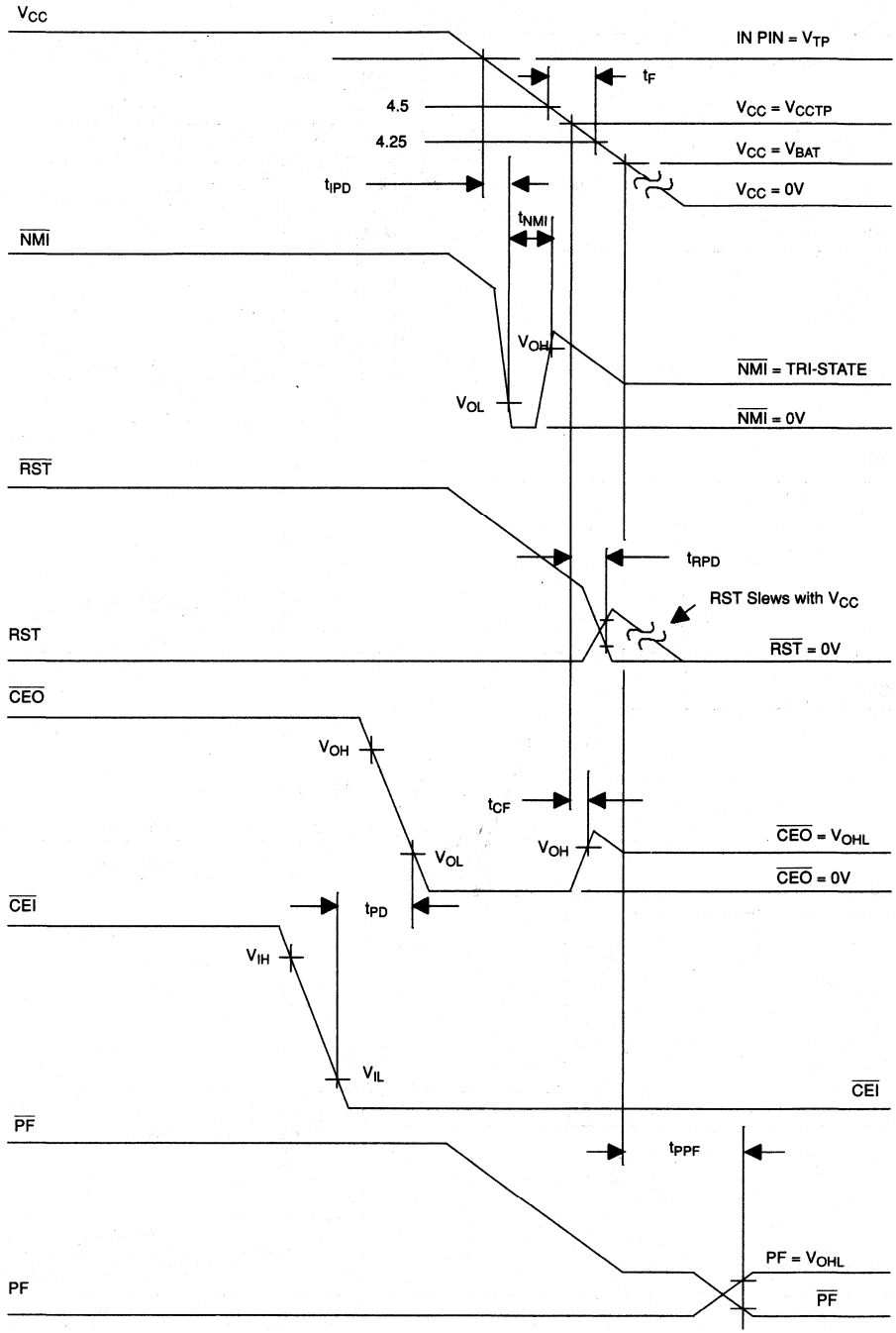
POWER SWITCHING Figure 9



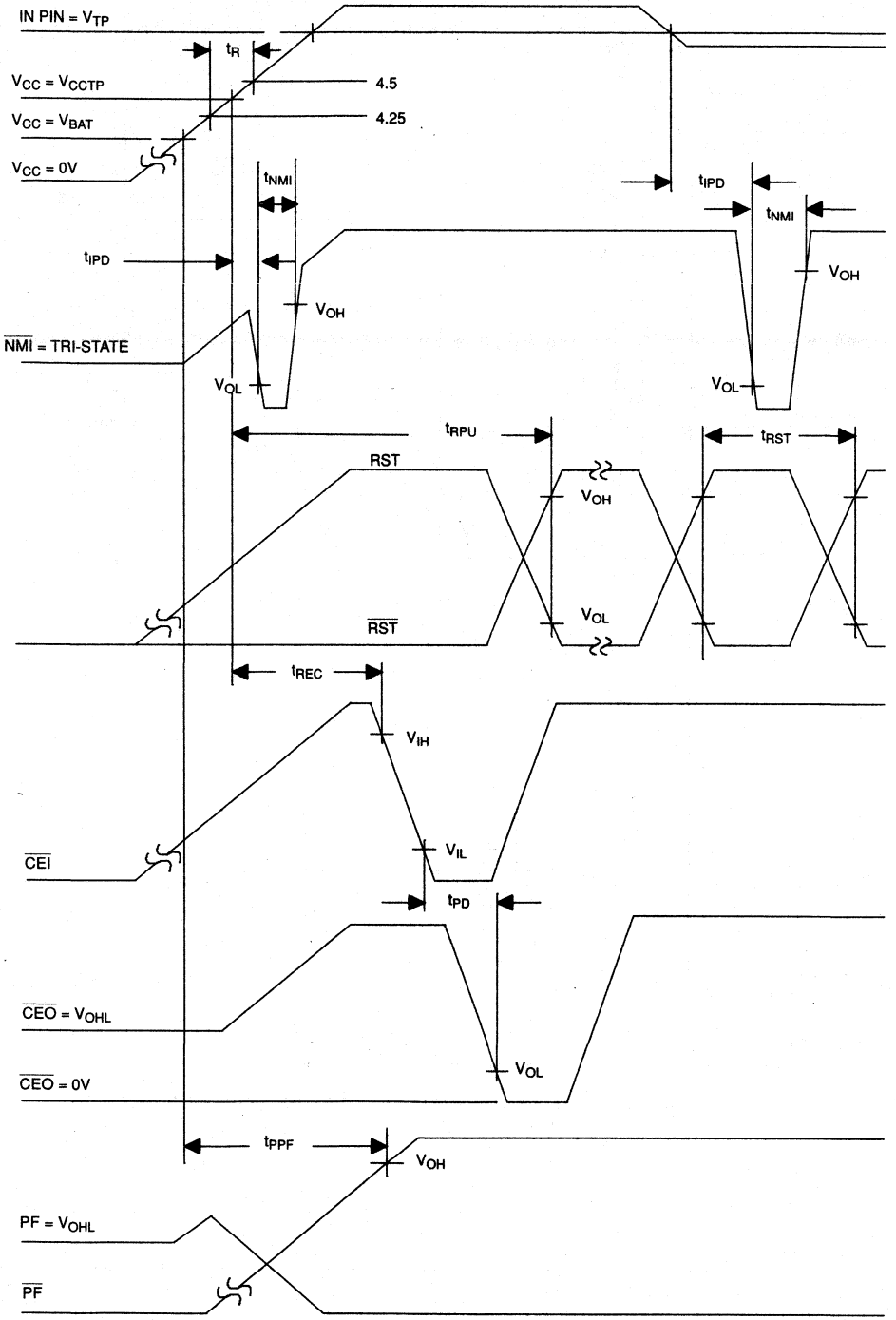
CMOS MODE POWER-DOWN (RC = V_{CCO}) Figure 10



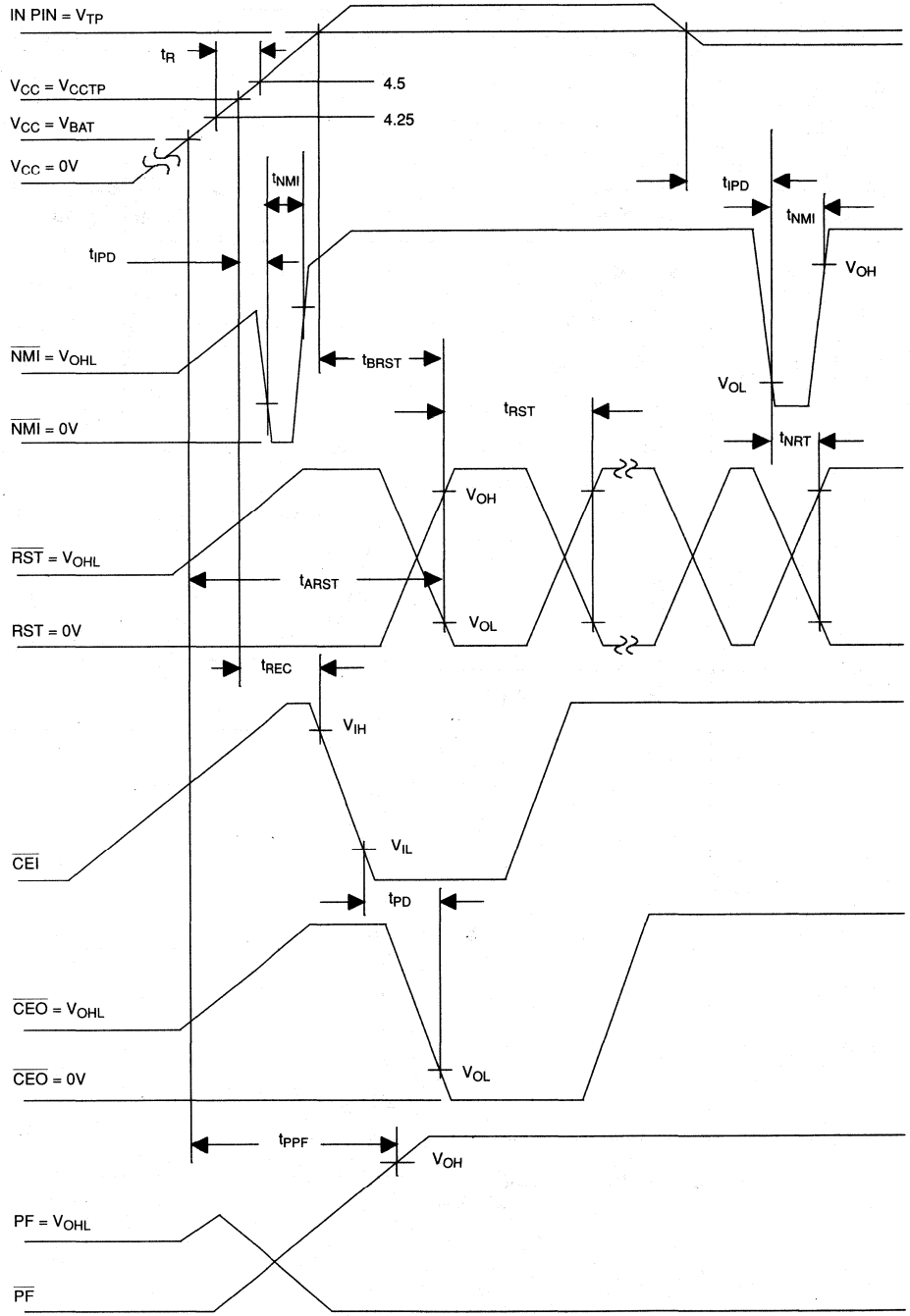
NMOS MODE POWER-DOWN (RC = GND) Figure 11



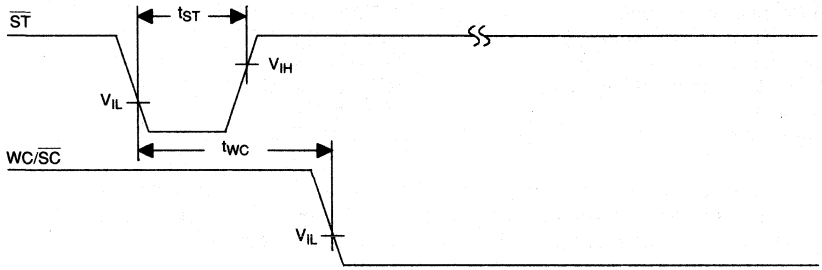
NMOS MODE POWER-UP (RC = GND) Figure 12



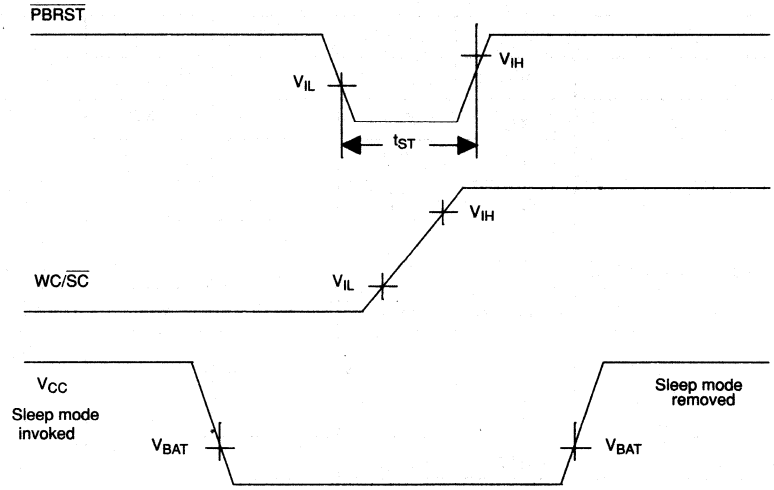
CMOS MODE POWER-UP (RC = V_{CCO}) Figure 13



WAKE/SLEEP CONTROL Figure 14



OPTIONS FOR INVOKING WAKEUP Figure 15



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	-0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Voltage on IN Pin Relative to Ground	–3.5V to V_{CC} + 0.5V
Operating Temperature	0°C to 70°C
Operating Temperature (Industrial Version)	–40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Supply Voltage (5% Option)	V_{CC}	4.75	5.0	5.5	V	1
Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	1
Input Low Level	V_{IL}	-0.3		+0.8	V	1
IN Input Pin	V_{IN}	-0.3		V_{CC} +0.3	V	1
Battery Input	V_{BAT}	2.7		4.0	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5 V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}			4	mA	2
Sleep Supply Current in Sleep mode	I_{CC}			20	µA	
Battery Current	I_{BAT}			0.1	µA	2
Supply Output Current (V_{CCO}=V_{CC} - 0.3V)	I_{CC01}			100	mA	3
Supply Output Current in Data Retention (V_{CC} < V_{BAT})	I_{CC02}			1	mA	4
Supply Output Voltage	V_{CCO}		V_{CC}–0.3		V	1
Battery Backup Voltage	V_{CCO}		V_{BAT}–0.7		V	1,6
Low Level @ RST	V_{OL}			0.4	V	1
Output Voltage @ –500 µA	V_{OH}	V_{CC}–0.5V	V_{CC}–0.1V		V	1
$\overline{CEO}$ and PF Output	V_{OHL}		V_{BAT}–0.7		V	1,6
$\overline{PBRST}$ Pull Up Resist	R_{PBRST}	10K			Ohms	
Input Leakage Current	I_{LI}	-1.0		+1.0	µA	18
Output Leakage	I_{LO}	-1.0		+1.0	µA	18
Output Current @0.4V	I_{OL}			4.0	mA	12

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Current @2.4V	I_{OH}	-1.0			mA	13
Power Sup. Trip Point	V_{CCTP}	4.25	4.37	4.50	V	1
Power Supply Trip (5% Option)	V_{CCTP}	4.50	4.62	4.75	V	1
IN Input Pin Current	I_{CCIN}	-1.0		+1.0	µA	
IN Input Trip Point	V_{TP}	2.5	2.54	2.6	V	1

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Fail Detect to RST, $\overline{RST}$	t_{RPD}	40	100	175	µs	
V_{TP} to $\overline{NMI}$	t_{IPD}	40	100	175	µs	
RESET Active Time	t_{RST}	25	100	150	ms	
$\overline{NMI}$ Pulse Width	t_{NMI}	200	300	500	µs	14
$\overline{ST}$ Pulse Width	t_{ST}	20			ns	19
$\overline{PBRST}$ @ V_{IL}	t_{PB}	30			ms	
V_{CC} Slew Rate 4.75 to 4.25	t_F	300			µs	
Chip Enable Propagation Delay	t_{PD}			20	ns	
V_{CC} Fail to Chip Enable High	t_{CF}	7	12	44	µs	17
V_{CC} Valid to RST, $\overline{RST}$ (RC=1)	t_{FPU}			100	ns	
V_{CC} Valid to RST & $\overline{RST}$	t_{RPU}	25	100	150	ms	5
V_{CC} Slew to 4.24 to V_{BAT}	t_{FB1}	10			µs	7
V_{CC} Slew 4.25 to 4.75 V_{BAT}	t_{FB2}	100			µs	8
Chip Enable Output Recovery Time	t_{REC}	.1			µs	9
V_{CC} Slew 4.25 to 4.75	t_R	0			µs	
Chip Enable Pulse Width	t_{CE}			5	s	10
Watchdog Time Delay	t_{TD}	100	400	600	ms	
$\overline{ST}$ to WC/$\overline{SC}$	t_{WC}	0.1		50	µs	
V_{BAT} Detect to PF, $\overline{PF}$	t_{PPF}			2	µs	7
$\overline{ST}$ to $\overline{NMI}$	t_{STN}			30	ns	11
$\overline{NMI}$ to RST & $\overline{RST}$	t_{NRT}			30	ns	
V_{BAT} Detect to RST & $\overline{RST}$	t_{ARST}			200	µs	15
V_{CC} Valid to RST, $\overline{RST}$	t_{BRST}	30	100	150	µs	16

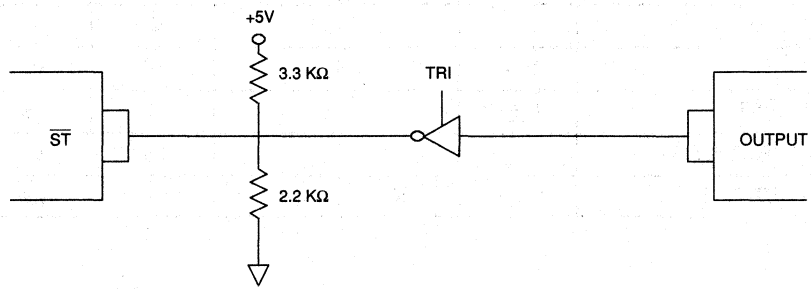
CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

NOTES:

1. All voltages referenced to ground. A 0.1 µF capacitor is recommended between V_{CC} and GND.
2. Measured with V_{CCO}, $\overline{CEO}$, PF, $\overline{ST}$, $\overline{PBRST}$, RST, $\overline{RST}$, and $\overline{NMI}$ pin open. I_{BAT} specified at 25°C.
3. I_{CCO1} is the maximum average load which the DS1236 can supply at V_{CC}-0.3V through the V_{CCO} pin during normal 5-volt operation.
4. I_{CCO2} is the maximum average load which the DS1236 can supply through the V_{CCO} pin during data retention battery supply operation, with a maximum drop of 0.8 volts.
5. With t_R = 5 µs.
6. V_{CCO} is approximately V_{BAT}-0.5V at 1 µA load.
7. Sleep mode is not invoked.
8. Sleep mode is invoked.
9. t_{REC} is the minimum time required before $\overline{CEI}$/$\overline{CEO}$ memory access is allowed.
10. t_{CE} maximum must be met to ensure data integrity on power loss.
11. IN input is less than V_{TP} but V_{CC} greater than V_{CCTP}.
12. All outputs except RST which is 25 µA maximum.
13. All outputs except $\overline{RST}$ and $\overline{NMI}$ which is 25 µA minimum.
14. Pulse width of $\overline{NMI}$ requires that the IN pin remain below V_{TP}. If the IN pin returns to a level above V_{TP} for a period longer than t_{IPD} and before the t_{NMI} period has elapsed, the $\overline{NMI}$ pin will immediately return to a high.
15. IN pin greater than V_{TP} when V_{CC} supply rises to V_{BAT}. Example: IN tied to GND.
16. IN pin less than V_{TP} when V_{CC} supply rises to V_{BAT}.
17. $\overline{CEI}$ low.
18. The WC/$\overline{SC}$ pin contains an internal latch which drives back on to the pin. This latch requires ±200 µamps to switch states. The $\overline{ST}$ pin will sink ±50 uamps in normal operation and ±1 µamp in the sleep mode.
19. $\overline{ST}$ should be active low before the watchdog is disabled (i.e., before the $\overline{ST}$ input is tristated).



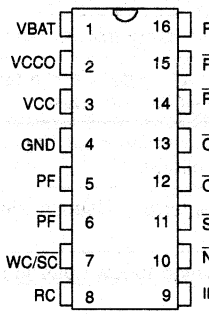
DALLAS SEMICONDUCTOR

DS1236A
MicroManager Chip

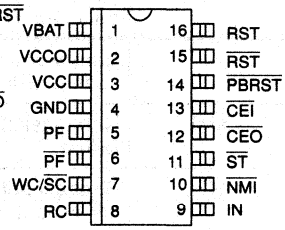
FEATURES

- Holds microprocessor in check during power transients
- Halts and restarts an out-of-control microprocessor
- Monitors pushbutton for external override
- Warns microprocessor of an impending power failure
- Converts CMOS SRAM into nonvolatile memory
- Unconditionally write protects memory when power supply is out of tolerance
- Consumes less than 100 nA of battery current at 25°C
- Controls external power switch for high current applications
- Accurate 10% power supply monitoring
- Optional 5% power supply monitoring designated DS1236A-5
- Provides orderly shutdown in nonvolatile microprocessor applications
- Supplies necessary control for low-power "stop mode" in battery operated hand-held applications
- Standard 16-pin DIP or space-saving 16-pin SOIC
- Optional industrial temperature range -40°C to +85°C

PIN ASSIGNMENT



16-Pin DIP (300 Mil.)
See Mech. Drawing
Pg. 480



16-Pin SOIC (300 Mil.)
See Mech. Drawing
Pg 484

PIN DESCRIPTION

V_{BAT}	–	+3 Volt Battery Input
V_{CCO}	–	Switched SRAM Supply Output
V_{CC}	–	+5 Volt Power Supply Input
GND	–	Ground
PF	–	Power Fail (Active High)
$\overline{PF}$	–	Power Fail (Active Low)
WC/$\overline{SC}$	–	Wake-Up Control (Sleep)
RC	–	Reset Control
IN	–	Early Warning Input
$\overline{NMI}$	–	Non-Maskable Interrupt
$\overline{ST}$	–	Strobe Input
$\overline{CEO}$	–	Chip Enable Output
$\overline{CEI}$	–	Chip Enable Input
$\overline{PBRST}$	–	Pushbutton Reset Input
$\overline{RST}$	–	Reset Output (Active Low)
RST	–	Reset Output (Active High)

DESCRIPTION

The DS1236A MicroManager Chip provides all the necessary functions for power supply monitoring, reset control, and memory backup in microprocessor-based systems. A precise internal voltage reference and comparator circuit monitor power supply status. When an out-of-tolerance condition occurs, the microprocessor reset and power fail outputs are forced active, and static RAM control unconditionally write protects external memory. The DS1236A also provides early warning detection of a user-defined threshold by driving a non-maskable interrupt. External reset control is provided by a pushbutton reset input which is debounced and activates reset outputs. An internal watchdog timer can also force the reset outputs to the active state if the strobe input is not driven low prior to watchdog time-out. Reset control and wake-up/sleep control inputs also provide the necessary signals for orderly shutdown and start-up in battery backup and battery operated applications. A block diagram of the DS1236A is shown in Figure 1.

PIN DESCRIPTION

PIN NAME	DESCRIPTION
V_{BAT}	+3V battery input provides nonvolatile operation of control functions.
V_{CCO}	V_{CC} output for nonvolatile SRAM applications.
V_{CC}	+5V primary power input.
PF	Power fail indicator, active high, used for external power switching as shown in Figure 9.
$\overline{PF}$	Power fail indicator, active low.
WC/$\overline{SC}$	Wake-up and Sleep control. Invokes low-power mode.
RC	Reset control input. Determines reset output . Normally low for NMOS processors and high for battery-backed CMOS processors.
IN	Early warning power fail input. This voltage sense point can be tied (via resistor divider) to a user-selected voltage.
$\overline{NMI}$	Non-maskable interrupt. Used in conjunction with the IN pin to indicate an impending power failure.
$\overline{ST}$	Strobe input. A high-to-low transition will reset the watchdog timer, indicating that software is still in control.
$\overline{CEO}$	Chip enable output. Used with nonvolatile SRAM applications.
$\overline{CEI}$	Chip enable input.
$\overline{PBRST}$	Pushbutton reset input.
$\overline{RST}$	Active low reset output.
RST	Active high reset output.

PROCESSOR MODE

A distinction is often made between CMOS and NMOS processor systems. In a CMOS system, power consumption may be a concern, and nonvolatile operation is possible by battery backing both the SRAM and the CMOS processor. All resources would be maintained in the absence of V_{CC}. A power-down reset is not issued since the low-power mode of most CMOS processors (Stop) is terminated with a Reset. A pulsed interrupt ($\overline{NMI}$) is issued to allow the CMOS processor to invoke a sleep mode to save power. For this case, a power-on reset is desirable to wake up and initialize the processor. The CMOS mode is invoked by connecting RC to V_{CCO}.

An NMOS processor consumes more power, and consequently may not be battery backed. In this case, it is desirable to notify the processor of a power fail, then keep it in reset during the loss of V_{CC}. This avoids intermittent or aberrant operation. On power-up, the processor will continue to be reset until V_{CC} reaches an operational level to provide an orderly start. The NMOS mode is invoked by connecting RC to ground.

POWER MONITOR

The DS1236A employs a band gap voltage reference and a precision comparator to monitor the 5-volt supply (V_{CC}) in microprocessor-based systems. When an out-of-tolerance condition occurs, the RST and $\overline{RST}$ outputs are driven to the active state. Th e V_{CC} trip point (V_{CCTP}) is set for 10% operation so that the RST and $\overline{RST}$ outputs will become active as V_{CC} falls below 4.5 volts (4.37 typical). The V_{CCTP} for the 5% operation option (DS1236A–5) is set for 4.75 volts (4.62 typical). The RST and $\overline{RST}$ signals are excellent for microprocessor reset control, as processing is stopped at the last possible moment of in-tolerance V_{CC}. On power-up, the RST and $\overline{RST}$ signals are held active for a minimum of 25 ms (100 ms typical) after V_{CCTP} is reached to allow the power supply and microprocessor to stabilize. Note: The operation described above is obtained with the reset control pin (RC) connected to GND (NMOS mode). Please review the reset control section for more information.

WATCHDOG TIMER

The DS1236A provides a watchdog timer function which forces the RST and $\overline{RST}$ signals to the active state when the strobe input ($\overline{ST}$) is not stimulated for a predetermined time period. This time period is 400 ms typically with a maximum time-out of 600 ms. The watchdog time-out period begins as soon as RST and $\overline{RST}$ are inactive. If a high-to-low transition occurs at the $\overline{ST}$ input prior to time-out, the watchdog timer is reset and begins to time out again. The $\overline{ST}$ input timing is shown in Figure 2. To guarantee the watchdog timer does not time out, a high-to-low transition on $\overline{ST}$ must occur at or less than 100 ms (minimum time-out) from a reset. If the watchdog timer is allowed to time out, the RST and $\overline{RST}$ outputs are driven to the active state for 25 ms minimum. The $\overline{ST}$ input can be derived from microprocessor address, data, and/or control signals. Under normal operating conditions, these signals would routinely reset the watchdog timer prior to time-out. If the watchdog timer is not required, two methods have been provided to disable it.

Permanently grounding the IN pin in the CMOS mode (RC=1) will disable the watchdog. In normal operation with RC=1, the watchdog is disabled as soon as the IN pin is below V_{TP}. With IN grounded, an $\overline{NMI}$ output will occur only at power-up, or when the $\overline{ST}$ pin is strobed. As shown in the Figure 3, a falling edge on $\overline{ST}$ will generate an $\overline{NMI}$ when IN is below V_{TP}. This allows the processor to verify that power is between V_{TP} and V_{CCTP}, as an $\overline{NMI}$ will be returned immediately after the $\overline{ST}$ strobe. The watchdog timer is not affected by the IN pin when in NMOS mode (RC=0).

If the $\overline{NMI}$ signal is required to monitor supply voltages, the watchdog may also be disabled by leaving the $\overline{ST}$ input open. Independent of the state of the RC pin, the watchdog is also disabled as soon as V_{CC} falls to V_{CCTP}.

PUSHBUTTON RESET

An input pin is provided on the DS1236A for direct connection to a pushbutton. The pushbutton reset input requires an active low signal. Internally, this input is pulled high by a 10K resistor whenever V_{CC} is greater than V_{BAT}. The $\overline{PBRST}$ pin is also debounced and timed such that the RST and $\overline{RST}$ outputs are driven to the active state for 25 ms minimum. This 25 ms delay begins as the pushbutton is released from a low level. A typical example of the power monitor, watchdog timer, and pushbutton reset connections are shown in Figure 4. The $\overline{PBRST}$ input is disabled whenever the IN pin voltage level is less than V_{TP} and the reset control (RC) is tied high (CMOS mode). The $\overline{PBRST}$ input is also disabled whenever V_{CC} is below V_{BAT}. Timing of the $\overline{PBRST}$-generated RST is illustrated in Figure 5.

NON-MASKABLE INTERRUPT

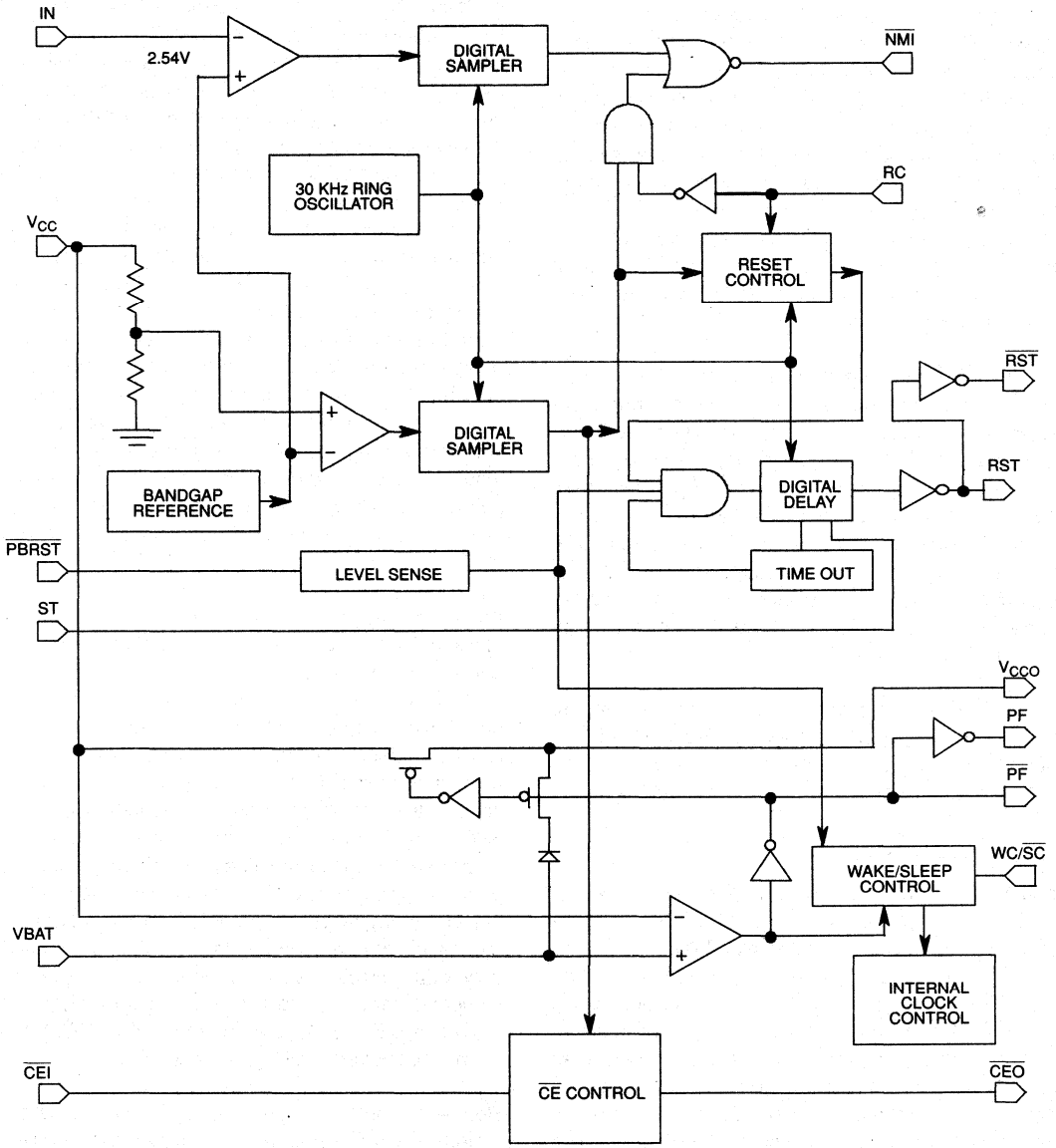
The DS1236A generates a non-maskable interrupt $\overline{NMI}$ for early warning of power failure to a microprocessor. A precision comparator monitors the voltage level at the IN pin relative to a reference generated by the internal band gap. The IN pin is a high impedance input allowing for a user-defined sense point. An external resistor voltage divider network (Figure 6) is used to interface with high voltage signals. This sense point may be derived from the regulated 5-volt supply or from a higher DC voltage level closer to the main system power input. Since the IN trip point V_{TP} is 2.54 volts, the proper values for R1 and R2 can be determined by the equation as shown in Figure 6. Proper operation of the DS1236A requires that the voltage at the IN pin be limited to V_{IN}. Therefore, the maximum allowable voltage at the supply being monitored (V_{MAX}) can also be derived as shown in Figure 6. A simple approach to solving this equation is to select a value for R2 high enough to keep power consumption low, and solve for R1. The flexibility of the IN input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time for microprocessor shut-down between $\overline{NMI}$ and RST or $\overline{RST}$.

When the supply being monitored decays to the voltage sense point, the DS1236A pulses the $\overline{NMI}$ output to the active state for a minimum of 200 µs. The $\overline{NMI}$ power fail detection circuitry also has built-in time domain hysteresis. That is, the monitored supply is sampled periodically at a rate determined by an internal ring oscillator running at approximately 30 KHz (33 µs/cycle). Three consecutive samplings of out-of-tolerance supply (below V_{SENSE}) must occur at the IN pin to active $\overline{NMI}$. Therefore, the supply must be below the voltage sense point for approximately 100 µs or the comparator will reset. In this way, power supply noise is removed from the monitoring function, preventing false trips. During a power-up , any detected IN pin levels be low V_{TP} by the comparator are disabled from reaching the $\overline{NMI}$ pin until V_{CC} rises to V_{CCTP}. As a result, any potential $\overline{NMI}$ pulse will not be initiated until V_{CC} reaches V_{CCTP}.

Removal of an active low level on the $\overline{NMI}$ pin is controlled by either an internal time-out (when IN pin is less than V_{TP}) or by the subsequent rise of the IN pin above

V_{TP}. The initiation and removal of the $\overline{NMI}$ signal during power-up results in an $\overline{NMI}$ pulse of from 0 µs minimum to 500 µs maximum, depending on the relative voltage relationship between V_{CC} and the IN pin voltage. As an example, when the IN pin is tied to ground during power-up, the internal time-out will result in a pulse of 200 µs minimum to 500 µs maximum. In contrast, if the IN pin is tied to V_{CCO} during power-up, $\overline{NMI}$ will not produce a pulse on power-up. Note that a fast slewing power supply may cause the $\overline{NMI}$ to be virtually non-existent on power-up. This is of no consequence, however, since a $\overline{RST}$ will be active.

DS1236A FUNCTIONAL BLOCK DIAGRAM Figure 1



If the IN pin is connected to V_{CCO}, the $\overline{NMI}$ output will pulse low as V_{CC} decays to V_{CCTP} in the NMOS mode (RC=0). In the CMOS mode (RC=V_{CCO}) the power-down of V_{CC} out-of-tolerance at V_{CCTP} will not produce a pulse on the $\overline{NMI}$ pin. Given that any $\overline{NMI}$ pulse has been completed by the time V_{CC} decays to V_{CCTP}, the $\overline{NMI}$ pin will remain high. The $\overline{NMI}$ voltage will follow V_{CC} down until V_{CC} decays to V_{BAT}. Once V_{CC} decays to V_{BAT}, the $\overline{NMI}$ pin will either remain at V_{OHL} or enter tri-state mode as determined by the RC pin (see "Reset Control" section).

MEMORY BACKUP

The DS1236A provides all of the necessary functions required to battery back a static RAM. First, a switch is provided to direct SRAM power from the incoming 5 volt supply (V_{CC}) or from an external battery (V_{BAT}), whichever is greater. This switched supply (V_{CCO}) can also be used to battery back a CMOS microprocessor. For more information about nonvolatile processor applications, review the "Reset Control" and "Wake Control" sections. Second, the same power fail detection described in the power monitor section is used to hold the chip enable output ($\overline{CEO}$) to within 0.3 volts of V_{CC} or to within 0.7 volts of V_{BAT}. This write protection mechanism occurs as V_{CC} falls below V_{CCTP} as specified. If $\overline{CEI}$ is low at the time power fail detection occurs, $\overline{CEO}$ is held in its present state until $\overline{CEI}$ is returned high, or the period t_{CE} expires. This delay of write protection until the current memory cycle is completed prevents the corruption of data. If $\overline{CEO}$ is in an inactive state at the time of V_{CC} fail detection, $\overline{CEO}$ will be unconditionally disabled within t_{CF}. During nominal supply conditions $\overline{CEO}$ will follow $\overline{CEI}$ with a maximum propagation delay of 20 ns. Figure 7 shows a typical nonvolatile SRAM application. The DS1236A unlike the DS1236 can be operated without a battery. In this method of operation the V_{BAT}, pin 1, must be grounded. In general, it would also be expected to have the RC, pin 8, grounded (NMOS mode) since no battery backup is available.

FRESHNESS SEAL

In order to conserve battery capacity during initial construction of an end system, the DS1236A provides a freshness seal that electrically disconnects the battery. This means that upon battery attach, the V_{CCO} output will remain inactive until V_{CC} is applied. This prevents V_{CCO} from powering other devices when the battery is first attached, and V_{CC} is not present. Once V_{CC} is applied, the freshness seal is broken and cannot be invoked again without subsequent removal and re–attachment of the battery.

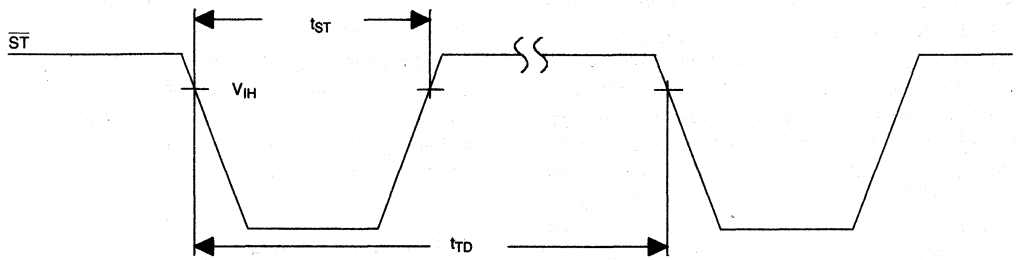
POWER SWITCHING

When larger operating currents are required in a battery-backed system, the 5-volt supply and battery supply switches internal to the DS1236A may not be large enough to support the required load through V_{CCO} with a reasonable voltage drop. For these applications, the PF and $\overline{PF}$ outputs are provided to gate external power switching devices. As shown in Figure 8, power to the load is switched from V_{CC} to battery on power-down, and from battery to V_{CC} on power- up. The DS1336 is designed to use the $\overline{PF}$ output to switch between V_{BAT} and V_{CC}. It provides better leakage and switchover performance than currently available discrete components. The transition threshold for PF and $\overline{PF}$ is set to the external battery voltage V_{BAT}, allowing a smooth transition between sources. The load applied to the PF pin from the external switch will be supplied by the battery. Therefore, if a discrete switch is used, this load should be taken into consideration when sizing the battery.

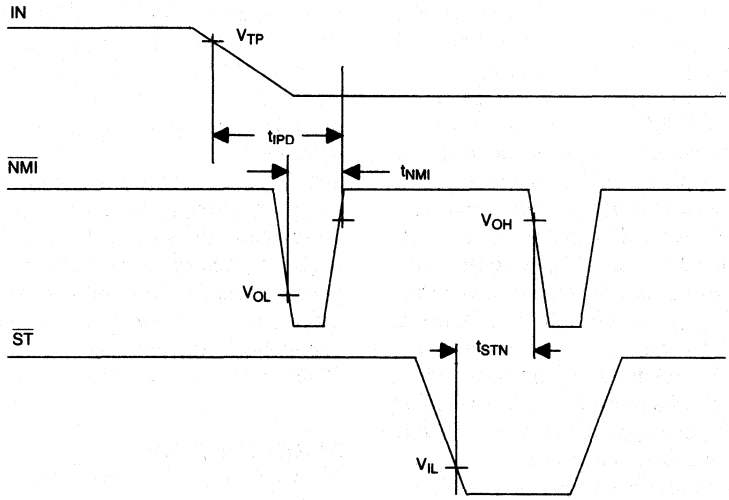
RESET CONTROL

As mentioned above, the DS1236A supports two modes of operation. The CMOS mode is used when the system incorporates a CMOS microprocessor which is battery backed. The NMOS mode is used when a non-battery backed processor is incorporated. The mode is selected by the RC (Reset Control) pin. The level of this pin distinguishes timing and level control on RST, $\overline{RST}$, and $\overline{NMI}$ outputs for volatile processor operation versus nonvolatile battery backup or battery-operated processor applications.

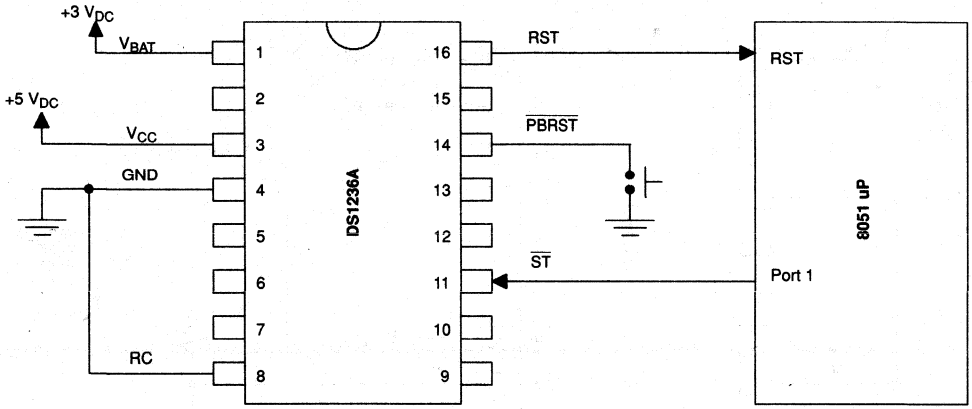
ST/INPUT TIMING Figure 2



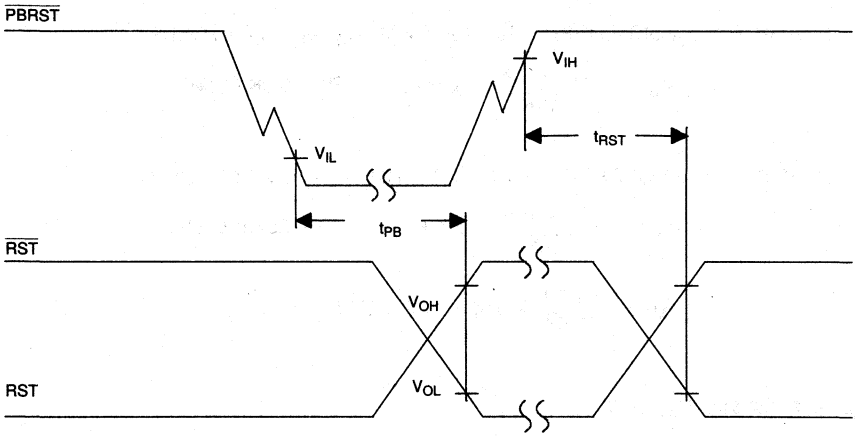
NMI/FROM ST/INPUT Figure 3



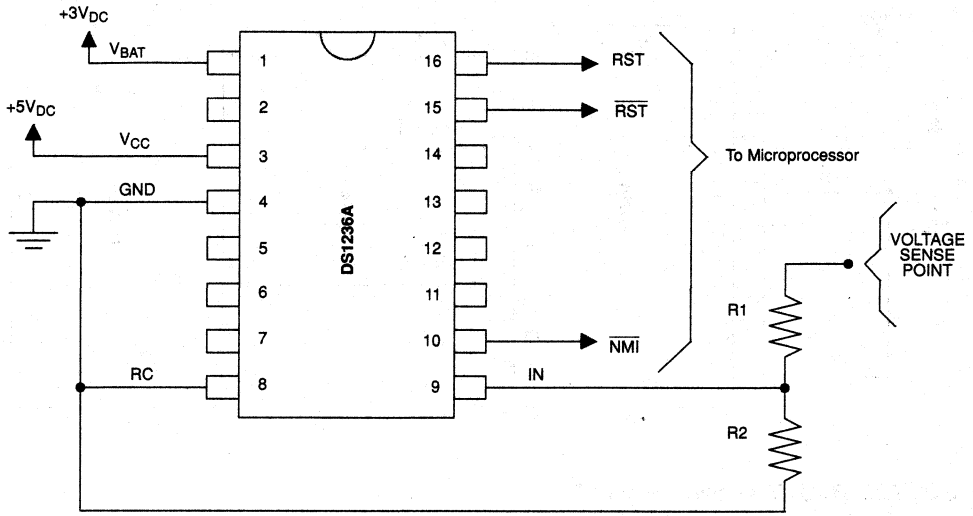
POWER MONITOR, WATCHDOG Figure 4



PUSH BUTTON RESET TIMING Figure 5



NON-MASKABLE INTERRUPT Figure 6



EXAMPLE 1: 5 VOLT SUPPLY, R2 = 10K OHM, V_{SENSE} = 4.80 VOLTS

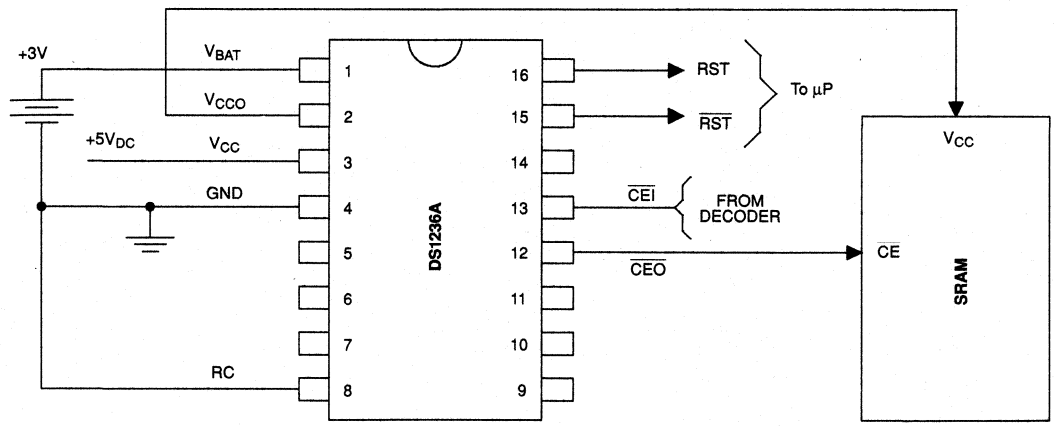
$$\therefore 4.80 = \frac{R1 + 10K}{10K} \times 2.54 \qquad R1 = 8.9K\ OHM$$

EXAMPLE 2: 12 VOLT SUPPLY, R2 = 10K OHM, V_{SENSE} = 9.00 VOLTS

$$\therefore 9.00 = \frac{R1 + 10K}{10K} \times 2.54 \qquad R1 = 25.4K\ OHM$$

$$V_{MAX} = \frac{9.00}{2.54} \times 5.00 = 17.7\ VOLTS$$

NONVOLATILE SRAM Figure 7



When the RC pin is tied to ground, the DS1236A is designed to interface with NMOS processors which do not have the microamp currents required during a battery backed mode. Grounding the RC pin does, however, continue to support nonvolatile backup of system SRAM memory. Nonvolatile systems incorporating NMOS processors generally require that only the SRAM memory and/or timekeeping functions be battery backed. When the processor is not battery backed (RC = 0), all signals connected from the processor to the DS1236A are disconnected from the backup battery supply, or grounded when system V_{CC} decays below V_{BAT}. In the NMOS processor system, the principal emphasis is placed on giving early warnings with $\overline{NMI}$, then providing a continuously active RST and $\overline{RST}$ signal during power-down while isolating the backup battery from the processor during a loss of V_{CC}.

During power-down, $\overline{NMI}$ will pulse low for a minimum of 200 µs, and then return high. If RC is tied low (NMOS mode), the voltage on $\overline{NMI}$ will follow V_{CC} until V_{CC} supply decays to V_{BAT}, at which point $\overline{NMI}$ will enter tri-state (see timing diagram). Also, upon V_{CC} out-of-tolerance at V_{CCTP}, the RST and $\overline{RST}$ outputs are driven active and RST will follow V_{CC} as the supply decays. On power-up, RST follows V_{CC} up, $\overline{RST}$ is held low, and both remain active for t_{RST} after valid V_{CC}. During a power-up from a V_{CC} voltage below V_{BAT}, any detected IN pin levels below V_{TP} are disabled from reaching the $\overline{NMI}$ pin until V_{CC} rises to V_{CCTP}. As a result, any potential $\overline{NMI}$ pulse will not be initiated until V_{CC} reaches V_{CCTP}. Removal of an active low level on the $\overline{NMI}$ pin is controlled by either an internal time-out (when the IN pin is less than V_{TP}), or by the subsequent rise of the IN pin above V_{TP}. The initiation and removal of the $\overline{NMI}$ signal results in an $\overline{NMI}$ pulse of 0 µs minimum to 500 µs maximum during power-up, depending on the relative voltage relationship between V_{CC} and the IN pin. As an example, when the IN pin is tied to ground, the internal time-out will result in a pulse of 200 µs minimum to 500 µs maximum. In contrast, if the IN pin is tied to V_{CCO}, $\overline{NMI}$ will not produce a pulse on power-up.

Connecting the RC pin to a high (V_{CCO}) invokes CMOS mode and provides nonvolatile support to both the system SRAM as well as a low power CMOS processor. When using CMOS microprocessors, it is possible to place the microprocessor into a very low- power mode termed the "stop" or "halt" mode. In this state the CMOS processor requires only microamp currents and is fully capable of being battery backed. This mode generally allows the CMOS microprocessor to maintain the contents of internal RAM as well as state control of I/O ports during battery backup. The processor can subsequently be restarted by any of several different signals. To maintain this low-power state, the DS1236A issues no $\overline{NMI}$ and/or reset signals to the processor until it is time to bring the processor back into full operation. To support the low-power processor battery backed mode (RC = 1), the DS1236A provides a pulsed $\overline{NMI}$ for early power failure warning. Waiting to initiate a Stop mode until after the $\overline{NMI}$ pin has returned high will guarantee the processor that no other active $\overline{NMI}$ or RST/$\overline{RST}$ will be issued by the DS1236A until one of two conditions occurs: 1) Voltage on the pin rises above V_{TP}, which activates the watchdog, or 2) V_{CC} cycles below then above V_{BAT}, which also results in an active RST and $\overline{RST}$. If V_{CC} does not fall below V_{CCTP}, the processor will be restarted by the reset derived from the watchdog timer as the IN pin rises above V_{TP}.

With the RC pin tied to V_{CCO}, RST and $\overline{RST}$ are not forced active as V_{CC} collapses to V_{CCTP}. The $\overline{RST}$ is held at a high level via the external battery as V_{CC} falls below battery potential. This mode of operation is intended for applications in which the processor is made nonvolatile with an external source, and allows the processor to power down into a Stop mode as signaled from $\overline{NMI}$ at an earlier voltage level. The $\overline{NMI}$ output pin will pulse low for t_{NMI} following a low voltage detect at the IN pin of V_{TP}. Following t_{NMI}, however, $\overline{NMI}$ will also be held at a high level (V_{BAT}) by the battery as V_{CC} decays below V_{BAT}. On power-up, RST and $\overline{RST}$ are held inactive until V_{CC} reaches V_{BAT}, then RST and $\overline{RST}$ are driven active for t_{RST}. If the IN pin falls below V_{TP} during an active reset, the reset outputs will be forced inactive by the $\overline{NMI}$ output. In addition, as long as the IN pin is less than V_{TP}, stimulation of the ST pin will result in additional $\overline{NMI}$ pulses. In this way, the $\overline{ST}$ pin can be used to allow the CMOS processor to determine if the supply voltage, as monitored by the IN pin, is above or below a selected operating value. This is illustrated in Figure 3. As discussed above, the RC pin determines the timing relationships and levels of several signals. The following section describes the power-up and power-down timing diagrams in more detail.

TIMING DIAGRAMS

This section provides a description of the timing diagrams shown in Figure 9, Figure 10, Figure 11, and Figure 12. These diagrams show the relative timing and levels in both the NMOS and the CMOS mode for power-up and down. Figure 9 illustrates the relationship for

power-down in CMOS mode. As V_{CC} falls, the IN pin voltage drops below V_{TP}. As a result, the processor is notified of an impending power failure via an active $\overline{NMI}$, which allows it to enter a sleep mode. As the power falls further, V_{CC} crosses V_{CCTP}, the power monitor trip point. Since the DS1236A is in CMOS mode, no reset is generated. The $\overline{RST}$ voltage will follow V_{CC} down, but will fall no further than V_{BAT}. At this time, $\overline{CEO}$ is brought high to write protect the RAM. When the V_{CC} reaches V_{BAT}, a power fail is issued via the PF and $\overline{PF}$ pins.

Figure 10 illustrates operation of the power-down sequence in NMOS mode. Once again, as power falls, an $\overline{NMI}$ is issued. This gives the processor time to save critical data in nonvolatile SRAM. When V_{CC} reaches V_{CCTP}, an active RST and $\overline{RST}$ are given. The RST voltage will follow V_{CC} as it falls. $\overline{CEO}$, PF, and $\overline{PF}$ will operate in a similar manner to CMOS mode. Notice that the $\overline{NMI}$ will tri-state to prevent a loss of battery power.

Figure 11 shows the power-up sequence for the NMOS mode. As V_{CC} slews above V_{BAT}, the PF and $\overline{PF}$ pins are deactivated. An active reset occurs as well as an $\overline{NMI}$. Although the $\overline{NMI}$ may be short due to slew rates, reset will be maintained for the standard t_{RST} time-out period. At a later time, if the IN pin falls below V_{TP}, a new $\overline{NMI}$ will occur. If the processor does not issue a $\overline{ST}$, a watchdog reset will also occur. The second $\overline{NMI}$ and RST are provided to illustrate these possibilities.

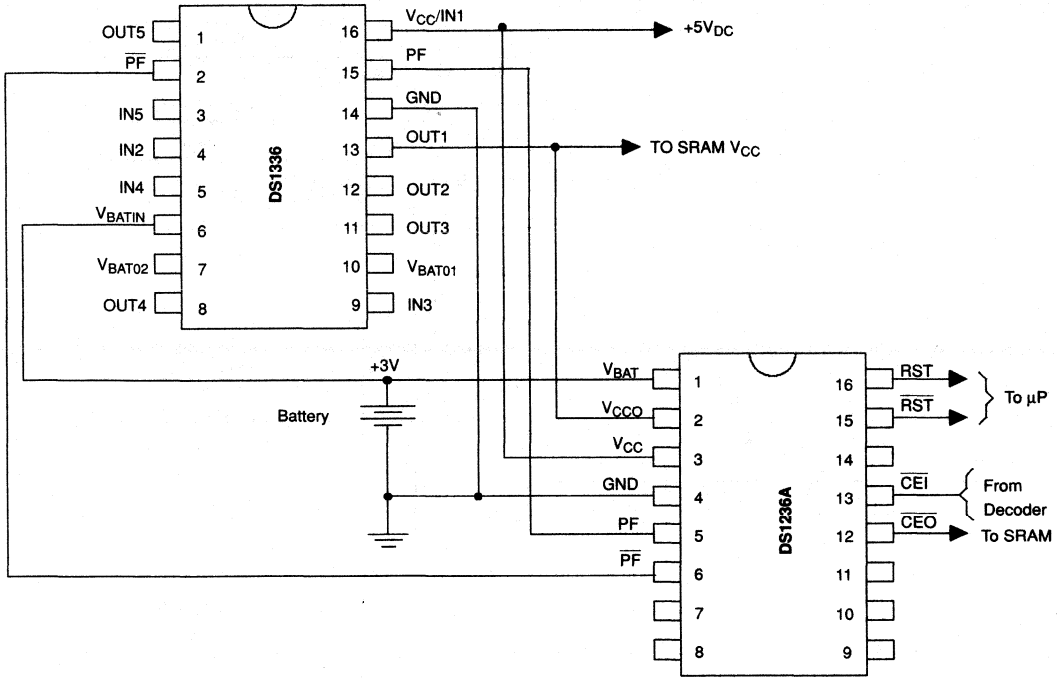
Figure 12 illustrates the power-up timing for CMOS mode. The principal difference is that the DS1236A issues a reset immediately in the NMOS mode. In CMOS mode, a reset is issued when IN rises above V_{TP}. Depending on the processor type, the $\overline{NMI}$ may terminate the Stop mode in the processor.

WAKE CONTROL/SLEEP CONTROL

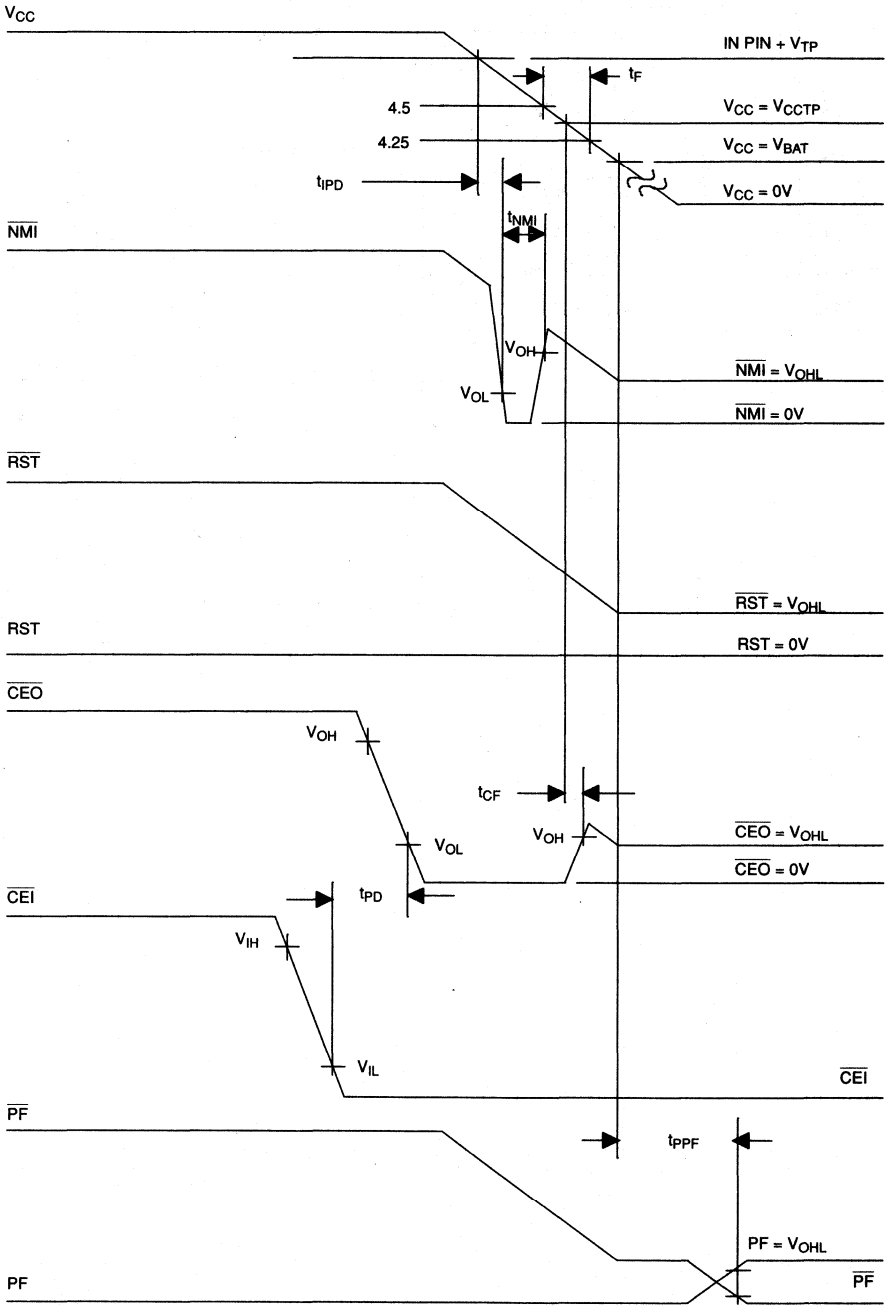
The Wake/Sleep Control input (WC/$\overline{SC}$) allows the processor to disable all comparators on the DS1236A before entering the Stop mode. This feature allows the DS1236A, processor, and static RAM to maintain nonvolatility in the lowest power mode possible. The processor may invoke the sleep mode in battery-operated applications to conserve battery capacity when an absence of activity is detected. The operation of this signal is shown in Figure 13. The DS1236A may subsequently be restarted by a high-to-low transition on the $\overline{PBRST}$ input through human interface via a keyboard, touchpad, etc. The processor will then be restarted as the watchdog times out and drives RST and $\overline{RST}$ active. The DS1236A can also be started up by forcing the WC/$\overline{SC}$ pin high from an external source. Also, if the DS1236A is placed in a sleep mode by the processor and system power is lost, the DS1236A will wake up the next time V_{CC} rises above V_{BAT}. These possibilities are illustrated in Figure 14.

When the sleep mode is invoked during normal power-valid conditions, all operation on the DS1236A is disabled, thus leaving the $\overline{NMI}$, RST, and $\overline{RST}$ outputs disabled as well as the $\overline{ST}$ and IN inputs. However, a loss of power during a sleep mode will result in an active RST and $\overline{RST}$ when the RC pin is grounded (NMOS mode). If the RC pin is tied high, the RST and $\overline{RST}$ pins will remain inactive during power-down in a sleep mode. Removal of the sleep mode by the $\overline{PBRST}$ input is not affected by the IN pin threshold at V_{TP} when the RC pin is tied high (CMOS mode). Subsequent power-up of the V_{CC} supply with the RC pin tied high will activate the RST and $\overline{RST}$ outputs as the main supply rises above V_{BAT}. A high-to-low transition on the WC/$\overline{SC}$ pin must follow a high-to-low transition on the ST pin by t_{WC} to invoke a Sleep mode for the DS1236A.

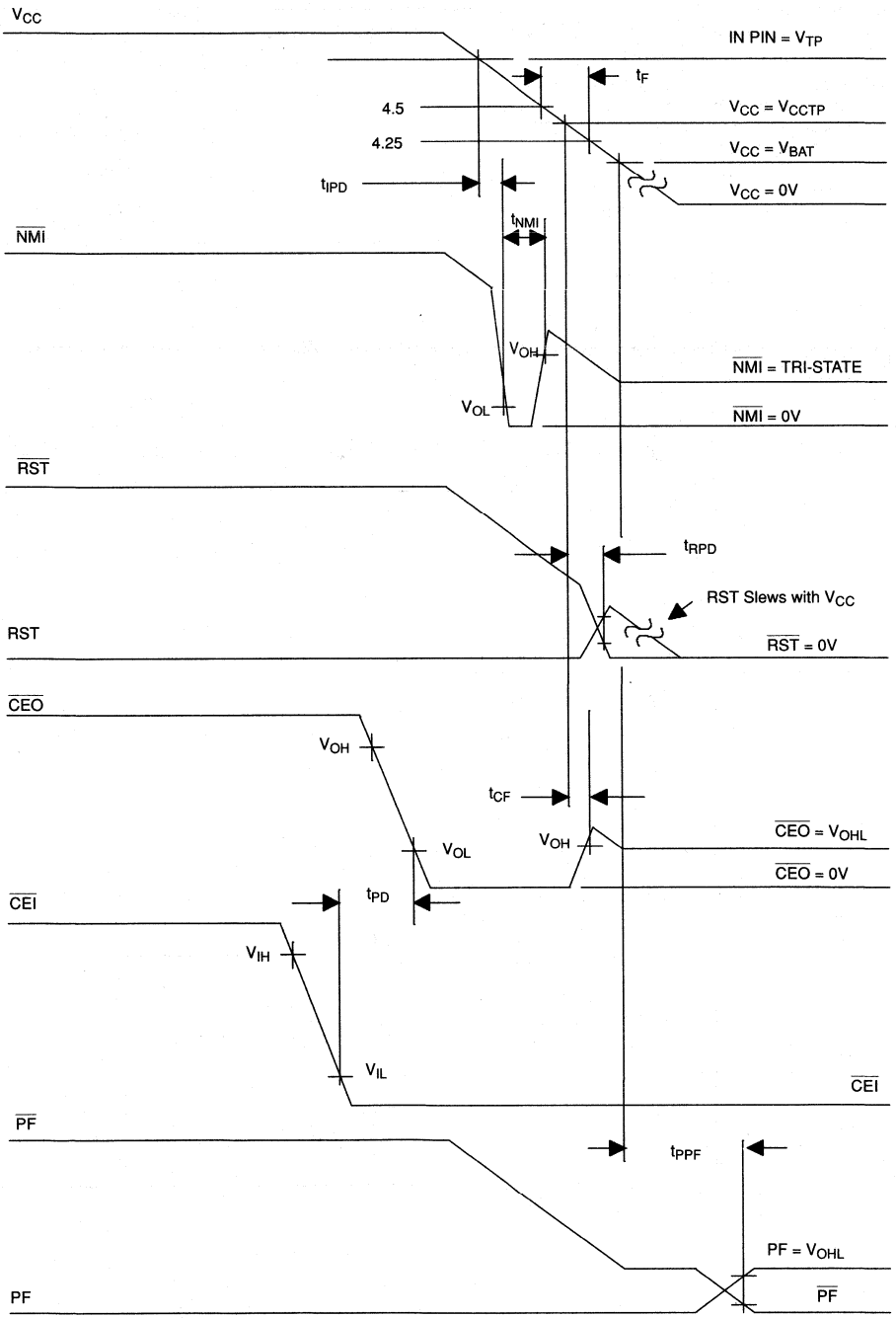
POWER SWITCHING Figure 8



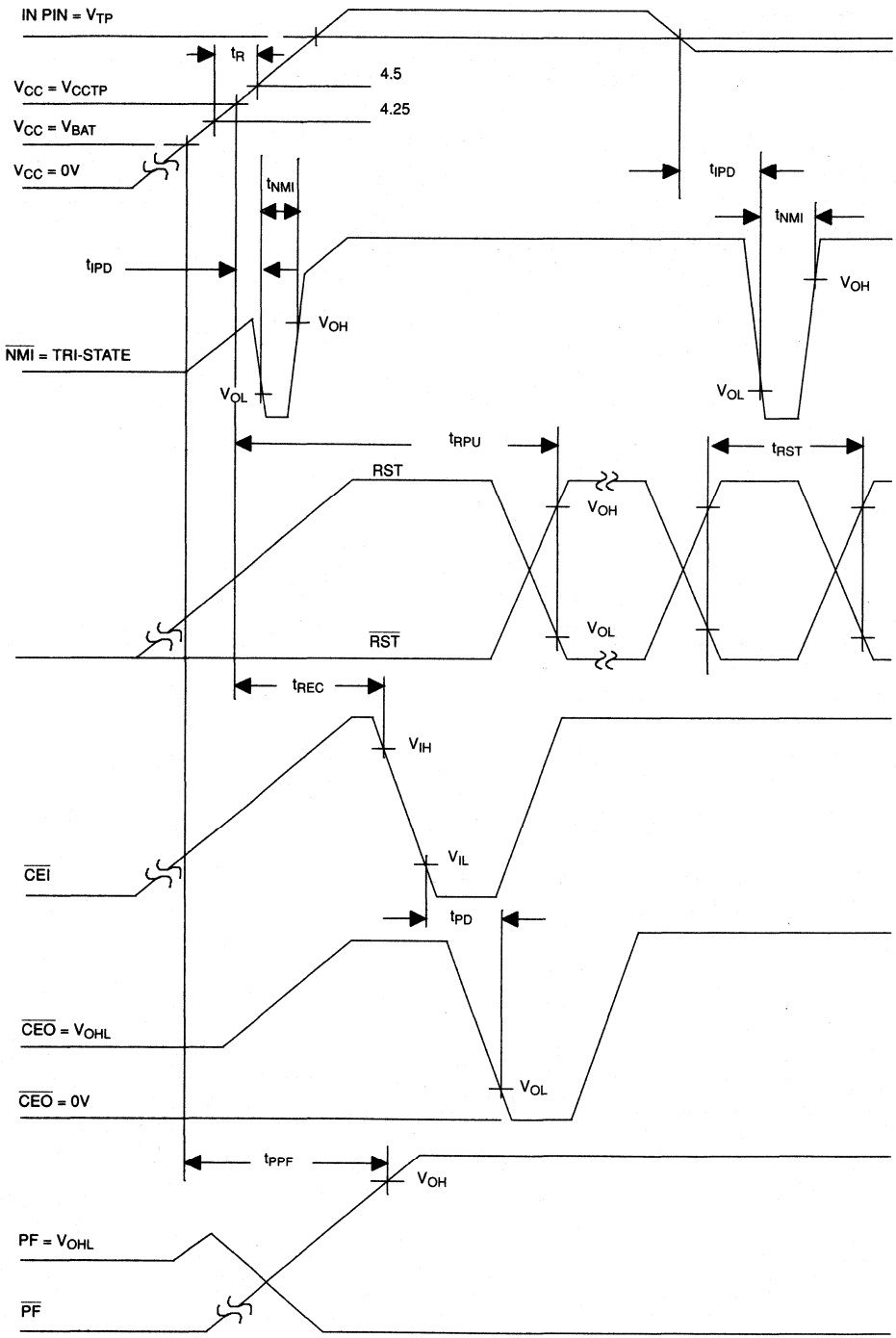
CMOS MODE POWER-DOWN (RC = V_{CCO}) Figure 9



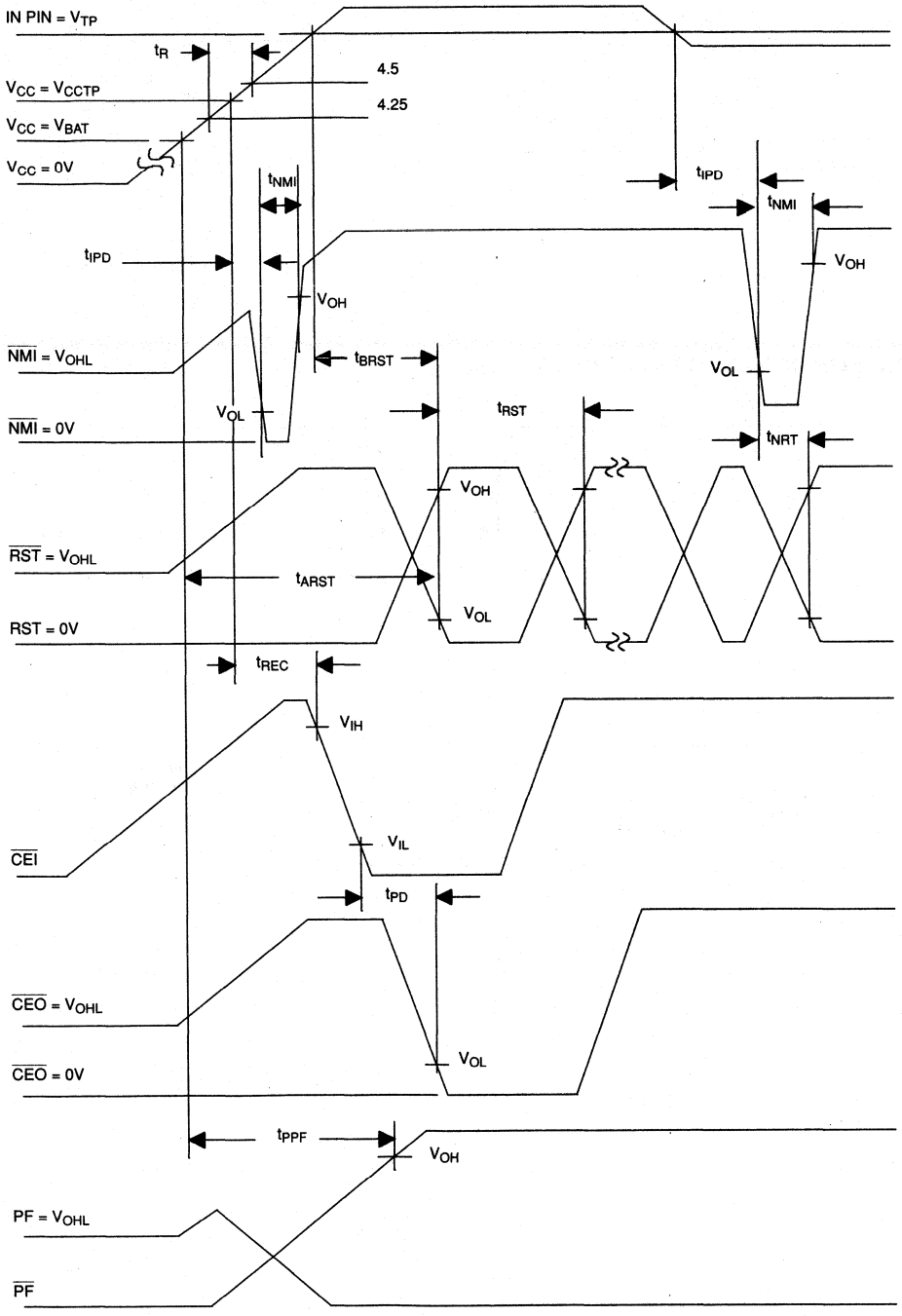
NMOS MODE POWER-DOWN (RC = GND) Figure 10



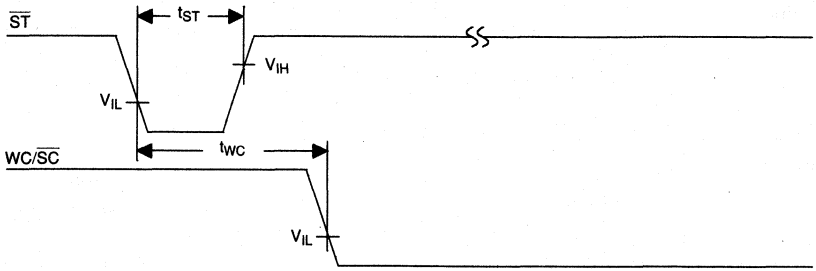
NMOS MODE POWER-UP (RC = GND) Figure 11



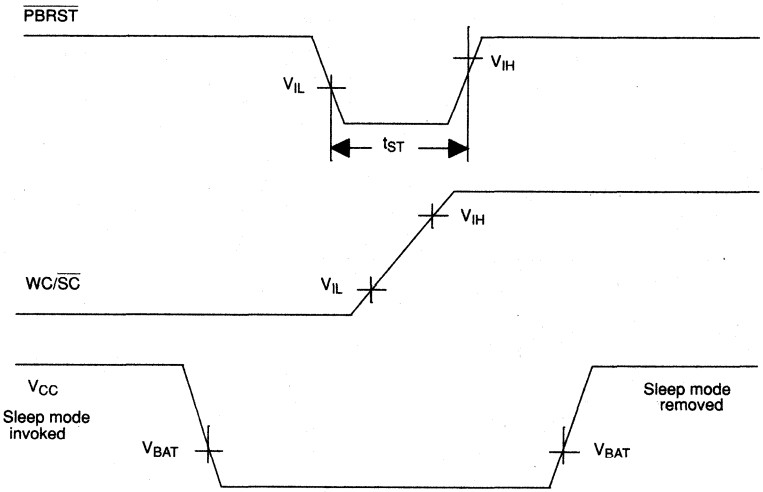
CMOS MODE POWER-UP (RC = V_{CCO}) Figure 12



WAKE/SLEEP CONTROL Figure 13



OPTIONS FOR INVOKING WAKEUP Figure 14



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	–0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	0°C to 70°C
Operating Temperature (Industrial Version)	–40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Supply Voltage (5% Option)	V_{CC}	4.75	5.0	5.5	V	1
Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	1
Input Low Level	V_{IL}	-0.3		+0.8	V	1
IN Input Pin	V_{IN}	-0.3		V_{CC} +0.3	V	1
Battery Input	V_{BAT}	0		4.0	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=4.5 V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}			4	mA	2
Sleep Supply Current in Sleep Mode	I_{CC}			20	µA	
Battery Current	I_{BAT}			0.1	µA	2
Supply Output Current (V_{CCO}=V_{CC} - 0.3V)	I_{CC01}			100	mA	3
Supply Output Current in Data Retention (V_{CC} < V_{BAT})	I_{CC02}			1	mA	4
Supply Output Voltage	V_{CCO}		V_{CC} -0.3		V	1
Battery Backup Voltage	V_{CCO}		V_{BAT} -0.7		V	1,6
Low Level @ RST	V_{OL}			0.4	V	1
Output Voltage @ –500 µA	V_{OH}	V_{CC}–0.5V	V_{CC}–0.1V		V	1
$\overline{CEO}$ and PF Output	V_{OHL}		V_{BAT} -0.7		V	1,6,19
$\overline{PBRST}$ Pull Up Resistor	R_{PBRST}	10K			Ω	
Input Leakage Current	I_{LI}	-1.0		+1.0	µA	18
Output Leakage	I_{LO}	-1.0		+1.0	µA	18
Output Current @0.4V	I_{OL}			4.0	mA	12
Output Current @2.4V	I_{OH}	-1.0			mA	13
Power Sup. Trip Point	V_{CCTP}	4.25	4.37	4.50	V	1
Power Supply Trip (5% Option)	V_{CCTP}	4.50	4.62	4.75	V	1
IN Input Pin Current	I_{CCIN}	-1.0		+1.0	µA	
IN Input Trip Point	V_{TP}	2.5	2.54	2.6	V	1

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Fail Detect to RST, $\overline{RST}$	t_{RPD}	40	100	175	µs	
V_{TP} to $\overline{NMI}$	t_{IPD}	40	100	175	µs	
RESET Active Time	t_{RST}	25	100	150	ms	
$\overline{NMI}$ Pulse Width	t_{NMI}	200	300	500	µs	14
$\overline{ST}$ Pulse Width	t_{ST}	20			ns	20
$\overline{PBRST}$ @ V_{IL}	t_{PB}	30			ms	
V_{CC} Slew Rate 4.75 to 4.25	t_F	300			µs	
Chip Enable Propagation Delay	t_{PD}			20	ns	
V_{CC} Fail to Chip Enable High	t_{CF}	7	12	44	µs	17
V_{CC} Valid to RST, $\overline{RST}$ (RC=1)	t_{FPU}			100	ns	
V_{CC} Valid to RST & $\overline{RST}$	t_{RPU}	25	100	150	ms	5
V_{CC} Slew to 4.24 to V_{BAT}	t_{FB1}	10			µs	7
V_{CC} Slew 4.25 to 4.75 V_{BAT}	t_{FB2}	100			µs	8
Chip Enable Output Recovery Time	t_{REC}	.1			µs	9
V_{CC} Slew 4.25 to 4.75	t_R	0			µs	
Chip Enable Pulse Width	t_{CE}			5	s	10
Watchdog Time Delay	t_{TD}	100	400	600	ms	
$\overline{ST}$ to WC/$\overline{SC}$	t_{WC}	0.1		50	µs	
V_{BAT} Detect to PF, $\overline{PF}$	t_{PPF}			2	µs	7
$\overline{ST}$ to $\overline{NMI}$	t_{STN}			30	ns	11
$\overline{NMI}$ to RST & $\overline{RST}$	t_{NRT}			30	ns	
V_{BAT} Detect to RST & $\overline{RST}$	t_{ARST}			200	µs	15
V_{CC} Valid to RST, $\overline{RST}$	t_{BRST}	30	100	150	µs	16

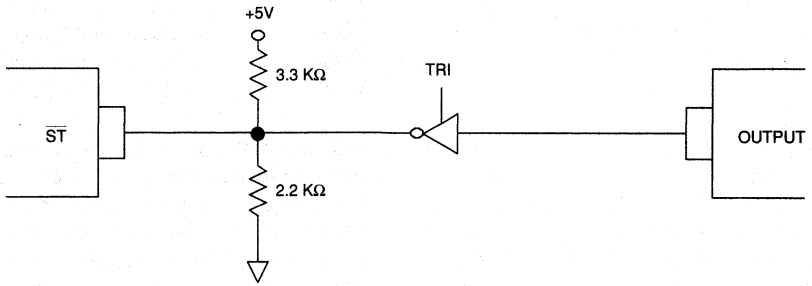
CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

NOTES:

1. All voltages referenced to ground. A 0.1 µF capacitor is recommended between V_{CC} and GND.
2. Measured with V_{CCO}, $\overline{CEO}$, $\overline{PF}$, PF, $\overline{ST}$, $\overline{PBRST}$, RST, $\overline{RST}$, and $\overline{NMI}$ pin open. I_{BAT} specified at 25°C.
3. I_{CCO1} is the maximum average load which the DS1236A can supply at V_{CC}-0.3V through the V_{CCO} pin during normal 5-volt operation.
4. I_{CCO2} is the maximum average load which the DS1236A can supply through the V_{CCO} pin during data retention battery supply operation, with a maximum drop of 0.8 volts.
5. With t_R = 5 µs.
6. V_{CCO} is approximately V_{BAT}-0.5V at 1 µA load.
7. Sleep mode is not invoked.
8. Sleep mode is invoked.
9. t_{REC} is the minimum time required before $\overline{CEI}$/$\overline{CEO}$ memory access is allowed.
10. t_{CE} maximum must be met to ensure data integrity on power loss.
11. IN input is less than V_{TP} but V_{CC} greater than V_{CCTP}.
12. All outputs except RST which is 25 µA maximum.
13. All outputs except $\overline{RST}$ and $\overline{NMI}$, which is 25 µA minimum.
14. Pulse width of $\overline{NMI}$ requires that the IN pin remain below V_{TP}. If the IN pin returns to a level above V_{TP} for a period longer than t_{IPD} and before the t_{NMI} period has elapsed, the $\overline{NMI}$ pin will immediately return to a high.
15. IN pin greater than V_{TP} when V_{CC} supply rises to V_{BAT}. Example: IN tied to GND.
16. IN pin less than V_{TP} when V_{CC} supply rises to V_{BAT}.
17. $\overline{CEI}$ low.
18. The WC/$\overline{SC}$ pin contains an internal latch which drives back on to the pin. This latch requires ±200 µamps to switch states. The $\overline{ST}$ pin will sink ±50 uamps in normal operation and ±1 µamp in the sleep mode.
19. If no battery is attached (i.e., V_{BAT}=GND) then V_{OHL} will track V_{CC}.
20. $\overline{ST}$ should be active low before the watchdog is disabled (i.e., before the $\overline{ST}$ input is tristated).



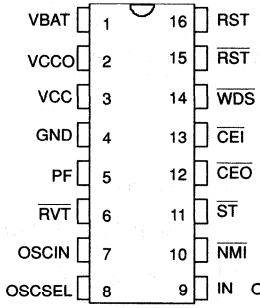
DALLAS SEMICONDUCTOR

DS1238 MicroManager

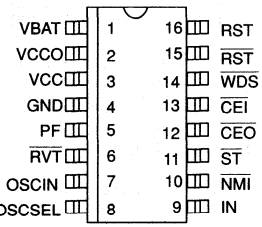
FEATURES

- Holds microprocessor in check during power transients
- Halts and restarts an out-of-control microprocessor
- Warns microprocessor of an impending power failure
- Converts CMOS SRAM into nonvolatile memory
- Unconditionally write protects memory when power supply is out of tolerance
- Delays write protection until completion of the current memory cycle
- Consumes less than 200 nA of battery current
- Controls external power switch for high current applications
- Debounces pushbutton reset
- Accurate 10% power supply monitoring
- Optional 5% power supply monitoring designated DS1238-5
- Provides orderly shutdown ini mcroprocessor applications
- Pin-for-pin compatible with MAX691
- Standard 16-pin DIP or space-saving 16-pin SOIC
- Optional industrial temperature range -40°C to +85°C

PIN ASSIGNMENT



16-Pin DIP (300 Mil.)
See Mech. Drawing
Pg 480



16-Pin SOIC (300 Mil.)
See Mech. Drawing
Pg 484

PIN DESCRIPTION

V_{BAT}	–	+3 Volt Battery Input
V_{CCO}	–	Switched SRAM Supply Output
V_{CC}	–	+5 Volt Power Supply Input
GND	–	Ground
PF	–	Power Fail
$\overline{RVT}$	–	Reset Voltage Threshold
OSCIN	–	Oscillator In
OSCSEL	–	Oscillator Select
IN	–	Early Warning Input
$\overline{NMI}$	–	Non–Maskable Interrupt
$\overline{ST}$	–	Strobe Input
$\overline{CEO}$	–	Chip Enable Output
$\overline{CEI}$	–	Chip Enable Input
$\overline{WDS}$	–	Watchdog Status
$\overline{RST}$	–	Reset Output (active low)
RST	–	Reset Output (active high)

DESCRIPTION

The DS1238 MicroManager provides all the necessary functions for power supply monitoring, reset control, and memory backup in microprocessor-based systems. A precise internal voltage reference and comparator circuit monitor power supply status. When an out-of-tolerance condition occurs, the microprocessor reset and power fail outputs are forced active, and static RAM control unconditionally write protects external memory. The DS1238 also provides early warning detection of a user-defined threshold by driving a non-maskable interrupt. External reset control is provided by a pushbutton reset debounce circuit connected to the $\overline{RST}$ pin. An internal watchdog timer can also force the reset outputs to the active state if the strobe input is not driven low prior to watchdog timeout. Oscillator control pins OSCSEL and OSCIN provide either external or internal clock timing for both the reset pulse width and the watchdog timeout period. The Watchdog Status and Reset Voltage Threshold are provided via $\overline{WDS}$ and $\overline{RVT}$, respectively. A block diagram of the DS1238 is shown in Figure 1.

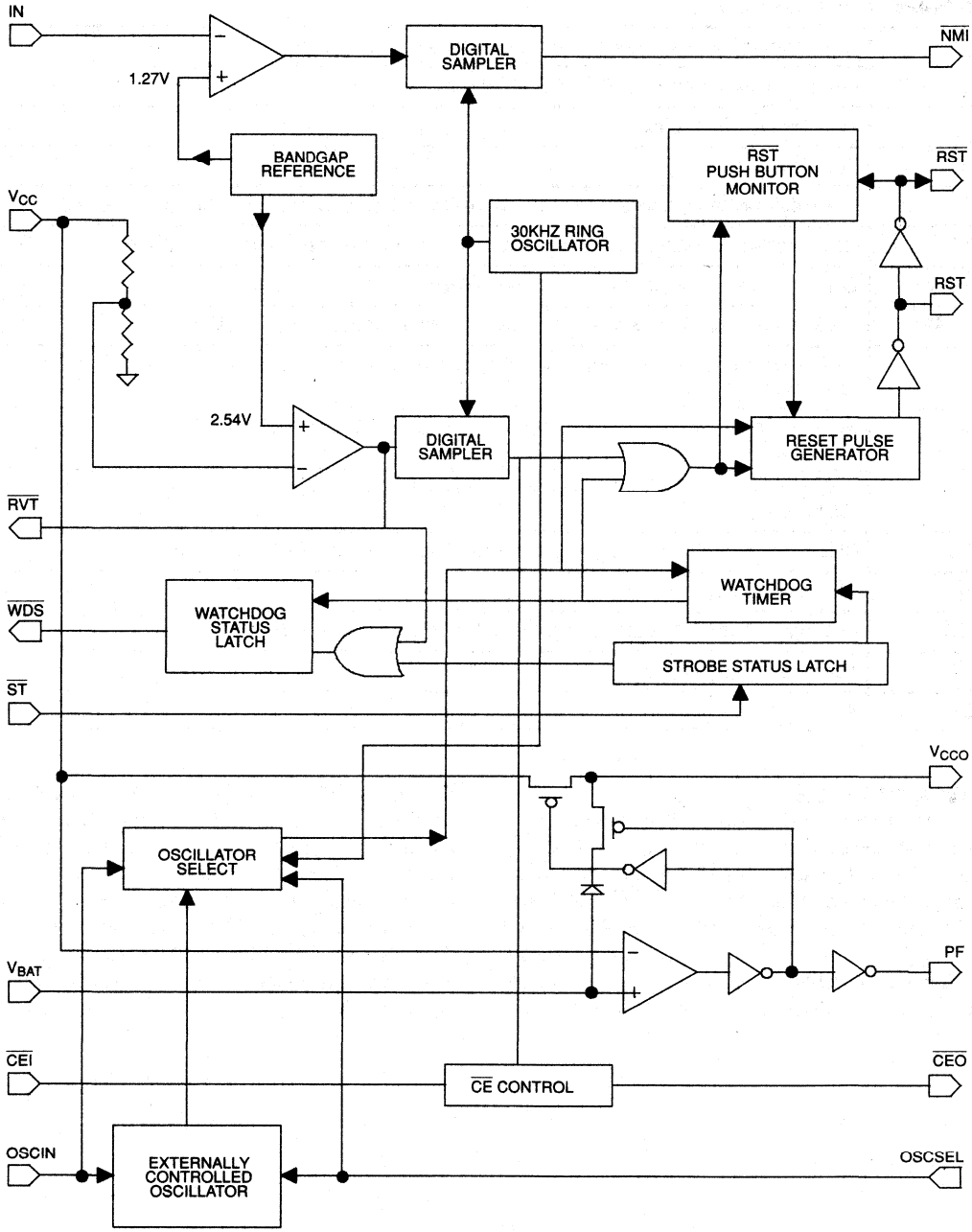
PIN DESCRIPTION

PIN NAME	DESCRIPTION
V_{BAT}	+3V Battery Input provides nonvolatile operation of control functions.
V_{CCO}	V_{CC} output for nonvolatile SRAM applications.
V_{CC}	+5V primary power input.
GND	System ground.
PF	Power fail indicator, active high, used for external power switching as shown in Figure 9.
$\overline{RVT}$	Reset Voltage Threshold. Indicates that V_{CC} is below the reset voltage threshold.
OSCIN	Oscillator input or timing capacitor. See Table 1.
OSCSEL	Oscillator Select. Selects internal or external clock functions. See Table 1.
IN	Early warning power fail input. This voltage sense point may be tied (via resistor divider) to a user-selected voltage.
$\overline{NMI}$	Non-maskable interrupt. Output used in conjunction with the IN pin to indicate an impending power failure.
$\overline{ST}$	Strobe input. A high–to–low transition will reset the watchdog timer, indicating that software is still in control.
$\overline{CEO}$	Chip enable output. Write protected. Used with nonvolatile SRAM applications.
$\overline{CEI}$	Chip enable input.
$\overline{WDS}$	Watchdog Status. Indicates that a watchdog timeout has occurred.
$\overline{RST}$	Active low reset output.
RST	Active high reset output.

POWER MONITOR

The DS1238 employs a band gap voltage reference and a precision comparator to monitor the 5–volt supply (V_{CC}) in microprocessor-based systems. When an out-of-tolerance condition occurs, the $\overline{RVT}$, RST, and $\overline{RST}$ outputs are driven to the active state. The V_{CC} trip point (V_{CCTP}) is set for 10% operation so that the $\overline{RVT}$, RST and $\overline{RST}$ outputs will become active as V_{CC} falls below 4.5 volts (4.37 typical). The V_{CCTP} for the 5% operation option (DS1238-5) is set for 4.75 volts (4.62 typical). The RST and $\overline{RST}$ signals are excellent for microprocessor reset control, as processing is stopped at the last possible moment of in-tolerance V_{CC}. On power up, $\overline{RVT}$ will become inactive as soon as V_{CC} rises above V_{CCTP}. However, the RST and $\overline{RST}$ signals remain active for a minimum of 50 ms (100 ms typical) after V_{CCTP} is reached to allow the power supply and microprocessor to stabilize.

DS1238 FUNCTIONAL BLOCK DIAGRAM Figure 1



WATCHDOG TIMER

The DS1238 provides a watchdog timer function which forces the $\overline{WDS}$, RST, and $\overline{RST}$ signals to the active state when the strobe input ($\overline{ST}$) is not stimulated for a predetermined time period. This time period is described below in Table 1. The watchdog timeout period begins as soon as RST and $\overline{RST}$ are inactive. If a high-to-low transition occurs at the $\overline{ST}$ input prior to time out, the watchdog timer is reset and begins to time out again. The $\overline{ST}$ input timing is shown in Figure 2. In order to guarantee that the watchdog timer does not timeout, a high-to-low transition on $\overline{ST}$ must occur at or less than the minimum timeout of the watchdog as described in the AC Electrical Characteristics. If the watchdog timer is allowed to time out, the $\overline{WDS}$, RST, and $\overline{RST}$ outputs are driven to the active state. $\overline{WDS}$ is a latched signal which indicates the watchdog status, and is activated as soon as the watchdog timer completes a full period as outlined in Table 1. The $\overline{WDS}$ pin will remain low until one of three operations occurs. The first is to strobe the $\overline{ST}$ pin with a falling edge, which will both set the $\overline{WDS}$ as well as the watchdog timer count. The second is to leave the $\overline{ST}$ pin open, which disables the watchdog. Lastly, the $\overline{WDS}$ pin is active low whenever V_{CC} falls below V_{CCTP} and activates the $\overline{RVT}$ signal. The $\overline{ST}$ input can be derived from microprocessor address, data, or control signals, as well as microcontroller port pins. Under normal operating conditions, these signals would routinely reset the watchdog timer prior to time out. The watchdog is disabled by leaving the $\overline{ST}$ input open, or as soon as V_{CC} falls to V_{CCTP}.

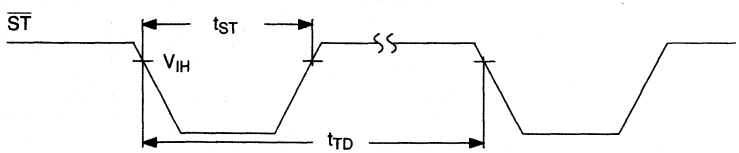
NON–MASKABLE INTERRUPT

The DS1238 generates a non-maskable interrupt ($\overline{NMI}$) for early warning of a power failure to the microprocessor. A precision comparator monitors the voltage level at the IN pin relative to an on-chip reference generated by an internal band gap. The IN pin is a high impedance input allowing for a user-defined sense point. An external resistor voltage divider network (Figure 5) is used to interface with high voltage signals. This sense point may be derived from the regulated 5-volt supply, or from a higher DC voltage level closer to the main system power input. Since the IN trip point V_{TP} is 1.27 volts, the proper values for R1 and R2 can be determined by the equation as shown in Figure 5. Proper operation of the DS1238 requires that the voltage at the IN pin be limited to V_{IH}. Therefore, the maximum allowable voltage at the supply being monitored (V_{MAX}) can also be derived as shown in Figure 5. A simple approach to solving this equation is to select a value for R2 of high enough value to keep power consumption low, and solve for R1. The flexibility of the IN input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time for microprocessor shut-down between $\overline{NMI}$ and RST or $\overline{RST}$.

When the supply being monitored decays to the voltage sense point, the DS1238 will force the $\overline{NMI}$ output to an active state. Noise is removed from the $\overline{NMI}$ power fail detection circuitry using built-in time domain hysteresis. That is, the monitored supply is sampled periodically at a rate determined by an internal ring oscillator running at approximately 30 KHz (33 µs/cycle). Three consecutive samplings of out-of-tolerance supply (below V_{SENSE}) must occur at the IN pin to active $\overline{NMI}$. Therefore, the supply must be below the voltage sense point for approximately 100 µs or the comparator will reset. In this way, power supply noise is removed from the monitoring function preventing false trips. During a power–up, any IN pin levels below V_{TP} detected by the comparator are disabled from reaching the $\overline{NMI}$ pin until V_{CC} rises to V_{CCTP}. As a result, any potential active $\overline{NMI}$ will not be initiated until V_{CC} reaches V_{CCTP}.

Removal of an active low level on the $\overline{NMI}$ pin is controlled by the subsequent rise of the IN pin above V_{TP}. The initiation and removal of the $\overline{NMI}$ signal during power up depends on the relative voltage relationship between V_{CC} and the IN pin voltage. Note that a fast slewing power supply may cause the $\overline{NMI}$ to be virtually non-existent on power up. This is of no consequence however, since an RST will be active. The $\overline{NMI}$ voltage will follow V_{CC} down until V_{CC} decays to V_{BAT}. Once V_{CC} decays to $V\overline{BAT}$, the $\overline{NMI}$ pin will enter a tri-state mode.

$\overline{ST}$ INPUT TIMING Figure 2

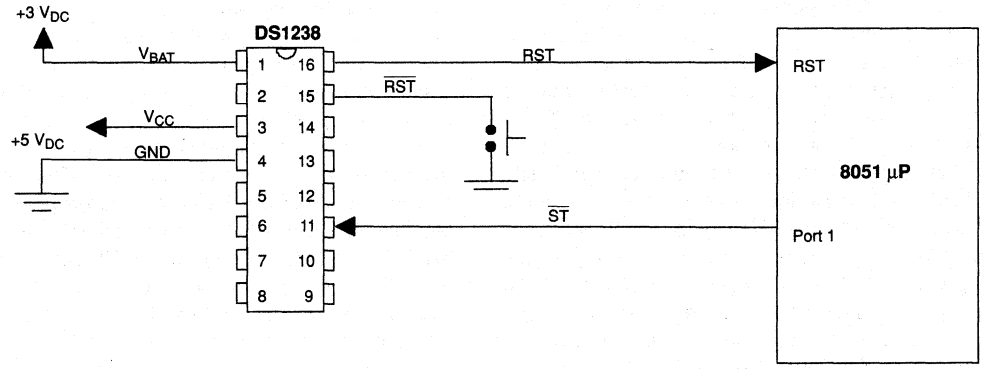


OSCILLATOR CONTROLS Table 1

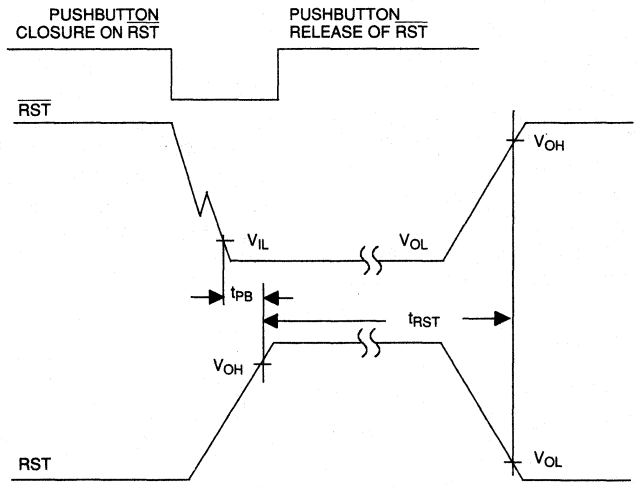
	OSCIN	OSCSEL	Watchdog Timeout Period (typ)		
			First Period Following a Reset	Other Timeout	Reset Active Duration
External	Ext Clk	Low	20480 Clks	5120 Clocks	641 Clks
	Ext Cap	Low	$\cong \frac{2.2\ \text{sec}}{47\ \text{pf}} \times \text{Cpf}$	$\cong \frac{550\ \text{ms}}{47\ \text{pf}} \times \text{Cpf}$	$\cong \frac{69\ \text{ms}}{47\ \text{pf}} \times \text{Cpf}$
Internal	Low	Hi/Open	2.7 sec	170 ms	85 ms
	Hi/Open	Hi/Open	2.7 sec	2.7 sec	85 ms

Note that the OSCIN and OSCSEL pins are tri-stated when V_{CC} is below V_{BAT}.

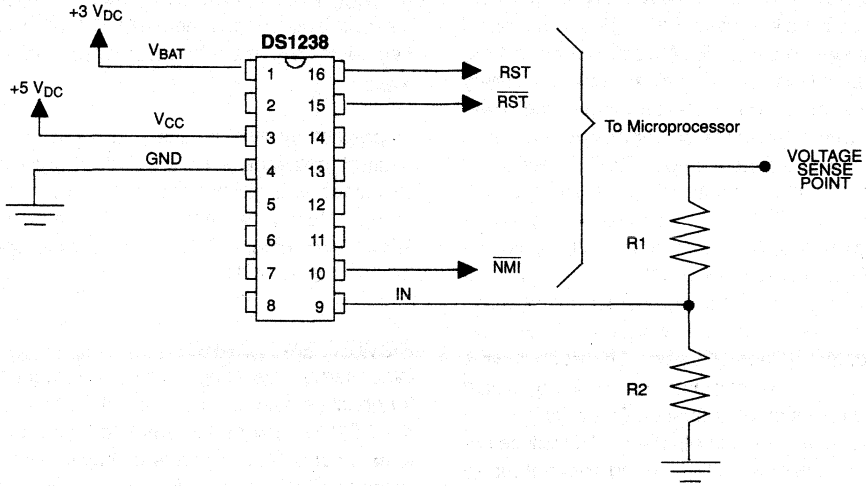
POWER MONITOR, WATCHDOG TIMER, AND PUSHBUTTON RESET Figure 3



PUSHBUTTON RESET TIMING Figure 4



NON-MASKABLE INTERRUPT Figure 5



$$V_{SENSE} = \frac{R1 + R2}{R2} \times 1.27$$

$$MAXVOLTAGE = \frac{V_{SENSE}}{1.27} \times 5.0 = VMAX$$

Example 1: 5 Volt Supply, R2 = 10K Ohms, V_{SENSE} = 4.8 Volts

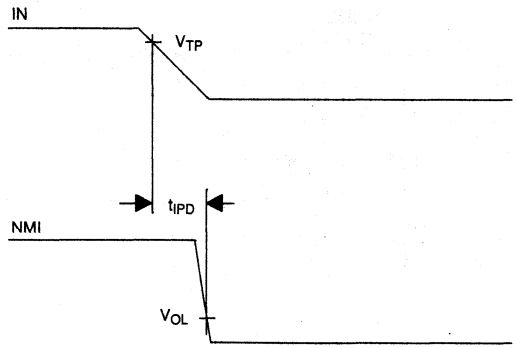
$$4.8 = \frac{R1 + 10K}{10K} \times 1.27 \geq R1 = 27.8K \text{ Ohm}$$

Example 2: 12 Volt Supply, R2 = 10K Ohms, V_{SENSE} = 9.0 Volts

$$9.0 = \frac{R1 + 10K}{10K} \times 1.27 \geq R1 = 60.9K \text{ Ohm}$$

$$V_{MAX} = \frac{9.00}{1.27} \times 5.0 = 35.4 \text{ Volts}$$

NMI FROM IN INPUT Figure 6



MEMORY BACKUP

The DS1238 provides all of the necessary functions required to battery back a static RAM. First, an internal switch is provided to supply SRAM power from the primary 5-volt supply (V_{CC}) or from an external battery (V_{BAT}), whichever is greater. Second, the same power fail detection described in the power monitor section is used to hold the chip enable output ($\overline{CEO}$) to within 0.3 volts of V_{CC} or to within 0.7 volts of V_{BAT}. The output voltage diode drop from V_{BAT} (0.7 V) is necessary to prevent charging of the battery in violation of UL standards. Write protection occurs as V_{CC} falls below V_{CCTP} as specified. If $\overline{CEI}$ is low at the time power fail detection occurs, $\overline{CEO}$ is held in its present state until $\overline{CEI}$ is returned high, or the period t_{CE} expires. This delay of write protection until the current memory cycle is completed prevents the corruption of data. If $\overline{CEO}$ is in an inactive state at the time of V_{CC} fail detection, $\overline{CEO}$ will be unconditionally disabled within t_{CF}. During nominal supply conditions $\overline{CEO}$ will follow $\overline{CEI}$ with a maximum propagation delay of 20 ns. Figure 7 shows a typical nonvolatile SRAM application.

FRESHNESS SEAL

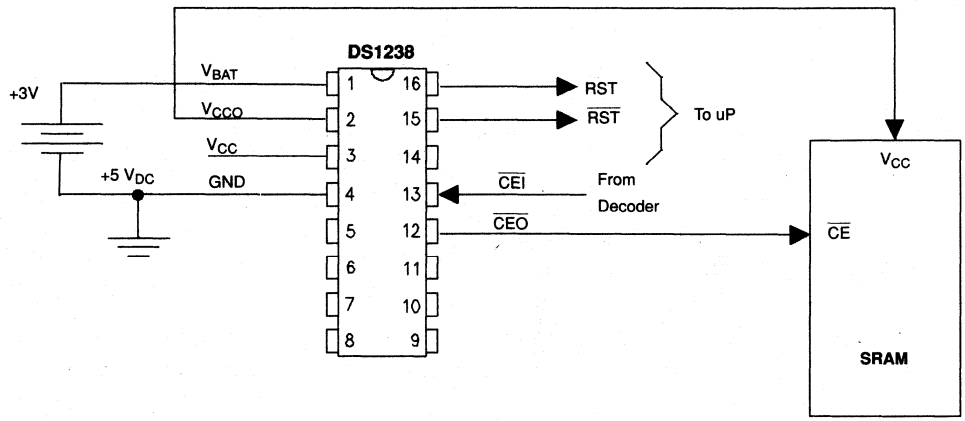
In order to conserve battery capacity during storage and/or shipment of an end system, the DS1238 provides an internal freshness seal to electrically disconnect the battery. Figure 8 depicts the three pulses below ground on the IN pin required to invoke the freshness seal. The freshness seal will result in the tri-state of outputs V_{CCO}, RST, $\overline{RST}$, and $\overline{CEO}$. The $\overline{WDS}$ output will be driven active low. The PF pin is not disabled by the freshness mode and will continue to source power from the V_{BAT} pin whenever V_{CC} is below V_{BAT}. The freshness seal will be disconnected and normal operation will begin when V_{CC} is cycled and reapplied to a level above V_{BAT}.

To prevent negative pulses associated with noise from setting the freshness mode in system applications, a series diode and resistor can be used to shunt noise to ground. During manufacturing, the freshness seal can still be set by holding TP2 at -3 volts while applying the 0 to -3-volt clock to TP1.

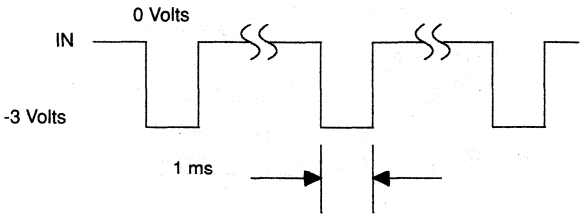
POWER SWITCHING

When larger operating currents are required in a battery-backed system, the internal switching devices of the DS1238 may be too small to support the required load through V_{CCO} with a reasonable voltage drop. For these applications, the PF output is provided to gate external power switching devices. As shown in Figure 9, power to the load is switched from V_{CC} to battery on power down, and from battery to V_{CC} on power up. The DS1336 is designed to use the PF output to switch between V_{BAT} and V_{CC}. It provides better leakage and switchover performance than currently available discrete components. The transition threshold for PF is set to the external battery voltage V_{BAT}, allowing a smooth transition between sources. Any load applied to the PF pin by an external switch will be supplied by the battery. Therefore, if a discrete switch is used, this load should be taken into consideration when sizing the battery.

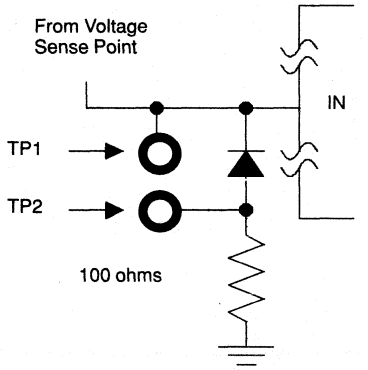
NONVOLATILE SRAM Figure 7



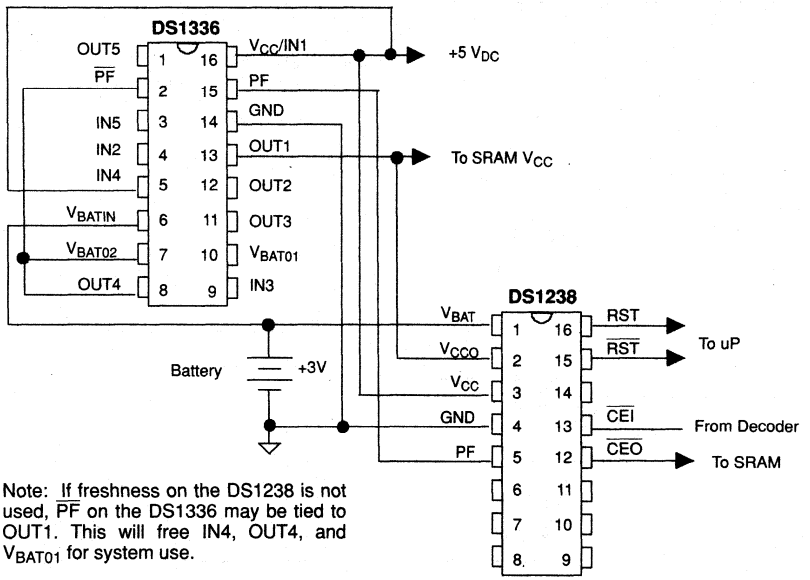
FRESHNESS SEAL Figure 8



Note: This series of pulses must be applied during normal +5 volt operation.



POWER SWITCHING Figure 9



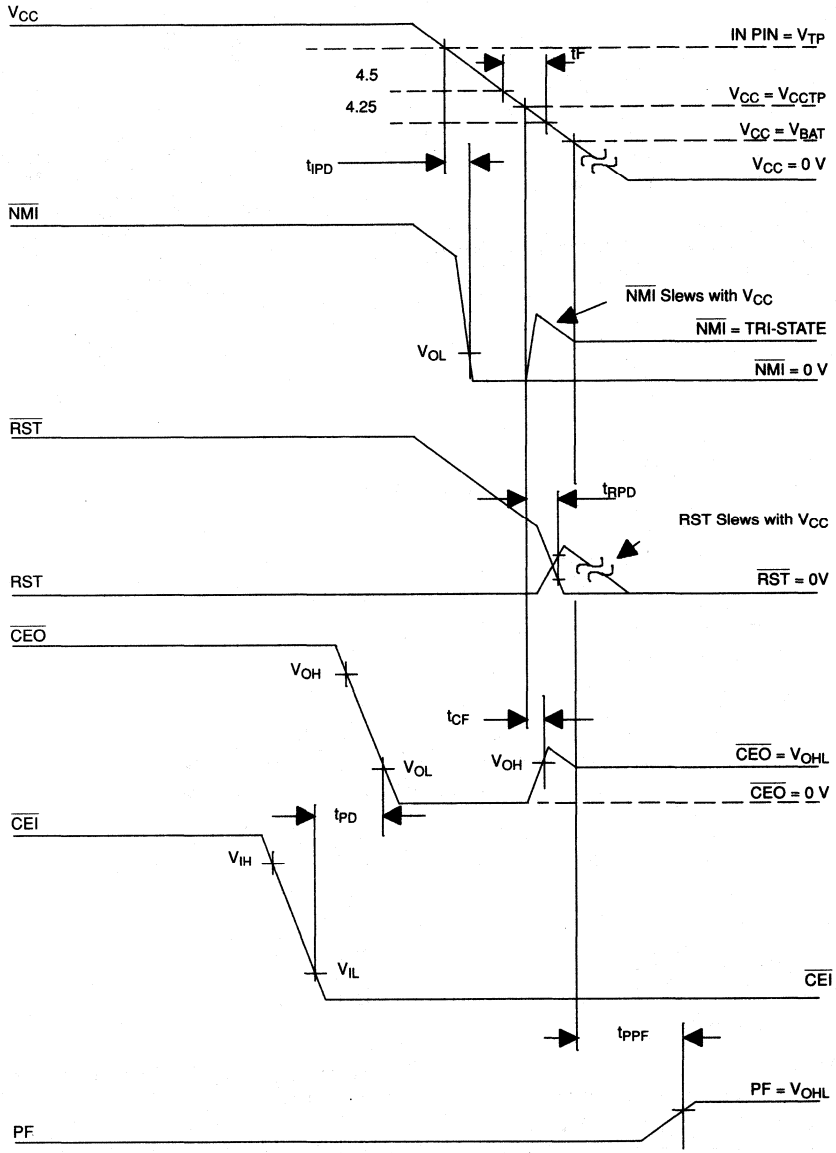
Note: If freshness on the DS1238 is not used, $\overline{PF}$ on the DS1336 may be tied to OUT1. This will free IN4, OUT4, and V_{BAT01} for system use.

TIMING DIAGRAMS

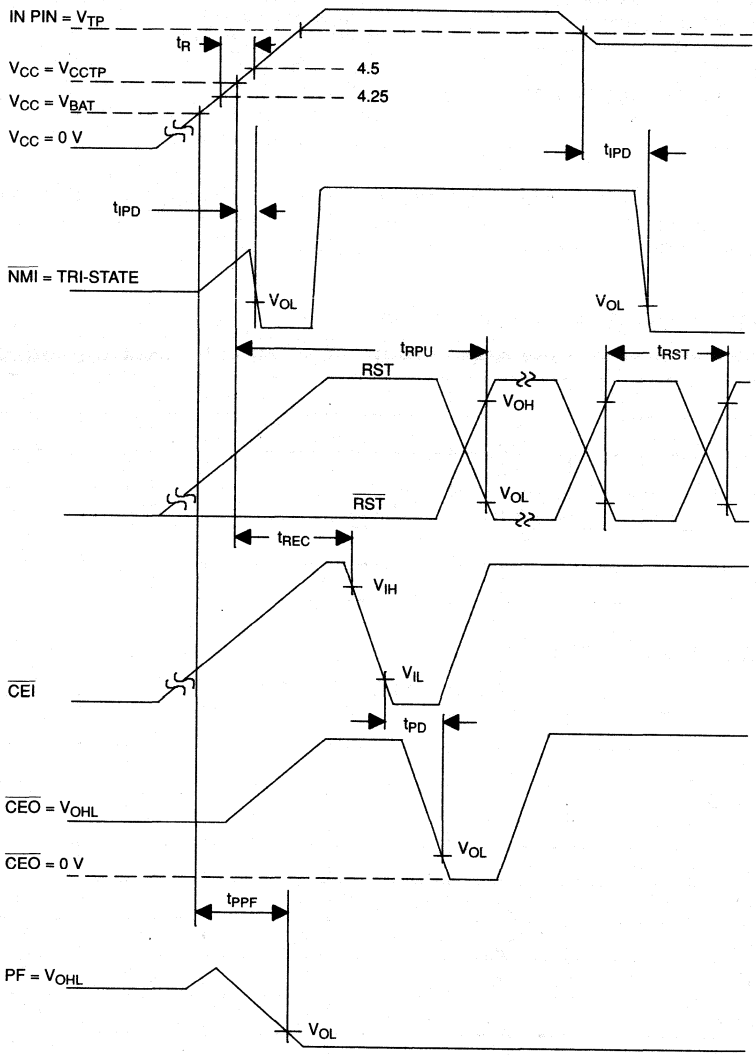
This section provides a description of the timing diagrams shown in Figure 10 and Figure 11. Figure 10 illustrates the relationship for power down. As V_{CC} falls, the IN pin voltage drops below V_{TP}. As a result, the processor is notified of an impending power failure via an active $\overline{NMI}$. This gives the processor time to save critical data in nonvolatile SRAM. As the power falls further, V_{CC} crosses V_{CCTP}, the power monitor trip point. When V_{CC} reaches V_{CCTP}, and active RST and $\overline{RST}$ are given. At this time, $\overline{CEO}$ is brought high to write protect the RAM. When the V_{CC} reaches V_{BAT}, a power fail is issued via the PF pin.

Figure 11 shows the power up sequence. As V_{CC} slews above V_{BAT}, the PF pin is deactivated. An active reset occurs as well as an $\overline{NMI}$. Although the $\overline{NMI}$ may be short due to slew rates, reset will be maintained for the standard t_{RPU} timeout period. At a later time, if the IN pin falls below V_{TP}, a new $\overline{NMI}$ will occur. If the processor does not issue an $\overline{ST}$, a watchdog reset will also occur. The second $\overline{NMI}$ and RST are provided to illustrate these possibilities.

POWER DOWN TIMING Figure 10



POWER UP TIMING Figure 11



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	–0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Voltage on IN Pin Relative to Ground	–3.5V to V_{CC} + 0.5V
Operating Temperature	0°C to 70°C
Operating Temperature (Industrial Version)	–40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Supply Voltage (5% Option)	V_{CC}	4.75	5.0	5.5	V	1
Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	1
Input Low Level	V_{IL}	-0.3		+0.8	V	1
IN Input Pin	V_{IN}	0		V_{CC}	V	1
Battery Input	V_{BAT}	2.7		4.0	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}			4	mA	2
Battery Current	I_{BAT}	0		200	nA	2, 12
Supply Output Current (V_{CCO} = V_{CC} - 0.3V)	I_{CC01}			100	mA	3
Supply Out Current (V_{CC} < V_{BAT})	I_{CC02}			1	mA	4
Supply Output Voltage	V_{CCO}	V_{CC} -0.3			V	1
Battery Back Voltage	V_{CCO}		V_{BAT} -0.8		V	6
Low Level @ RST	V_{OL}			0.4	V	1
Output Voltage @ –500 µA	V_{OH}	V_{CC}–0.5V	V_{CC}–0.1V		V	1
$\overline{CEO}$ and PF Output	V_{OHL}		V_{BAT} -0.8		V	6
Input Leakage Current	I_{LI}	-1.0		+1.0	µA	121
Output Leakage	I_{LO}	-1.0		+1.0	µA	
Output Current @0.4V	I_{OL}			4.0	mA	9
Output Current @2.4V	I_{OH}	-1.0			mA	10
Power Sup. Trip Point	V_{CCTP}	4.25	4.37	4.50	V	1
Power Supply Trip (5% Option)	V_{CCTP}	4.50	4.62	4.75	V	
IN Input Pin Current	I_{CCIN}	-1.0		+1.0	µA	
IN Input Trip Point	V_{TP}	1.15	1.27	1.35	V	1

AC ELECTRICAL CHARACTERISTIC

(0°C to 70°C; V_{CC} = 5V± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Fall Detect to RST, $\overline{RST}$	t_{RPD}	40	100	175	µs	
V_{TP} to $\overline{NMI}$	t_{IPD}	40	100	175	µs	
RESET Active OSCSEL=high	t_{RST}	40	85	150	ms	
$\overline{ST}$ Pulse Width	t_{ST}	20			ns	13
PBRST @ V_{IL}	t_{PB}	30			ms	
V_{CC} Slew Rate 4.75 to 4.25	t_F	300			µs	
Chip Enable Prop Delay	t_{PD}			20	ns	
V_{CC} Fail to Chip Enable High	t_{CF}	7	12	144	µs	11
V_{CC} Valid to RST (RC = 1)	t_{FPU}			100	ns	
V_{CC} Valid to RST	t_{RPU}	40	100	150	ms	5
V_{CC} Slew to 4.25 to V_{BAT}	t_{FB1}	10			µs	
Chip Enable Output Recovery Time	t_{REC}	.1			µs	7
V_{CC} Slew 4.25 to 4.75	t_R	0			µs	
Chip Enable Pulse Width	t_{CE}			5	µs	8
Watchdog Time Delay int clock Long period	t_{TD}	1.7	2.7		s	
Short period		110	170		ms	
Watchdog Time Delay, ext clock, After reset	t_{TD}		20480		clocks	
Normal			5120		clocks	
V_{BAT} Detect to PF	t_{PPF}			2	µs	
OSC IN Frequency	f_{OSC}	0		250	KHz	

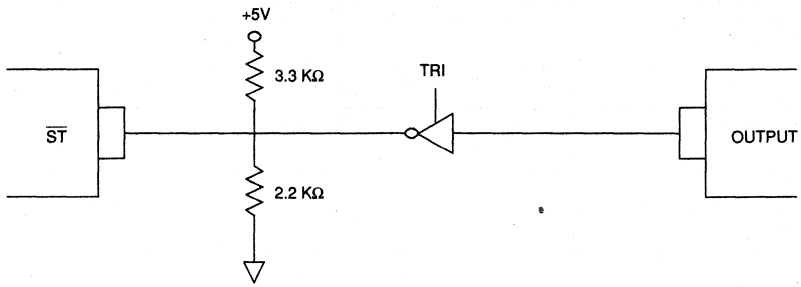
CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

NOTES:

1. All voltages referenced to ground.
2. Measured with V_{CCO}, $\overline{CEO}$, PF, $\overline{ST}$, RST, $\overline{RST}$, and $\overline{NMI}$ pin open.
3. I_{CCO1} is the maximum average load which the DS1238 can supply at V_{CC}-.3V through the V_{CCO} pin during normal 5-volt operation.
4. I_{CCO2} is the maximum average load which the DS1238 can supply through the V_{CCO} pin during data retention battery supply operation, with a maximum drop of 0.8 volts for commercial, 1.0V for industrial.
5. With t_R = 5 µs.
6. V_{CCO} is approximately V_{BAT}-0.5V at 1 µA load.
7. t_{REC} is the minimum time required before $\overline{CEI}/\overline{CEO}$ memory access is allowed.
8. t_{CE} maximum must be met to insure data integrity on power loss.
9. All outputs except RST which is 25 µA max.
10. All outputs except $\overline{RST}$, $\overline{RVT}$, and $\overline{NMI}$ which is 25 µA min.
11. The $\overline{ST}$ pin will sink ±50 µA in normal operation. The OSCIN pin will sink ±5 µA in normal operation. The OSCSEL pin will sink ±10 µA in normal operation.
12. I_{BAT} is measured with V_{BAT}=3.0V.
13. $\overline{ST}$ should be active low before the watchdog is disabled (i.e., before the $\overline{ST}$ input is tristated).



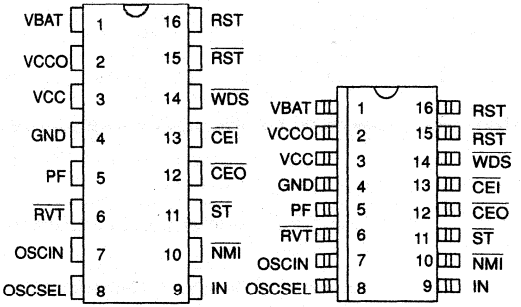
DALLAS SEMICONDUCTOR

DS1238A MicroManager

FEATURES

- Holds microprocessor in check during power transients
- Halts and restarts an out-of-control microprocessor
- Warns microprocessor of an impending power failure
- Converts CMOS SRAM into nonvolatile memory
- Unconditionally write protects memory when power supply is out of tolerance
- Delays write protection until completion of the current memory cycle
- Consumes less than 200 nA of battery current
- Controls external power switch for high current applications
- Debounces pushbutton reset
- Accurate 10% power supply monitoring
- Optional 5% power supply monitoring designated DS1238A-5
- Provides orderly shutdown in microprocessor applications
- Pin-for-pin compatible with MAX691
- Standard 16-pin DIP or space-saving 16-pin SOIC
- Optional industrial temperature range -40°C to +85°C

PIN ASSIGNMENT



16-Pin DIP (300 Mil.) See Mech. Drawing Pg. 480

16-Pin SOIC (300 Mil.) See Mech. Drawing Pg. 484

PIN DESCRIPTION

V_{BAT}	–	+3 Volt Battery Input
V_{CCO}	–	Switched SRAM Supply Output
V_{CC}	–	+5 Volt Power Supply Input
GND	–	Ground
PF	–	Power Fail
$\overline{RVT}$	–	Reset Voltage Threshold
OSCIN	–	Oscillator In
OSCSEL	–	Oscillator Select
IN	–	Early Warning Input
$\overline{NMI}$	–	Non–Maskable Interrupt
$\overline{ST}$	–	Strobe Input
$\overline{CEO}$	–	Chip Enable Output
$\overline{CEI}$	–	Chip Enable Input
$\overline{WDS}$	–	Watchdog Status
$\overline{RST}$	–	Reset Output (active low)
RST	–	Reset Output (active high)

DESCRIPTION

The DS1238A MicroManager provides all the necessary functions for power supply monitoring, reset control, and memory backup in microprocessor-based systems. A precise internal voltage reference and comparator circuit monitor power supply status. When an out-of-tolerance condition occurs, the microprocessor reset and power fail outputs are forced active, and static RAM control unconditionally write protects external memory. The DS1238A also provides early warning detection of a user-defined threshold by driving a nonmaskable interrupt. External reset control is provided by a pushbutton reset debounce circuit connected to the $\overline{RST}$ pin. An internal watchdog timer can also force the reset outputs to the active state if the strobe input is not driven low prior to watchdog timeout. Oscillator control pins OSCSEL and OSCIN provide either external or internal clock timing for both the reset pulse width and the watchdog timeout period. The Watchdog Status and Reset Voltage Threshold are provided via $\overline{WDS}$ and $\overline{RVT}$, respectively. A block diagram of the DS1238A is shown in Figure 1.

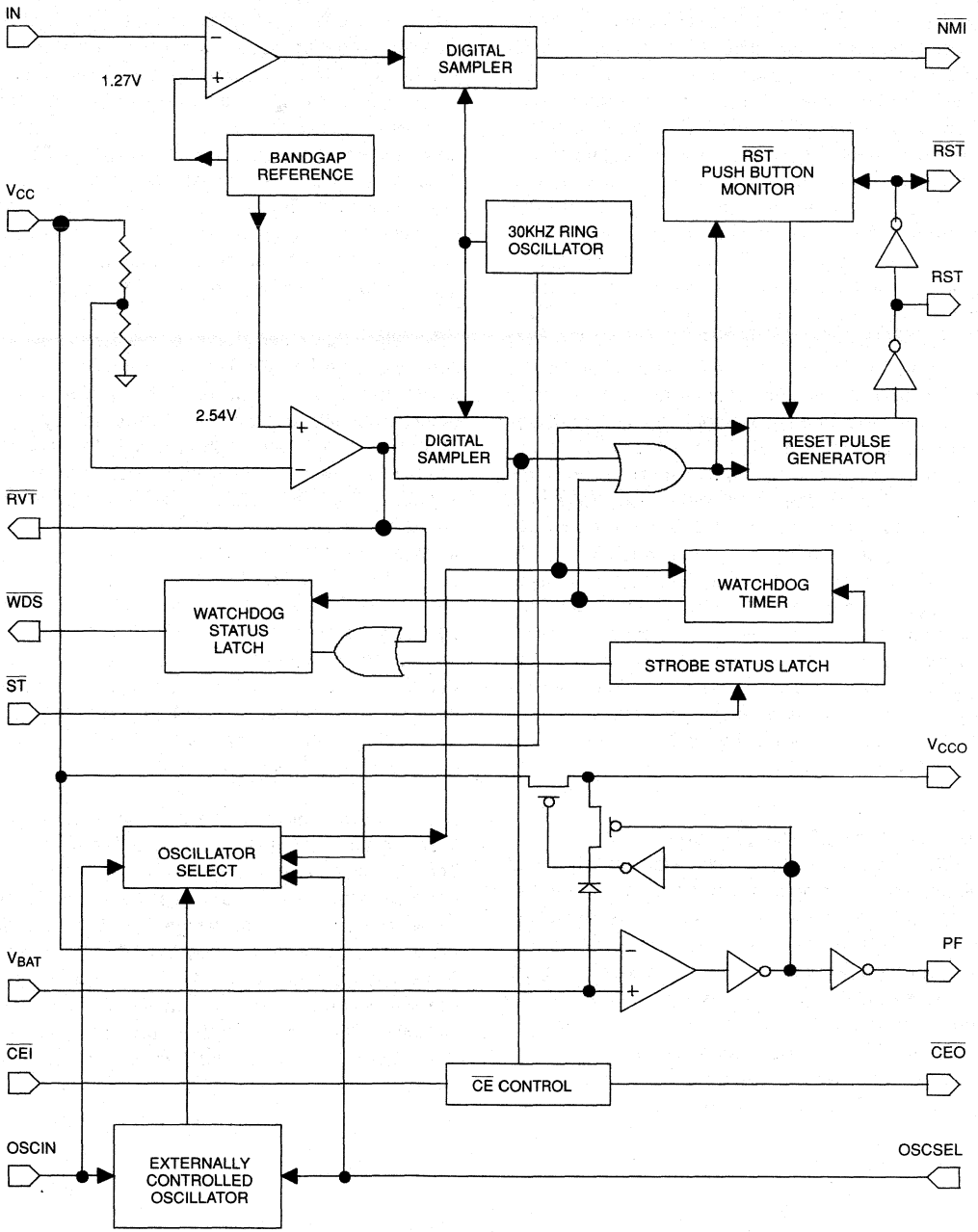
PIN DESCRIPTION

PIN NAME	DESCRIPTION
V_{BAT}	+3V Battery Input provides nonvolatile operation of control functions.
V_{CCO}	V_{CC} output for nonvolatile SRAM applications.
V_{CC}	+5V primary power input.
GND	System ground.
PF	Power fail indicator, active high, used for external power switching as shown in Figure 9.
$\overline{RVT}$	Reset Voltage Threshold. Indicates that V_{CC} is below the reset voltage threshold.
OSCIN	Oscillator input or timing capacitor. See Table 1.
OSCSEL	Oscillator Select. Selects internal or external clock functions. See Table 1.
IN	Early warning power fail input. This voltage sense point may be tied (via resistor divider) to a user-selected voltage.
$\overline{NMI}$	Non-maskable interrupt. Output used in conjunction with the IN pin to indicate an impending power failure.
$\overline{ST}$	Strobe input. A high–to–low transition will reset the watchdog timer, indicating that software is still in control.
$\overline{CEO}$	Chip enable output. Write protected. Used with nonvolatile SRAM applications.
$\overline{CEI}$	Chip enable input.
$\overline{WDS}$	Watchdog Status. Indicates that a watchdog timeout has occurred.
$\overline{RST}$	Active low reset output.
RST	Active high reset output.

POWER MONITOR

The DS1238A employs a band gap voltage reference and a precision comparator to monitor the 5–volt supply (V_{CC}) in microprocessor-based systems. When an out-of-tolerance condition occurs, the $\overline{RVT}$, RST, and $\overline{RST}$ outputs are driven to the active state. The V_{CC} trip point (V_{CCTP}) is set for 10% operation so that the $\overline{RVT}$, RST and $\overline{RST}$ outputs will become active as V_{CC} falls below 4.5 volts (4.37 typical). The V_{CCTP} for the 5% operation option (DS1238A-5) is set for 4.75 volts (4.62 typical). The RST and $\overline{RST}$ signals are excellent for microprocessor reset control, as processing is stopped at the last possible moment of in-tolerance V_{CC}. On power up, $\overline{RVT}$ will become inactive as soon as V_{CC} rises above V_{CCTP}. However, the RST and $\overline{RST}$ signals remain active for a minimum of 50 ms (100 ms typical) after V_{CCTP} is reached to allow the power supply and microprocessor to stabilize.

DS1238A FUNCTIONAL BLOCK DIAGRAM Figure 1



WATCHDOG TIMER

The DS1238A provides a watchdog timer function which forces the $\overline{WDS}$, RST, and $\overline{RST}$ signals to the active state when the strobe input ($\overline{ST}$) is not stimulated for a predetermined time period. This time period is described below in Table 1. The watchdog timeout period begins as soon as RST and $\overline{RST}$ are inactive. If a high-to-low transition occurs at the $\overline{ST}$ input prior to time out, the watchdog timer is reset and begins to time out again. The $\overline{ST}$ input timing is shown in Figure 2. In order to guarantee that the watchdog timer does not timeout, a high-to-low transition on $\overline{ST}$ must occur at or less than the minimum timeout of the watchdog as described in the AC Electrical Characteristics. If the watchdog timer is allowed to time out, the $\overline{WDS}$, RST, and $\overline{RST}$ outputs are driven to the active state. $\overline{WDS}$ is a latched signal which indicates the watchdog status, and is activated as soon as the watchdog timer completes a full period as outlined in Table 1. The $\overline{WDS}$ pin will remain low until one of three operations occurs. The first is to strobe the $\overline{ST}$ pin with a falling edge, which will both set the $\overline{WDS}$ as well as the watchdog timer count. The second is to leave the $\overline{ST}$ pin open, which disables the watchdog. Lastly, the $\overline{WDS}$ pin is active low whenever V_{CC} falls below V_{CCTP} and activates the $\overline{RVT}$ signal. The $\overline{ST}$ input can be derived from microprocessor address, data, or control signals, as well as microcontroller port pins. Under normal operating conditions, these signals would routinely reset the watchdog timer prior to time out. The watchdog is disabled by leaving the $\overline{ST}$ input open, or as soon as V_{CC} falls to V_{CCTP}.

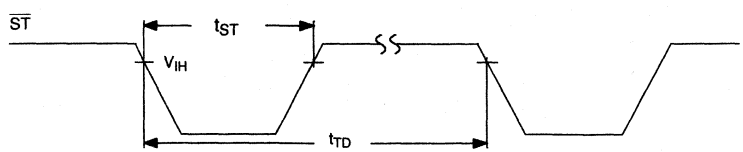
NON–MASKABLE INTERRUPT

The DS1238A generates a non-maskable interrupt ($\overline{NMI}$) for early warning of a power failure to the microprocessor. A precision comparator monitors the voltage level at the IN pin relative to an on-chip reference generated by an internal band gap. The IN pin is a high impedance input allowing for a user-defined sense point. An external resistor voltage divider network (Figure 5) is used to interface with high voltage signals. This sense point may be derived from the regulated 5-volt supply, or from a higher DC voltage level closer to the main system power input. Since the IN trip point V_{TP} is 1.27 volts, the proper values for R1 and R2 can be determined by the equation as shown in Figure 5. Proper operation of the DS1238A requires that the voltage at the IN pin be limited to V_{IH}. Therefore, the maximum allowable voltage at the supply being monitored (V_{MAX}) can also be derived as shown in Figure 5. A simple approach to solving this equation is to select a value for R2 of high enough value to keep power consumption low, and solve for R1. The flexibility of the IN input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time for microprocessor shut-down between $\overline{NMI}$ and RST or $\overline{RST}$.

When the supply being monitored decays to the voltage sense point, the DS1238A will force the $\overline{NMI}$ output to an active state. Noise is removed from the $\overline{NMI}$ power fail detection circuitry using built-in time domain hysteresis. That is, the monitored supply is sampled periodically at a rate determined by an internal ring oscillator running at approximately 30 KHz (33 µs/cycle). Three consecutive samplings of out-of-tolerance supply (below V_{SENSE}) must occur at the IN pin to active $\overline{NMI}$. Therefore, the supply must be below the voltage sense point for approximately 100 µs or the comparator will reset. In this way, power supply noise is removed from the monitoring function preventing false trips. During a power–up, any IN pin levels below V_{TP} detected by the comparator are disabled from reaching the $\overline{NMI}$ pin until V_{CC} rises to V_{CCTP}. As a result, any potential active $\overline{NMI}$ will not be initiated until V_{CC} reaches V_{CCTP}.

Removal of an active low level on the $\overline{NMI}$ pin is controlled by the subsequent rise of the IN pin above V_{TP}. The initiation and removal of the $\overline{NMI}$ signal during power up depends on the relative voltage relationship between V_{CC} and the IN pin voltage. Note that a fast slewing power supply may cause the $\overline{NMI}$ to be virtually non-existent on power up. This is of no consequence however, since an RST will be active. The $\overline{NMI}$ voltage will follow V_{CC} down until V_{CC} decays to V_{BAT}. Once V_{CC} decays to $\overline{VBAT}$, the $\overline{NMI}$ pin will enter a tri-state mode.

$\overline{ST}$ INPUT TIMING Figure 2

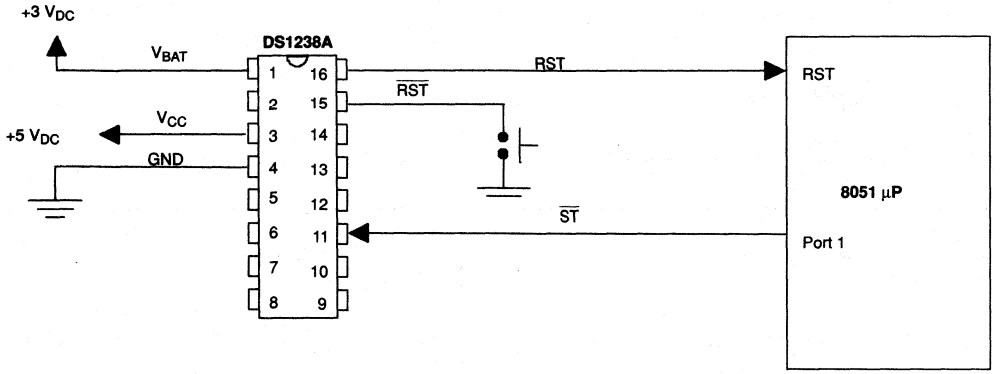


OSCILLATOR CONTROLS Table 1

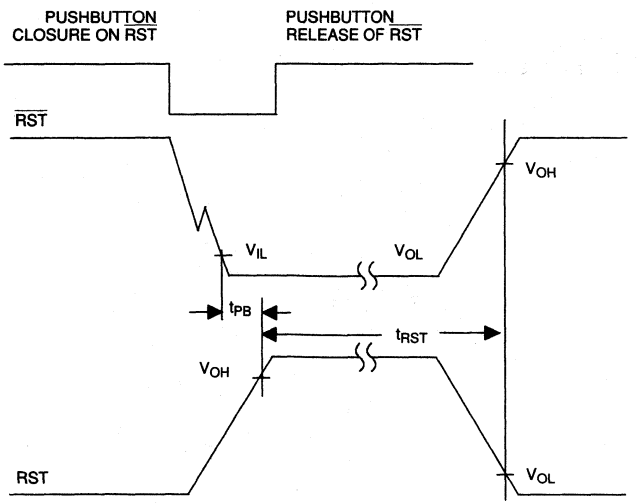
	OSCIN	OSCSEL	Watchdog Timeout Period (typ)		
			First Period Following a Reset	Other Timeout	Reset Active Duration
External	Ext Clk	Low	20480 Clks	5120 Clocks	641 Clks
	Ext Cap	Low	$\cong \frac{2.2\ \text{sec}}{47\ \text{pf}} \times \text{Cpf}$	$\cong \frac{550\ \text{ms}}{47\ \text{pf}} \times \text{Cpf}$	$\cong \frac{69\ \text{ms}}{47\ \text{pf}} \times \text{Cpf}$
Internal	Low	Hi/Open	2.7 sec	170 ms	85 ms
	Hi/Open	Hi/Open	2.7 sec	2.7 sec	85 ms

Note that the OSCIN and OSCSEL pins are tri-stated when V_{CC} is below V_{BAT}.

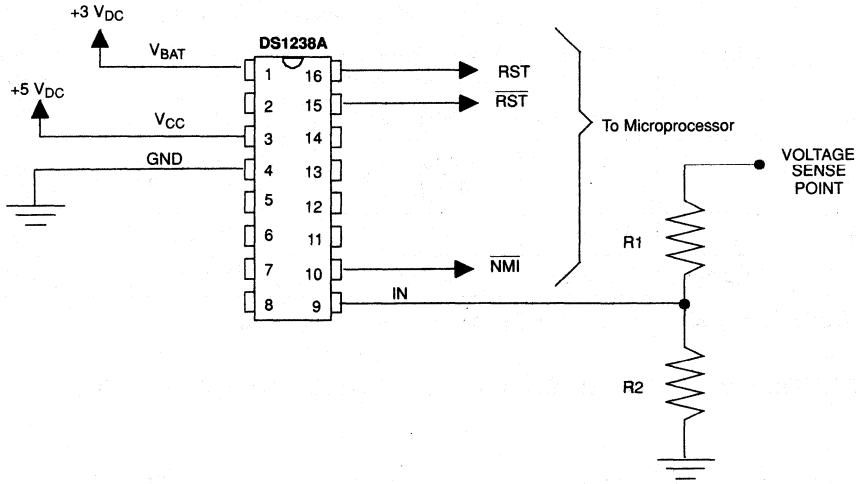
POWER MONITOR, WATCHDOG TIMER, AND PUSHBUTTON RESET Figure 3



PUSHBUTTON RESET TIMING Figure 4



NON-MASKABLE INTERRUPT Figure 5



$$V_{SENSE} = \frac{R1 + R2}{R2} \times 1.27$$

$$MAXVOLTAGE = \frac{V_{SENSE}}{1.27} \times 5.0 = VMAX$$

Example 1: 5 Volt Supply, R2 = 10K Ohms,
V_{SENSE} = 4.8 Volts

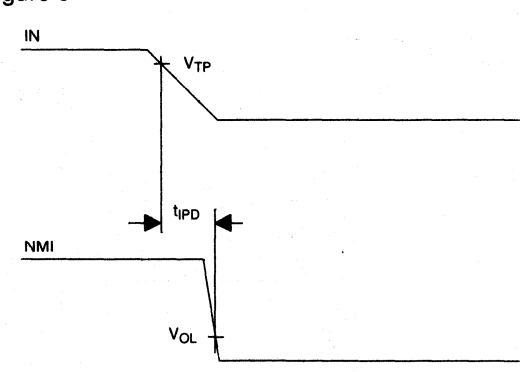
$$4.8 = \frac{R1 + 10K}{10K} \times 1.27 \geq R1$$
$$= 27.8K \text{ Ohm}$$

Example 2: 12 Volt Supply, R2 = 10K Ohms,
V_{SENSE} = 9.0 Volts

$$9.0 = \frac{R1 + 10K}{10K} \times 1.27 \geq R1 = 60.9K \text{ Ohm}$$

$$V_{MAX} = \frac{9.00}{1.27} \times 5.0 = 35.4 \text{ Volts}$$

$\overline{\text{NMI}}$ FROM IN INPUT Figure 6



MEMORY BACKUP

The DS1238A provides all of the necessary functions required to battery back a static RAM. First, an internal switch is provided to supply SRAM power from the primary 5-volt supply (V_{CC}) or from an external battery (V_{BAT}), whichever is greater. Second, the same power fail detection described in the power monitor section is used to hold the chip enable output ($\overline{CEO}$) to within 0.3 volts of V_{CC} or to within 0.7 volts of V_{BAT}. The output voltage diode drop from V_{BAT} (0.7V) is necessary to prevent charging of the battery in violation of UL standards. Write protection occurs as V_{CC} falls below V_{CCTP} as specified. If $\overline{CEI}$ is low at the time power fail detection occurs, $\overline{CEO}$ is held in its present state until $\overline{CEI}$ is returned high, or the period t_{CE} expires. This delay of write protection until the current memory cycle is completed prevents the corruption of data. If $\overline{CEO}$ is in an inactive state at the time of V_{CC} fail detection, $\overline{CEO}$ will be unconditionally disabled within t_{CF}. During nominal supply conditions $\overline{CEO}$ will follow $\overline{CEI}$ with a maximum propagation delay of 20 ns. Figure 7 shows a typical nonvolatile SRAM application.

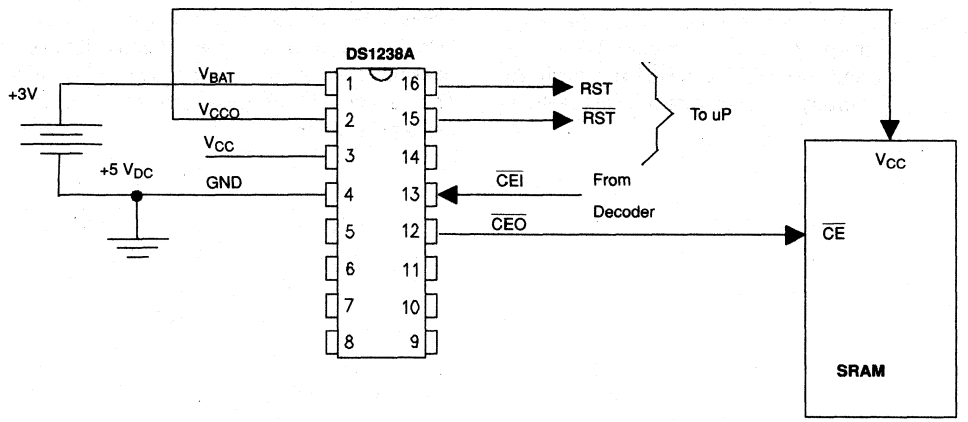
FRESHNESS SEAL

In order to conserve battery capacity during initial construction of an end system, the DS1238A provides a freshness seal that electrically disconnects the battery. This means that upon battery attach, the V_{CCO} output will remain inactive until V_{CC} is applied. This prevents V_{CCO} from powering other devices when the battery is first attached, and V_{CC} is not present. Once V_{CC} is applied, the freshness seal is broken and cannot be invoked again without subsequent removal and re–attachment of the battery.

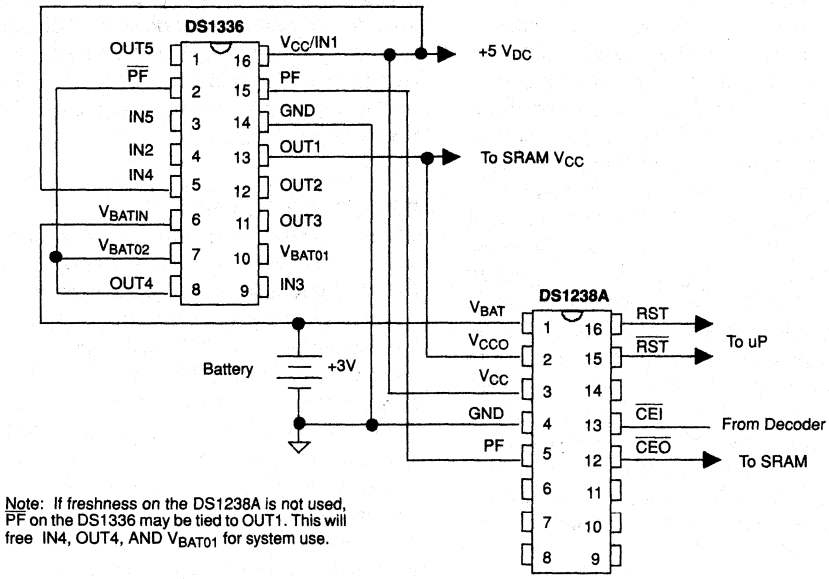
POWER SWITCHING

When larger operating currents are required in a battery-backed system, the internal switching devices of the DS1238A may be too small to support the required load through V_{CCO} with a reasonable voltage drop. For these applications, the PF output is provided to gate external power switching devices. As shown in Figure 8, power to the load is switched from V_{CC} to battery on power down, and from battery to V_{CC} on power up. The DS1336 is designed to use the PF output to switch between V_{BAT} and V_{CC}. It provides better leakage and switchover performance than currently available discrete components. The transition threshold for PF is set to the external battery voltage V_{BAT}, allowing a smooth transition between sources. Any load applied to the PF pin by an external switch will be supplied by the battery. Therefore, if a discrete switch is used, this load should be taken into consideration when sizing the battery.

NONVOLATILE SRAM Figure 7



POWER SWITCHING Figure 8



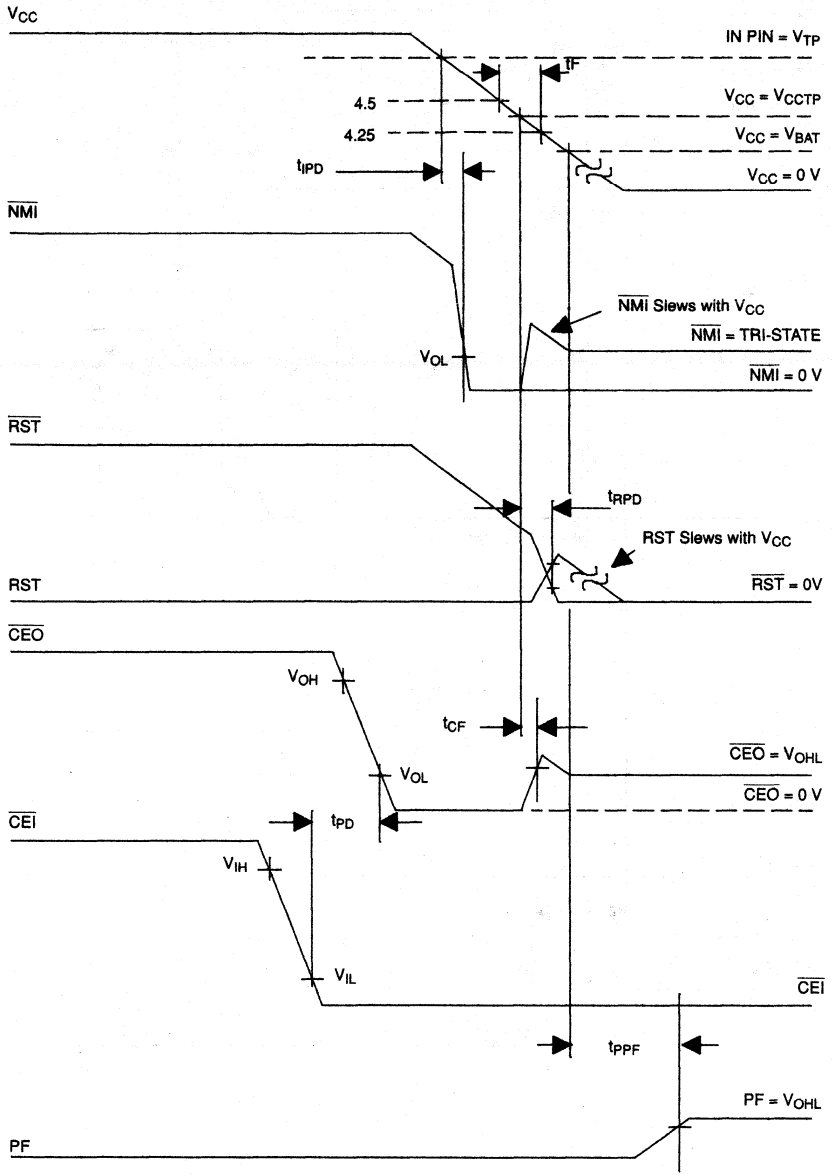
Note: If freshness on the DS1238A is not used, PF on the DS1336 may be tied to OUT1. This will free IN4, OUT4, AND V_{BAT01} for system use.

TIMING DIAGRAMS

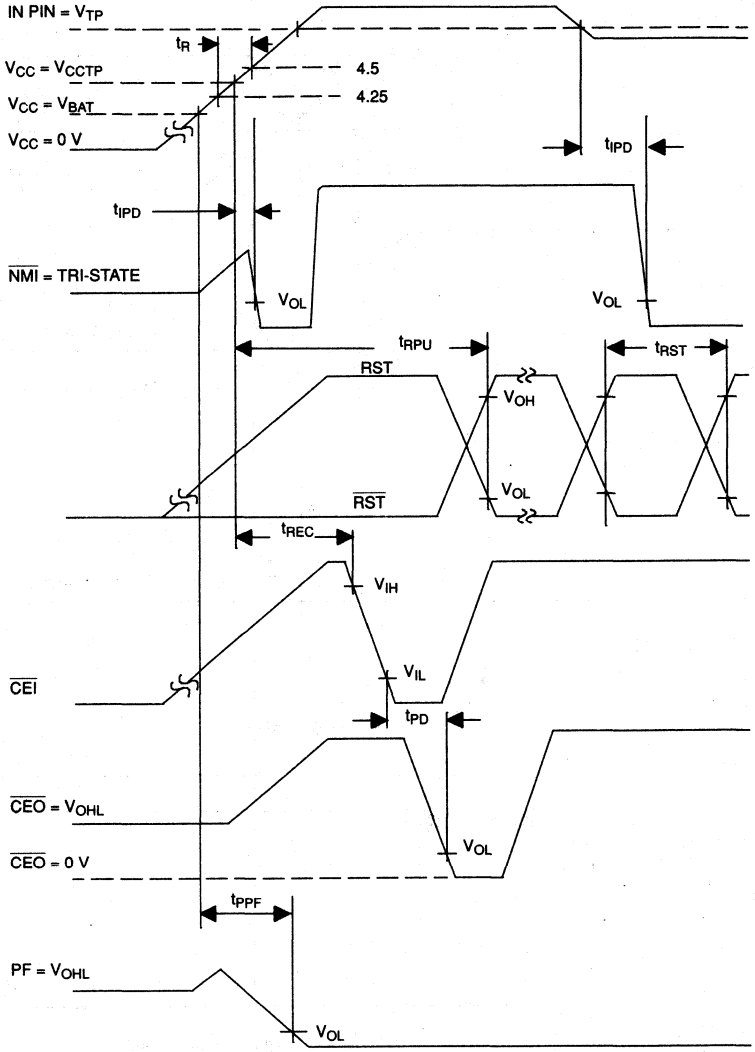
This section provides a description of the timing diagrams shown in Figure 9 and Figure 10. Figure 9 illustrates the relationship for power down. As V_{CC} falls, the IN pin voltage drops below V_{TP}. As a result, the processor is notified of an impending power failure via an active $\overline{NMI}$. This gives the processor time to save critical data in nonvolatile SRAM. As the power falls further, V_{CC} crosses V_{CCTP}, the power monitor trip point. When V_{CC} reaches V_{CCTP}, and active RST and $\overline{RST}$ are given. At this time, $\overline{CEO}$ is brought high to write protect the RAM. When the V_{CC} reaches V_{BAT}, a power fail is issued via the PF pin.

Figure 10 shows the power up sequence. As V_{CC} slews above V_{BAT}, the PF pin is deactivated. An active reset occurs as well as an $\overline{NMI}$. Although the $\overline{NMI}$ may be short due to slew rates, reset will be maintained for the standard t_{RPU} timeout period. At a later time, if the IN pin falls below V_{TP}, a new $\overline{NMI}$ will occur. If the processor does not issue an $\overline{ST}$, a watchdog reset will also occur. The second $\overline{NMI}$ and RST are provided to illustrate these possibilities.

POWER DOWN TIMING Figure 9



POWER UP TIMING Figure 10



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	–0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	0°C to 70°C
Operating Temperature (Industrial Version)	–40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Supply Voltage (5% Option)	V_{CC}	4.75	5.0	5.5	V	1
Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	1
Input Low Level	V_{IL}	-0.3		+0.8	V	1
IN Input Pin	V_{IN}	0		V_{CC}	V	1
Battery Input	V_{BAT}	0		4.0	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}			4	mA	2
Battery Current	I_{BAT}	0		200	nA	2, 12
Supply Output Current (V_{CCO} = V_{CC} - 0.3V)	I_{CC01}			100	mA	3
Supply Out Current (V_{CC} < V_{BAT})	I_{CC02}			1	mA	4
Supply Output Voltage	V_{CCO}	V_{CC} -0.3			V	1
Battery Back Voltage	V_{CCO}		V_{BAT} -0.8		V	6
Low Level @ RST	V_{OL}			0.4	V	1
Output Voltage @ –500 µA	V_{OH}	V_{CC}–0.5V	V_{CC}–0.1V		V	1
$\overline{CEO}$ and PF Output	V_{OHL}		V_{BAT} -0.8		V	6
Input Leakage Current	I_{LI}	-1.0		+1.0	µA	2
Output Leakage	I_{LO}	-1.0		+1.0	µA	11
Output Current @0.4V	I_{OL}			4.0	mA	9
Output Current @2.4V	I_{OH}	-1.0			mA	10
Power Sup. Trip Point	V_{CCTP}	4.25	4.37	4.50	V	1
Power Supply Trip (5% Option)	V_{CCTP}	4.50	4.62	4.75	V	
IN Input Pin Current	I_{CCIN}	-1.0		+1.0	µA	
IN Input Trip Point	V_{TP}	1.15	1.27	1.35	V	1

AC ELECTRICAL CHARACTERISTIC

(0°C to 70°C; V_{CC} = 5V± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Fall Detect to RST, $\overline{RST}$	t_{RPD}	40	100	175	µs	
V_{TP} to $\overline{NMI}$	t_{IPD}	40	100	175	µs	
RESET Active OSCSEL=high	t_{RST}	40	85	150	ms	
$\overline{ST}$ Pulse Width	t_{ST}	20			ns	13
PBRST @ V_{IL}	t_{PB}	30			ms	
V_{CC} Slew Rate 4.75 to 4.25	t_F	300			µs	
Chip Enable Prop Delay	t_{PD}			20	ns	
V_{CC} Fail to Chip Enable High	t_{CF}	7	12	144	µs	11
V_{CC} Valid to RST (RC = 1)	t_{FPU}			100	ns	
V_{CC} Valid to RST	t_{RPU}	40	100	150	ms	5
V_{CC} Slew to 4.25 to V_{BAT}	t_{FB1}	10			µs	
Chip Enable Output Recovery Time	t_{REC}	.1			µs	7
V_{CC} Slew 4.25 to 4.75	t_R	0			µs	
Chip Enable Pulse Width	t_{CE}			5	µs	8
Watchdog Time Delay int clock Long period	t_{TD}	1.7	2.7		s	
Short period		110	170		ms	
Watchdog Time Delay, ext clock, After reset	t_{TD}		20480		clocks	
Normal			5120		clocks	
V_{BAT} Detect to PF	t_{PPF}			2	µs	
OSC IN Frequency	f_{OSC}	0		250	KHz	

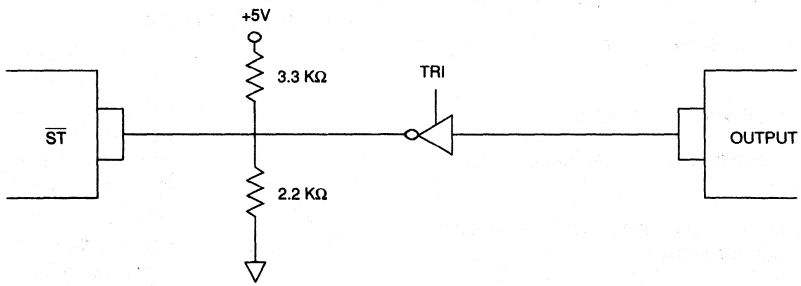
CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

NOTES:

1. All voltages referenced to ground.
2. Measured with V_{CCO}, $\overline{CEO}$, PF, $\overline{ST}$, RST, $\overline{RST}$, and $\overline{NMI}$ pin open.
3. I_{CCO1} is the maximum average load which the DS1238A can supply at V_{CC}-.3V through the V_{CCO} pin during normal 5-volt operation.
4. I_{CCO2} is the maximum average load which the DS1238A can supply through the V_{CCO} pin during data retention battery supply operation, with a maximum drop of 0.8 volts for commercial, 1.0V for industrial.
5. With t_R = 5 µs.
6. V_{CCO} is approximately V_{BAT}-0.5V at 1 µA load.
7. t_{REC} is the minimum time required before $\overline{CEI}/\overline{CEO}$ memory access is allowed.
8. t_{CE} maximum must be met to insure data integrity on power loss.
9. All outputs except RST which is 25 µA max.
10. All outputs except $\overline{RST}$, $\overline{RTV}$, and $\overline{NMI}$ which is 25 µA min.
11. The $\overline{ST}$ pin will sink ±50 µA in normal operation. The OSCIN pin will sink ±5 µA in normal operation. The OSCSEL pin will sink ±10 µA in normal operation.
12. I_{BAT} is measured with V_{BAT}=3.0V.
13. $\overline{ST}$ should be active low before the watchdog is disabled (i.e., before the $\overline{ST}$ input is tristated).



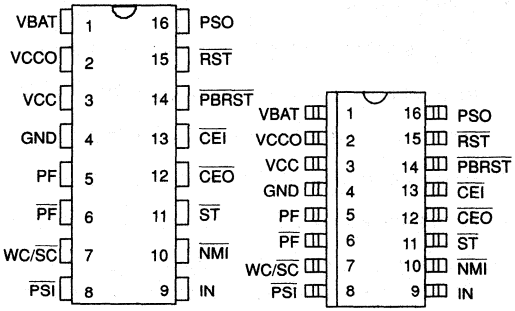
DALLAS SEMICONDUCTOR

DS1239
MicroManager Chip

FEATURES

- Provides necessary control for start up and shutdown of power supply from keyboard
- Holds microprocessor in check during power transients
- Halts and restarts an out-of-control microprocessor
- Monitors push button for external override
- Warns microprocessor of an impending power failure
- Converts CMOS SRAM into nonvolatile memory
- Unconditionally write-protects memory when power supply is out of tolerance
- Consumes less than 100 nA of battery current
- Controls external power switch for high current applications
- Accurate 10% power supply monitoring
- Optional 5% power supply monitoring designated DS1239-5
- Provides orderly shutdown in nonvolatile microprocessor applications
- Supplies necessary control for low-power "stop mode" in battery operate hand-held applications
- Standard 16-pin DIP or space-saving 16-pin SOIC
- Optional industrial temperature range -40°C to +85°C

PIN ASSIGNMENT



DS1239 16-Pin DIP (300 Mil) See Mech Drawing Pg. 480

DS1239 16-Pin SOIC (300 Mil) See Mech. Drawing Pg. 484

PIN DESCRIPTION

V_{BAT}	–	+3 Volt Battery Input
V_{CCO}	–	Switched SRAM Supply Output
V_{CC}	–	+5 Volt Power Supply Input
GND	–	Ground
PF	–	Power Fail (Active High)
$\overline{PF}$	–	Power Fail (Active Low)
WC/$\overline{SC}$	–	Wake-Up Control (Sleep)
$\overline{PSI}$	–	Power Supply Control Input
IN	–	Early Warning Input
$\overline{NMI}$	–	Non-Maskable Interrupt
$\overline{ST}$	–	Strobe Input
$\overline{CEO}$	–	Chip Enable Output
$\overline{CEI}$	–	Chip Enable Input
$\overline{PBRST}$	–	Pushbutton Reset Input
$\overline{RST}$	–	Reset Output (Active low)
PSO	–	Power Supply Control Outputs

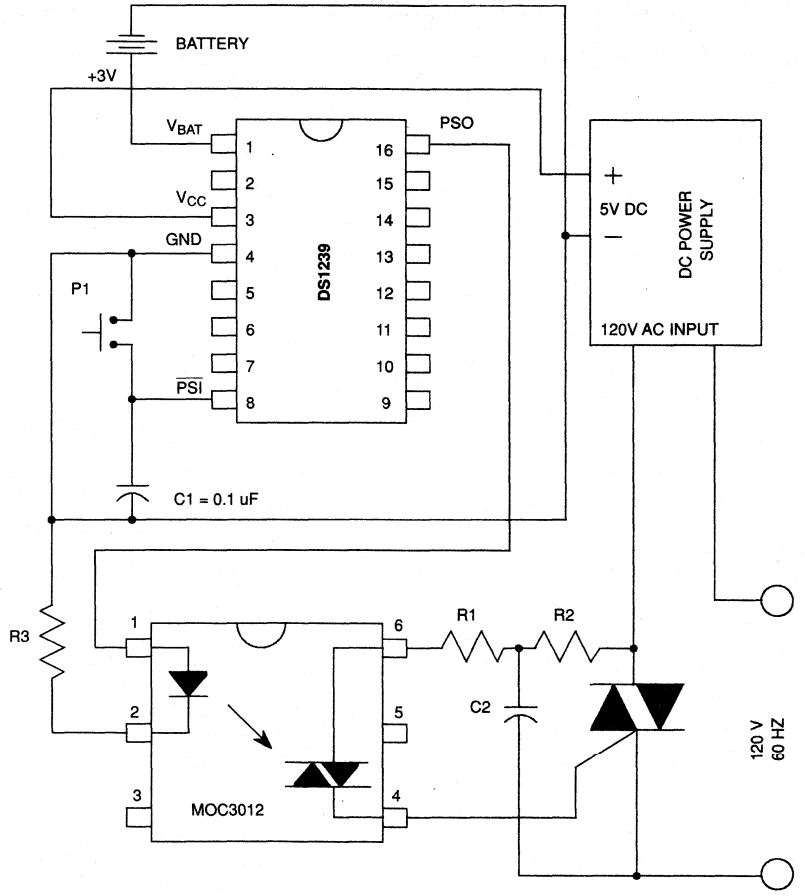
DESCRIPTION

The DS1239 MicroManager provides all the necessary functions for power supply control and monitoring, reset control, and memory backup in microprocessor-based systems. Using the DS1239, an AC power switch is no longer required for microprocessor-based systems. A keyboard control system for power supply start up and shutdown is provided through the use of the Power Supply Control Input and Output. In other respects, the DS1239 is functionally identical to a DS1236 in the NMOS mode. For a complete description of the other DS1239 features, refer to the DS1236 data sheet. Pin-out of the DS1239 is identical to the DS1236 with two exceptions. The RC and RST pins have been replaced with $\overline{PSI}$ and PSO, respectively. Other pins and functions operate exactly as the DS1236 in NMOS mode.

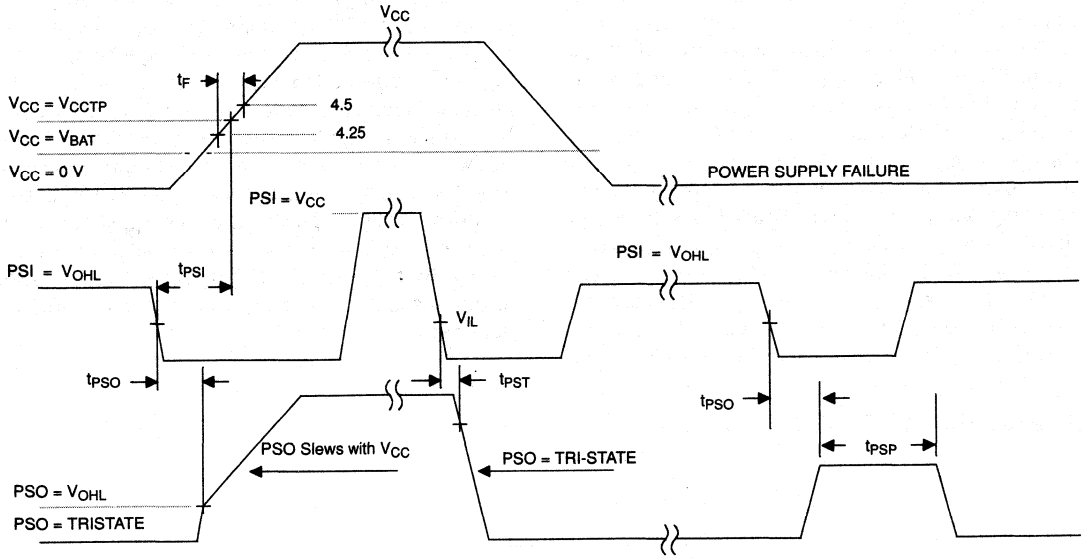
POWER SUPPLY CONTROL

The DS1239 facilitates the power-up and power down sequencing of a main power supply from a keyboard or pushbutton. The Power Supply Control Input ($\overline{PSI}$) and Power Supply Control Output (PSO) are used for this purpose. Prior to establishing a voltage on V_{CC} (+5V), the $\overline{PSI}$ is internally held at a high level at all times with the V_{BAT} supply. When $\overline{PSI}$ is forced low via a key pad or other source, the PSO is connected to the V_{BAT} to provide a high level. As shown in Figure 1, this active high signal can be wired directly to an optically isolated SCR to initiate an AC to DC power-up sequence. This in turn will provide the supply voltage for V_{CC}. The timing is illustrated in Figure 2. Holding the $\overline{PSI}$ input low, the PSO output will supply a connection to the V_{BAT} pin until the V_{CC} reaches V_{BAT}, or a maximum of 500 ms. If the supply voltage on V_{CC} rises above the V_{BAT} level before the t_{PSI} time-out, the PSO pin will remain high and track the V_{CC} input. If V_{CC} does not rise above V_{BAT} before either t_{PSI} or $\overline{PSI}$ is allowed to return to a high level, the PSO output will return to tristate. Once the PSO output and V_{CC} are set at a high level, a subsequent falling edge on $\overline{PSI}$ will tristate PSO to initiate a shut down condition. The 10 microamp current supplied by the $\overline{PSI}$ pin allows the use of a 0.1 µF capacitor as a simple pushbutton debounce circuit. The battery size for this application must be selected to provide the SCR on-current for the power supply response time and is consequently application-specific.

POWER SUPPLY CONTROL Figure 1



POWER SUPPLY CONTROL TIMING Figure 2



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	–0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	0°C to 70°C
Operating Temperature (Industrial Version)	–40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

These specifications reflect the power supply control feature of the DS1239. For complete electrical specifications, refer to the DS1236 data sheet.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{PSI}$ Output Current	I_{PSI}		3		µA	
PSO Output Current	I_{PSO}	10			mA	3

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{PSI}$ to Valid V_{CC}	t_{PSI}			200	ms	1
$\overline{PSI}$ to PSO Tri-state	t_{PST}			20	ns	
$\overline{PSI}$ to Valid PSO	t_{PSO}			100	ns	
PSO Pulse Width	t_{PSP}		200	500	ms	2

NOTES:

1. Minimum turn-on response time for AC-to-DC power supply.
2. PSO pulse width for V_{CC} held below V_{BAT}.
3. PSO will typically source 1.5 mA at 1.5V with V_{CC} = 0V, V_{BAT} = 3V.

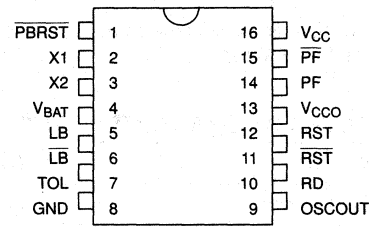
DALLAS SEMICONDUCTOR

DS1632
PC Power Fail and Reset Controller

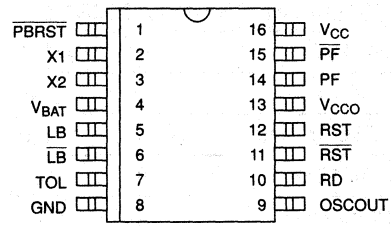
FEATURES

- Power fail detector for personal computers and workstations
- Connects directly to popular personal computer chip sets
- On chip 32.768 KHz oscillator for real time clock
- Provides battery backup power to clock chip
- Pushbutton reset input
- Accurate 5% or 10% +5 volt power supply monitoring
- Complementary outputs for reset, power fail, and low battery
- Provides for reset pulse width of either 95 ms or 190 ms
- Eliminates the need for discrete components
- Low–power CMOS circuitry
- 16-pin DIP or SOIC surface mount package
- 0°C to 70°C operation

PIN ASSIGNMENT



16-Pin DIP (300 Mil)
See Mech. Drawing – Pg. 480



16-Pin SOIC (300 Mil)
See Mech. Drawing – Pg. 484

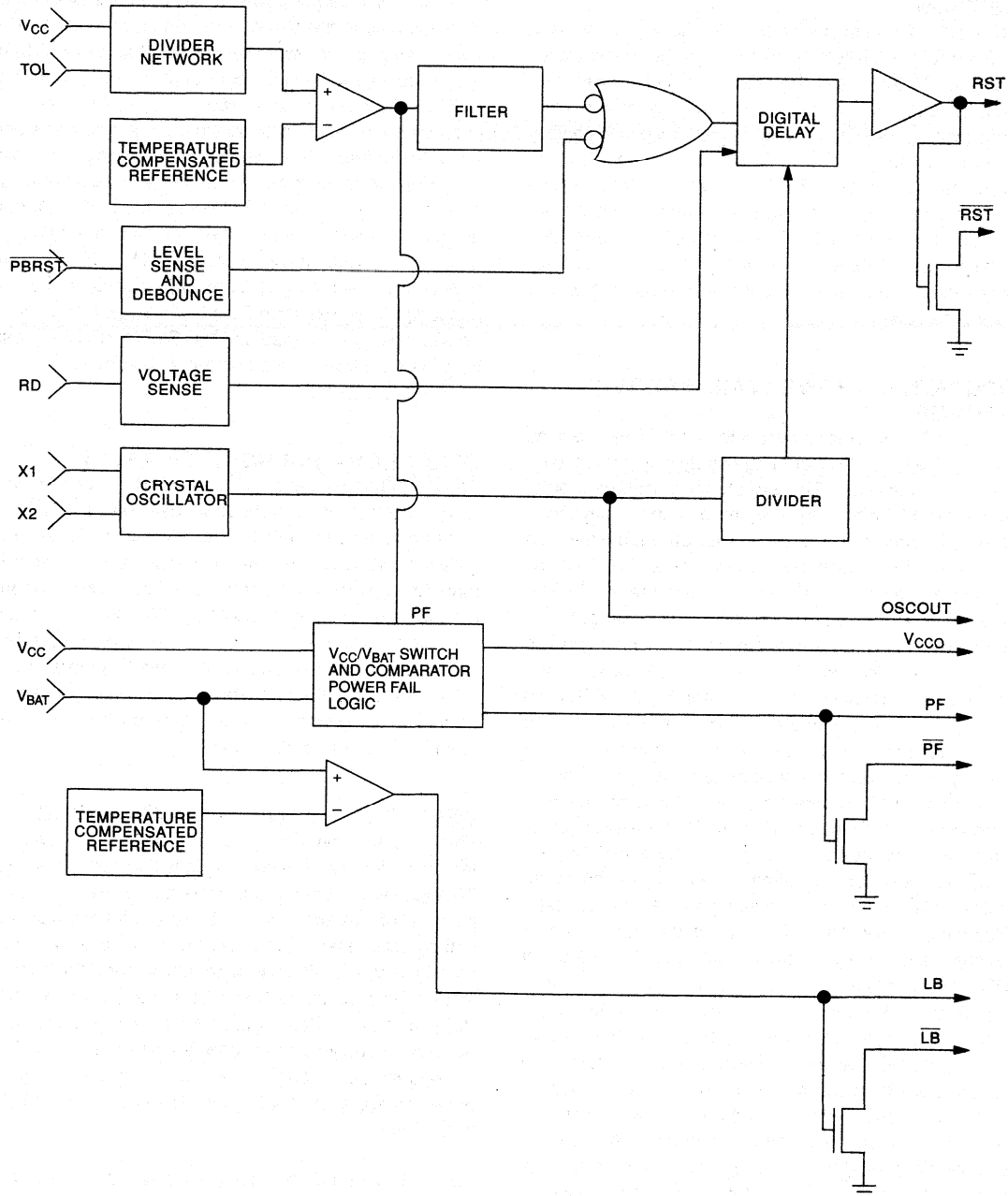
PIN DESCRIPTION

PBRST	-	Pushbutton Reset Input
X1, X2	-	Crystal Inputs
V_{BAT}	-	Battery Input
LB, LB	-	Low Battery Outputs
RST, RST	-	Reset Outputs
RD	-	Reset Duration
TOL	-	Selects 5% Or 10% Detection
GND	-	Ground
OSCOUT	-	Oscillator Out
V_{CCO}	-	Switched Power Out
PF, PF	-	Power Fail Outputs
V_{CC}	-	+5 Volt Power In

DESCRIPTION

The DS1632 PC Power Fail and Reset Controller is designed to do various functions involving battery backup and other functions typically accomplished with discrete components. The DS1632 provides a 32.768 KHz battery backed up crystal oscillator and switched V_{CC}/V_{BAT} power via V_{CCO} for the real–time clock function located in accompanying chip sets. In addition, the DS1632 provides for reset on both power up and via pushbutton input, power fail status signals for the processor, and low battery warning signals. The DS1632 is capable of detecting power failure at both the 5% and 10% power supply tolerances, and the reset pulse width can be set for either 95 ms or 190 ms. The device is designed to connect directly to popular laptop and notebook chip sets which eliminates the need for discrete components and reduces cost.

BLOCK DIAGRAM Figure 1



OPERATION – CRYSTAL OSCILLATOR SECTION

The DS1632 crystal oscillator is designed to be hooked directly to a 32.768 KHz crystal. By using the Daiwa Part No. DT26S, Seiko Part No. DS-VT-200 or equivalent, the oscillator will be accurate enough to run a real time clock to within ±2 minutes per month. If another crystal is to be selected, it should have a specified load capacitance (C_L) of 6 pF. The crystal oscillator will run as long as either V_{CC} or V_{BAT} is present, providing that V_{BAT} is greater than 2.3V. The oscillator output provides a rail to rail swing with regards to V_{CC} or V_{BAT}, whichever is greater. The crystal oscillator is also used internally as a time base.

OPERATION – POWER FAIL, BATTERY BACKUP

The DS1632 provides a switch to direct power from the battery (V_{BAT}) or the incoming supply (V_{CC}) depending on which is greater. This switch has a voltage drop of less than 0.2 volts. The V_{CC} input is constantly monitored by a precision comparator for an out of tolerance condition. When such a condition occurs, the power fail signals are driven to their active state immediately. The reset signals are also driven active, but this action is delayed by a time determined by the level of the input on the reset duration pin (RD). If RD is tied to ground then reset signals will become active after 9 ms. If RD is tied to V_{CC}, then reset signals will become active after 18 ms. Once active, both the reset signals and the power fail signals will remain active as long as a (V_{CC}) out of tolerance condition persists. If an out of tolerance condition is not long enough to activate the reset signals, then only the power fail signals would be affected. When power returns to within nominal limits the power fail signals will return immediately to the inactive state. However, the reset signals remain in the active state for a time which is dependent on the state of the RD pin. If RD is tied to ground, the reset signals will remain active for 95 ms. If RD is tied to V_{CC}, then the reset signals will remain active for 190 ms after power is within nominal limits. The delay action on the reset signals allows time for the power supply and microprocessor clock oscillators to stabilize. The tolerance pin (TOL) selects the point at which power fail detection occurs. With the tolerance pin grounded, power fail detection occurs in the range of 4.75V to 4.5V. If the tolerance pin is connected to V_{CC}, then power fail detection occurs in the range of 4.5V to 4.25V. During most power supply conditions the V_{CC} input will supply power to all functions within the chip and also to the V_{CCO} pin. The battery pin (V_{BAT}) only supplies power when V_{CC} is less than V_{BAT}. When V_{CC} is below the level of V_{BAT} only the V_{CCO} and the OSC OUT pin remain powered by V_{BAT}. All other outputs will be driven to ground when in a logic low state and will be driven to V_{CC} when in a logic high state. This is done to preserve battery capacity by avoiding battery drain resulting from loads on these outputs. The output ground level will be maintained for all levels of V_{CC}, even V_{CC} = GND. However, the output V_{CC} level will be maintained only for V_{CC} > 2.0V. Internal battery power consumption is less than 2 µA while V_{BAT} is supplying power. The external load on OSC OUT and V_{CCO} must be added to internal consumption to determine the total load on the battery.

OPERATION – PUSHBUTTON RESET

The DS1632 provides an input pin for direct connection to a pushbutton. The pushbutton reset input $\overline{PBRST}$ requires an active low level input. While TTL levels are sufficient to properly activate this input, it has been primarily designed for contact closure. Internally, this input is debounced and timed such that RST and $\overline{RST}$ signals of 95ms or 190 ms minimum are generated. If RD is tied to ground, then a reset pulse of 95 ms is generated. If RD is tied to V_{CC} then a reset pulse of 190 ms is generated. The delay time is started as the pushbutton reset input is released from low level.

OPERATION – LOW BATTERY WARNING

The DS1632 provides outputs which warn of a low battery condition. Whenever V_{CC} is within nominal limits, the V_{BAT} input is continuously monitored. If the V_{BAT} input is out of tolerance, the low battery outputs are driven to their active states, and will remain in the active state as long as V_{CC} is within nominal limits or until the battery input is restored to an in limit status. On power up, if the V_{BAT} input is out of tolerance, the low battery outputs are not guaranteed active until power fail is deactivated, but guaranteed active prior to reset inactive. When V_{CC} is below the V_{CC} fail trip point both LB and $\overline{LB}$ will be driven to ground.

For application information, please reference Application Note #64, published separately.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	-0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
$\overline{PBRST}$ Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	1, 3
$\overline{PBRST}$ Input Low Level	V_{IL}	-0.3		+0.8	V	1, 3
Battery Supply Voltage	V_{BAT}	2.3	3.0	3.5	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Current @ 2.4V	I_{OH}	1			mA	5, 7
Output Current @ 0.4V	I_{OL}	4			mA	7
Output Voltage @ -500 µA	V_{OH}	V_{CC}-0.5V	V_{CC}-0.1V		V	1, 6
Low Level @ RST	V_{OL}			0.4	V	1
Operating Current	I_{CC}		0.5	2.0	mA	2
V_{CC} Trip Point (TOL=GND)	V_{CCTP}	4.50	4.62	4.75	V	1
V_{CC} Trip Point (TOL=V_{CC})	V_{CCTP}	4.25	4.37	4.50	V	1
Battery Fail Trip Point	V_{BATTP}	2.30	2.45	2.55	V	1
Supply Voltage Output	V_{CCO}	V_{CC}-0.2			V	
Supply Current Output	I_{CCO1}			100	mA	4

DC ELECTRICAL CHARACTERISTICS

(0°C; V_{CC} = < V_{BAT})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Battery Current	I_{BAT}			2	µA	
Battery Backup Current	I_{CCO2}			500	µA	4

CAPACITANCE

(t_A = 25°C)

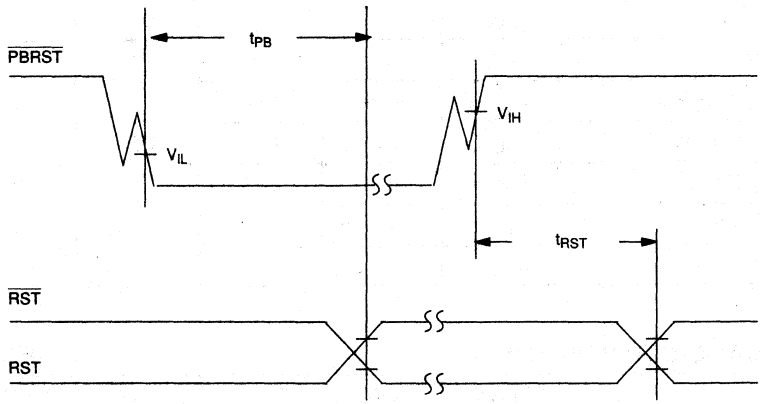
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

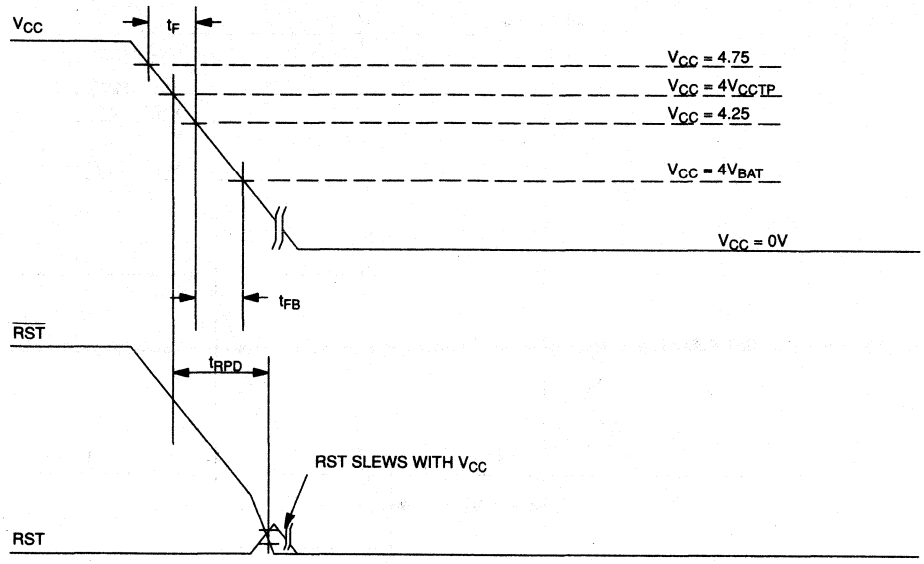
(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{PBRST}$ = V_{IL}	t_{PB}	t_{RPD}			ms	
Reset Pulse Width	t_{RST}	95		105	ms	RD=GND
Reset Pulse Width	t_{RST}	190		210	ms	RD=V_{CC}
Reset Active on Power Up	t_{RPU}	95		105	ms	RD=GND
Reset Active on Power Up	t_{RPU}	190		210	ms	RD=V_{CC}
Reset Active on Power Down	t_{RPD}	9		11	ms	RD=GND
Reset Active on Power Down	t_{RPD}	18		22	ms	RD=V_{CC}
V_{CC} Slew Rate Power Down	t_F	300			µs	
V_{CC} Slew Rate Power Down	t_{FB}	10			µs	
V_{CC} Slew Rate Power Up	t_R	10			µs	

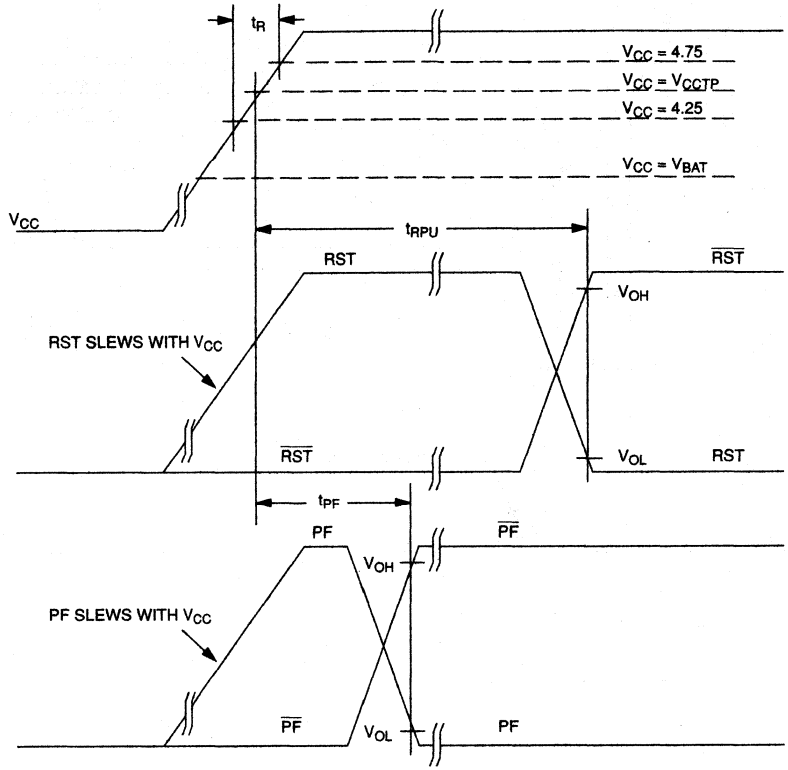
TIMING DIAGRAM: PUSHBUTTON RESET



TIMING DIAGRAM: POWER DOWN



TIMING DIAGRAM: POWER UP



NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. The $\overline{PBRST}$ input has an internal pull up of 10KΩ to V_{CC}.
4. Supply current output is specified with 0.2V drop from V_{BAT} or V_{CC}.
5. $\overline{RST}$, $\overline{PF}$, and $\overline{LB}$ are open drain outputs.
6. RST and PF remain within 0.5 volts of V_{CC} on power down until V_{CC} drops below 2.0V.
7. Sink and source currents apply to all outputs except OSC OUT which has a drive capability of sourcing 500 µA at $V_{OH} = V_{CCO}$ - 0.5V and sinking 1 mA at V_{OL} = 0.5 V.

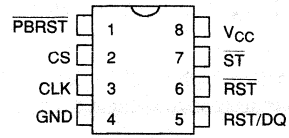
DALLAS SEMICONDUCTOR

DS1830
Programmable MicroMonitor

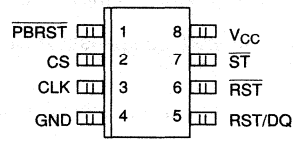
FEATURES

- Halts and restarts an out–of–control microprocessor
- Holds microprocessor in check during power transients
- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Major function parameters programmable through simple 3–wire interface, stored in nonvolatile memory
- Reset time programmable from 5 ms to 2.5 seconds
- Watchdog timeout programmable from 25 ms to 12.5 seconds
- Power trip points programmable 4.75V to 2.7V
- Pin compatible with the DS1232
- Low cost 8–pin DIP and 8–pin SOIC packages available
- Operating temperature of –40°C to +85°C

PIN ASSIGNMENT



DS1830 8–PIN DIP
(300 MIL)
See Mech. Drawing
Pg. 480



DS1830 8–PIN SOIC
(150 MIL)
See Mech. Drawing
Pg. 483

PIN DESCRIPTION

$\overline{\text{PBRST}}$	–	Pushbutton Reset Input
CS	–	Chip Select for Serial Port
CLK	–	Clock for Serial Port
GND	–	Ground
RST/DQ	–	Active High Reset Output/Serial Data Input
$\overline{\text{RST}}$	–	Active Low Reset Output
$\overline{\text{ST}}$	–	Strobe Input
V_{CC}	–	Power Supply

DESCRIPTION

The DS1830 Programmable MicroMonitor monitors three vital conditions for a microprocessor: power supply, software execution, and external override. All monitored parameters are programmable, with values stored in nonvolatile EPROM. This allows parameters such as reset time, watchdog timeout period, and power supply tolerance to be programmed into the device and tailored to the application circuit and microprocessor which is to be monitored.

In addition, the watchdog timer, reset, and pushbutton functions may be disabled via software. This allows maximum flexibility for use in new product development and system application testing.

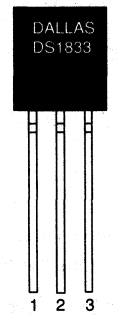
DALLAS SEMICONDUCTOR

DS1833
5V EconoReset

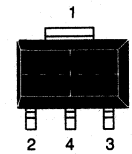
FEATURES

- Automatically restarts microprocessor after power failure
- Maintains active–high reset for 350 ms after V_{CC} returns to an in-tolerance condition
- Accurate 5%, 10% or 15% microprocessor 5V power supply monitoring
- Reduces need for discrete components
- Precision temperature-compensated voltage reference and voltage sensor
- Low-cost TO-92 package or surface mount SOT-223 package
- Internal 5K pull-up resistor
- Operating temperature of –40°C to +85°C

PIN ASSIGNMENT



TO-92 Package
See Mech Drawing
Pg. 486



SOT-223 Package
See Mech Drawing
Pg. 490

PIN DESCRIPTION

PIN 1	GROUND
PIN 2	RESET
PIN 3	V_{CC}
PIN 4	GROUND (SOT–223 ONLY)

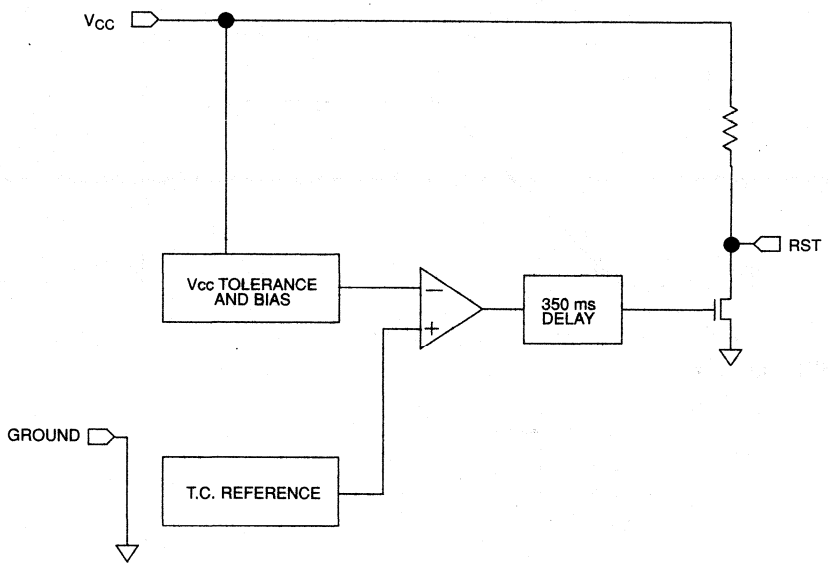
DESCRIPTION

The DS1833 EconoReset uses a precision temperature compensated reference and comparator circuit to monitor the status of the power supply (V_{CC}). When an out-of-tolerance condition is detected, an internal power fail signal is generated which forces reset to the active (high) state. When V_{CC} returns to an in-tolerance condition, the reset signal is kept in the active state for approximately 350 ms to allow the power supply and processor to stabilize.

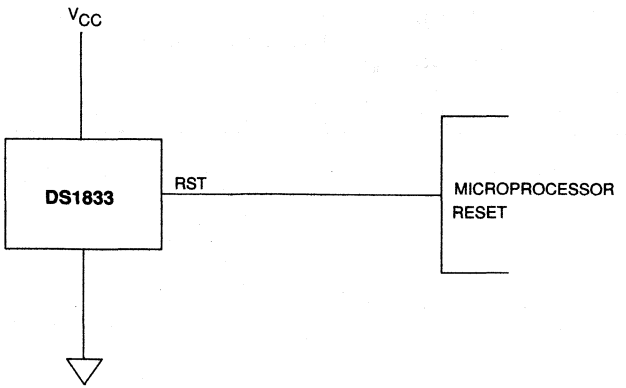
OPERATION - POWER MONITOR

The DS1833 provides the functions of detecting out-of-tolerance power supply conditions and warning a processor-based system of impending power failure. When V_{CC} is detected as out-of-tolerance, as defined by the tolerance of the part selected, the RST signal is asserted. On power-up, RST is kept active for approximately 350 ms after the power supply has reached the selected tolerance. This allows the power supply and microprocessor to stabilize before RST is released.

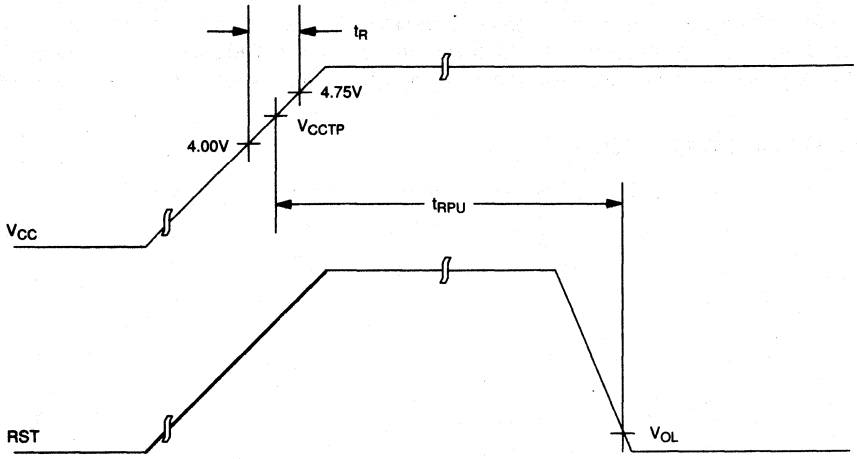
BLOCK DIAGRAM Figure 1



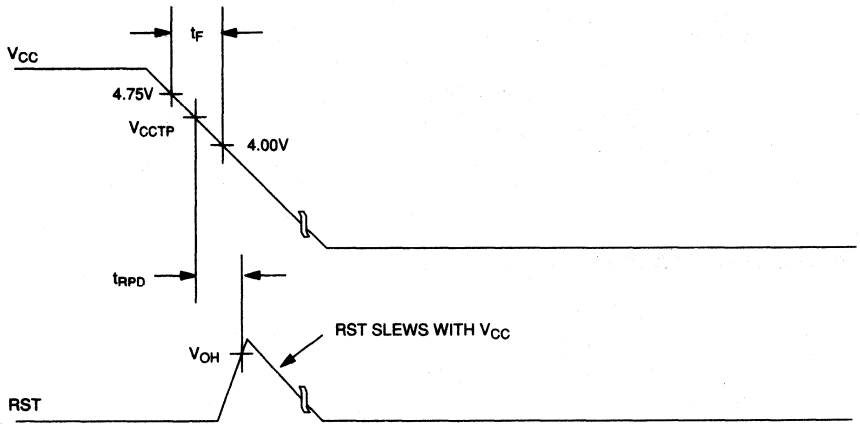
APPLICATION EXAMPLE Figure 2



POWER UP Figure 3



POWER DOWN Figure 4



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	-0.5V to +7.0V
Voltage on I/O Relative to Ground	–0.5V to V_{CC} + 0.5V
Operating Temperature	–40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	1.2	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Low Level @ RST	V_{OL}			0.4	V	1
Output Voltage @ –500 µA	V_{OH}	V_{CC}–0.5V	V_{CC}–0.1V		V	1
Output Current @ 2.4V	I_{OH}		350		µA	
Output Current @ 0.4V	I_{OL}	+10			mA	
Operating Current	I_{CC}		1.5	2	mA	
V_{CC} Trip Point 5%	V_{CCTP1}	4.5	4.625	4.74	V	1
V_{CC} Trip Point 10%	V_{CCTP2}	4.25	4.375	4.49	V	1
V_{CC} Trip Point 15%	V_{CCTP3}	4.0	4.125	4.24	V	1
Output Capacitance	C_{OUT}			10	pF	
Internal Pull-Up Resistor	R_P	3.75	5	6.25	KΩ	

AC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Active Time	t_{RST}	250	350	450	ms	
V_{CC} Detect to RST	t_{RPD}			100	ns	
V_{CC} Slew Rate (4.75V - 4.00V)	t_F	300			µs	
V_{CC} Slew Rate (4.00V - 4.75V)	t_R	0			ns	
V_{CC} detect to RST	t_{RPU}	250	350	450	ms	

NOTE:

1. All voltages are referenced to ground.

ECONORESET SELECTION GUIDE

		VCC TRIP POINT			PUSHBUTTON DETECT		
		MIN	TYP	MAX	MIN	TYP	MAX
5V	DS1233-15	4.0	4.125	4.24	2.4	–	3.3
	DS1233-10	4.25	4.375	4.49	2.4	–	3.3
	DS1233-5	4.5	4.625	4.75	2.4	–	3.3
	DS1233D–15	4.0	4.125	4.24	N/A		N/A
	DS1233D–10	4.25	4.375	4.49	N/A		N/A
	DS1233D–5	4.5	4.625	4.75	N/A		N/A
	DS1833–15	4.0	4.125	4.24	N/A		N/A
	DS1833–10	4.25	4.375	4.49	N/A		N/A
	DS1833–5	4.5	4.625	4.75	N/A		N/A
3.3V	DS1233A-15	2.64	2.72	2.80	1.8	–	3.0
	DS1233A-10	2.8	2.88	2.97	1.8	–	3.0

DIGITAL POTENTIOMETERS

DALLAS SEMICONDUCTOR

DS1267
Dual Digital Potentiometer Chip

FEATURES

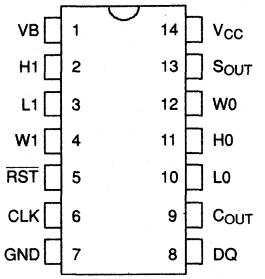
- Ultra–lowpower consumption, quiet, pumpless design
- Two digitally controlled, 256–position potentiometers
- Serial port provides means for setting and reading both potentiometers
- Resistors can be connected in series to provide increased total resistance
- 14–pin DIP, 16–pin SOIC, 20–pin TSSOP packages
- Resistive elements are temperature compensated to ±0.3 LSB relative linearity
- Standard resistance values:
  - DS1267–10 ~ 10KΩ
  - DS1267–50 ~ 50KΩ
  - DS1267–100 ~ 100KΩ
- Temperature:
  - Commercial: 0°C to 70°C
  - Industrial: –40°C to 85°C

DESCRIPTION

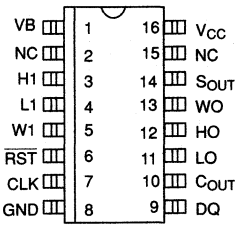
The DS1267 consist of two digitally controlled solid–state potentiometers. Each potentiometer is composed of 256 resistive sections. Between each resistive section and both ends of the potentiometer are tap points which are accessible to the wiper. The position of the wiper on the resistive array is set by an 8–bit value that controls which tap point is connected to the wiper output. Communication and control of the device is accomplished via a 3–wire serial port interface. This interface allows the device wiper position to be read or written.

Both potentiometers can be connected in series (or stacked) for an increased total resistance with the same resolution. For multiple device–single processor environments, the DS1267 can be cascaded or daisy chained. This feature provides for control of multiple devices over a single 3–wire bus.

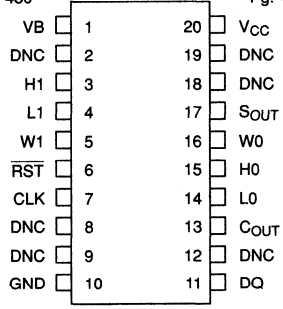
PIN ASSIGNMENT



14–Pin DIP (300 Mil)
See Mech. Drawing
Pg. 480



16–Pin SOIC (300 Mil)
See Mech. Drawing
Pg. 484



20–Pin TSSOP (173 Mil)

PIN DESCRIPTION

L0, L1	–	Low End of Resistor
H0, H1	–	High End of Resistor
W0, W1	–	Wiper Terminal of Resistor
V_B	–	Substrate Bias Voltage
S_{OUT}	–	Stacked Configuration Output
$\overline{RST}$	–	Serial Port Reset Input
DQ	–	Serial Port Data Input
CLK	–	Serial Port Clock Input
C_{OUT}	–	Cascade Port Output
V_{CC}	–	+5 Volt Supply
GND	–	Ground
NC	–	No Internal Connection
DNC	–	Do Not Connect

The DS1267 is offered in three standard resistance values which include 10K, 50K, and 100K ohm versions. Commercial and industrial temperature parts are also available. Available packages for the device include a 14–pin DIP, 16–pin SOIC, and 20–pin TSSOP.

OPERATION

The DS1267 contains two 256–position potentiometers whose wiper positions are set by an 8–bit value. These two 8–bit values are written to a 17–bit I/O shift register which is used to store the two wiper positions and the stack select bit when the device is powered. A block diagram of the DS1267 is presented in Figure 1.

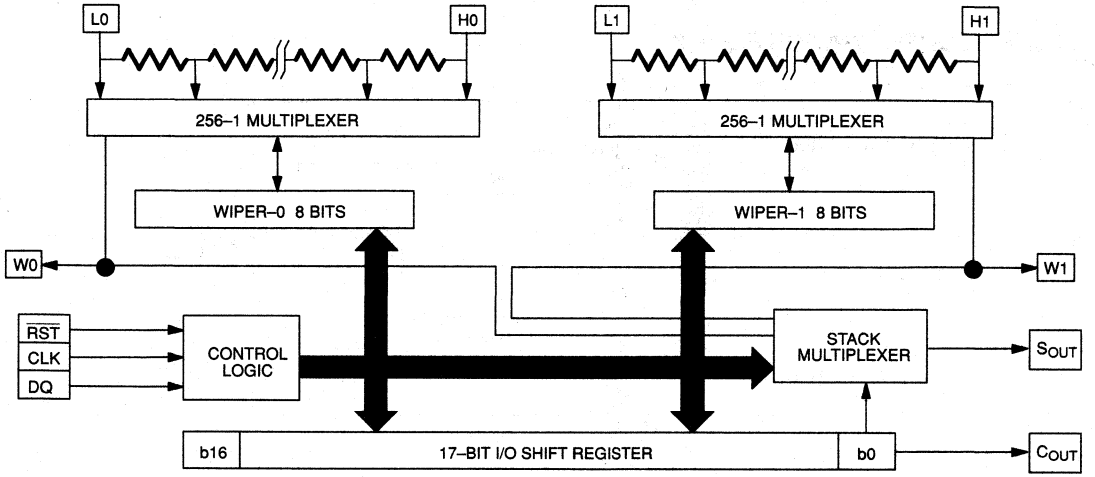
Communication and control of the DS1267 is accomplished through a 3–wire serial port interface that drives an internal control logic unit. The 3–wire serial interface consists of the three input signals: $\overline{RST}$, CLK, and DQ.

The $\overline{RST}$ control signal is used to enable the 3–wire serial port operation of the device. The $\overline{RST}$ signal is an active high input and is required to begin any communication to the DS1267. The CLK signal input is used to provide timing synchronization for data input and output. The DQ signal line is used to transmit potentiometer wiper settings and the stack select bit configuration to the 17–bit I/O shift register of the DS1267.

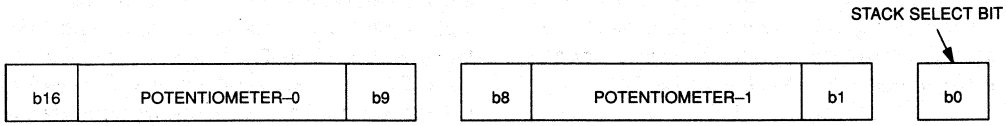
Figure 9(a) presents the 3–wire serial port protocol. As shown, the 3–wire port is inactive when the $\overline{RST}$ signal input is low. Communication with the DS1267 requires the transistion of the $\overline{RST}$ input from a low state to a high state. Once the 3–wire port has been activated, data is entered into the part on the low to high transistion of the CLK signal inputs. Three–wire serial timing requirements are provided in the timing diagrams of Figure 9(b),(c).

Data written to the DS1267 over the 3–wire serial interface is stored in the 17–bit I/O shift register (see Figure 2). The 17–bit I/O shift register contains both 8–bit potentiometer wiper position values and the stack select bit. The composition of the I/O shift register is presented in Figure 2. Bit 0 of the I/O shift register contains the stack select bit. This bit will be discussed in the section entitled Stacked Configuration. Bits 1 through 8 of the I/O shift register contain the potentiometer–1 wiper position value. Bit 1 will contain the MSB of the wiper setting for potentiometer–1 and bit 8 the LSB for the wiper setting. Bits 9 through 16 of the I/O shift register contain the value of the potentiometer–0 wiper position with the MSB for the wiper position occupying bit 9 and the LSB bit 16.

DS1267 BLOCK DIAGRAM Figure 1



I/O SHIFT REGISTER Figure 2



17–BIT I/O SHIFT REGISTER

Transmission of data always begins with the stack select bit followed by the potentiometer–1 wiper position value and lastly the potentiometer–0 wiper position value.

When wiper position data is to be written to the DS1267, 17 bits (or some integer multiple) of data should always be transmitted. Transactions which do not send a complete 17–bits (or multiple) will leave the register incomplete and possibly an error in the desired wiper positions.

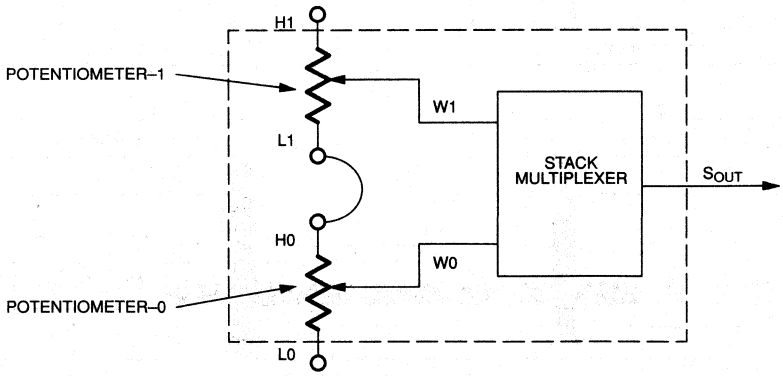
After a communication transaction has been completed the $\overline{RST}$ signal input should be taken to a low state to prevent any inadvertent changes to the device shift register. Once $\overline{RST}$ has reached a low state, the contents of the I/O shift register are loaded into the respective multiplexers for setting wiper position. A new wiper position will only engage after a $\overline{RST}$ transition to the inactive state. On device power–up the DS1267 wiper positions will be set at 50% of the total resistance or binary value 1000 0000.

STACKED CONFIGURATION

The potentiometers of the DS1267 can be connected in series as shown in Figure 3. This is referred to as the stacked configuration and allows the user to double the total end–to–end resistance of the part. The resolution of the combined potentiometers will remain the same as a single potentiometer but with a total of 512 wiper positions available. Device resolution is defined as Rtot/256 (per potentiometer); where Rtot equals the total potentiometer resistance.

The wiper output for the combined stacked potentiometer will be taken at the S_{OUT} pin, which is the multiplexed output of the wiper of potentiometer–0 (W0) or potentiometer–1 (W1). The potentiometer wiper selected at the S_{OUT} output is governed by the setting of the stack select bit (bit 0) of the 17–bit I/O shift register. If the stack select bit has value 0, the multiplexed output, S_{OUT}, will be that of the potentiometer–0 wiper. If the stack select bit has value 1, the multiplexed output, S_{OUT}, will be that of the potentiometer–1 wiper.

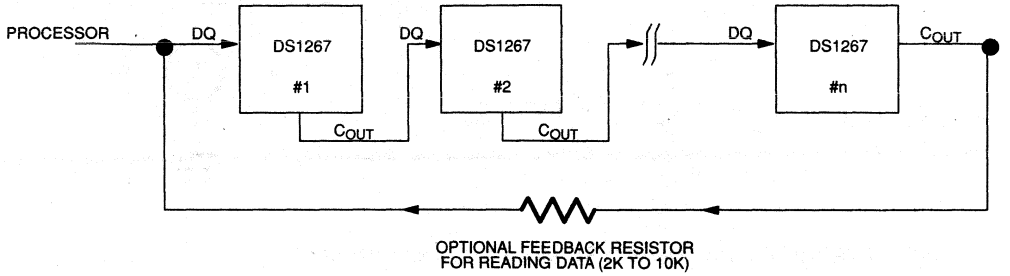
STACKED CONFIGURATION Figure 3



CASCADE OPERATION

A feature of the DS1267 is the ability to control multiple devices from a single processor. Multiple DS1267s can be linked or daisy chained as shown in Figure 4. As a data bit is entered into the I/O shift register of the DS1267 a bit will appear at the C_{OUT} output after a minimum delay of 50 nanoseconds. The stack select bit of the DS1267 will always be the first out the part at the beginning of a transaction. Additionally the C_{OUT} pin is always active regardless of the state of $\overline{RST}$. This allows one to read the I/O shift register without changing its value.

CASCADING MULTIPLE DEVICES Figure 4



The C_{OUT} output of the DS1267 can be used to drive the DQ input of another DS1267. When connecting multiple devices, the total number of bits transmitted is always 17 times the number of DS1267s in the daisy chain.

An optional feedback resistor can be placed between the C_{OUT} terminal of the last device and the first DS1267 DQ input thus allowing the controlling processor to read, as well as, write data, or circularly clock data through the daisy chain. The value of the feedback or isolation resistor should be in the range from 1K to 10K ohms.

When reading data via the C_{OUT} pin and isolation resistor, the DQ line is left floating by the reading device. When $\overline{RST}$ is driven high, bit 17 is present on the C_{OUT} pin, which is fed back to the input DQ pin through the isolation resistor. When the CLK input transitions low to high, bit 17 is loaded into the first position of the I/O shift register and bit 16 becomes present on C_{OUT} and DQ of the next device. After 17 bits (or 17 times the number of DS1267s in the daisy chain), the data has shifted completely around and back to its original position. When $\overline{RST}$ transitions to the low state to end data transfer, the value (the same as before the read occurred) is loaded into the wiper–0, wiper–1, and stack select bit I/O register.

ABSOLUTE AND RELATIVE LINEARITY

Absolute linearity is defined as the difference between the actual measured output voltage and the expected output voltage. Figure 5 presents the test circuit used to measure absolute linearity. Absolute linearity is given in terms of a minimum increment or expected output when the wiper is moved one position. In the case of the test circuit, a minimum increment (MI) or one LSB would equal 10/512 volts. The equation for absolute linearity is given as follows:

(1) ABSOLUTE LINEARITY

$$AL=\{V_O(actual) - V_O(expected)\}/MI$$

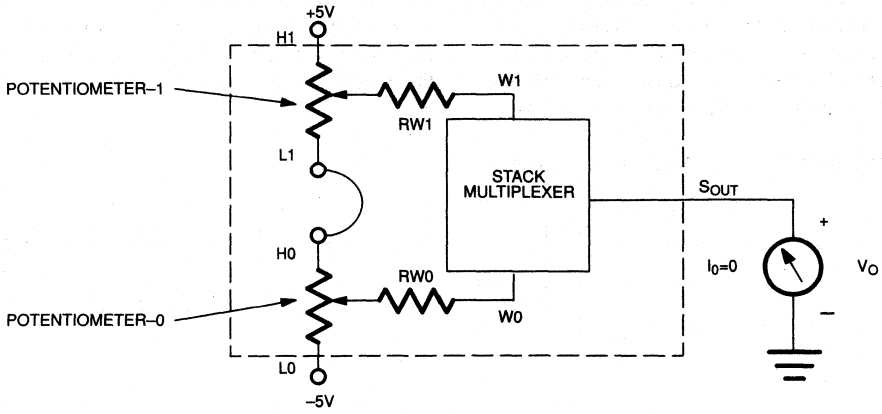
Relative Linearity is a measure of error between two adjacent wiper position points and is given in terms of MI by equation (2).

(2) RELATIVE LINEARITY

$$RL=\{V_O(n+1) - V_O(n)\}/MI$$

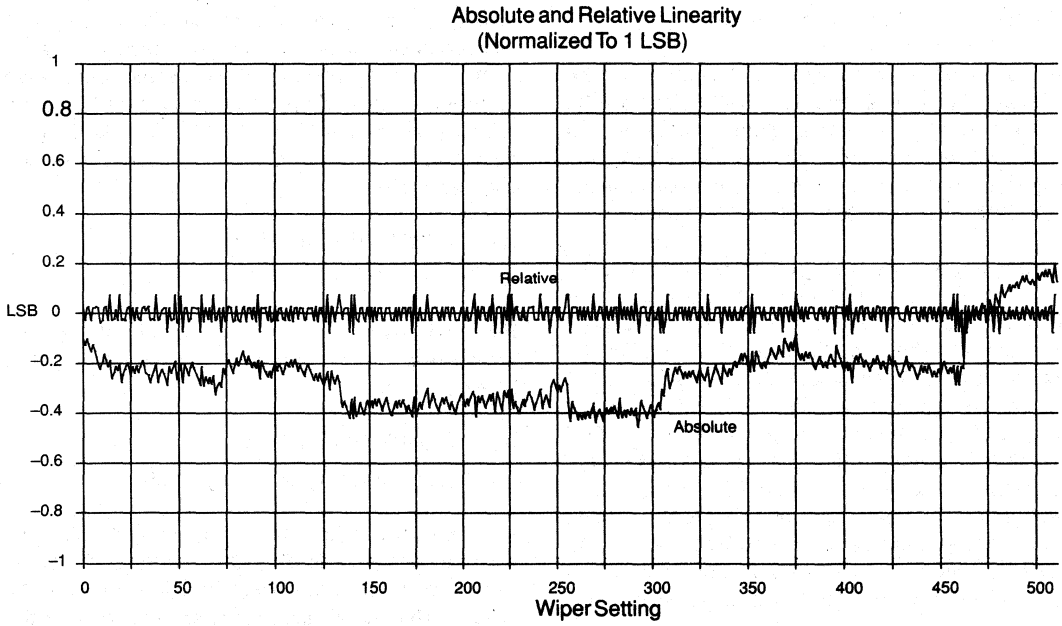
Figure 6 is a plot of absolute linearity and relative linearity versus wiper position for the DS1267 at 25°C. The specification for absolute linearity of the DS1267 is ±0.75 MI typical. The specification for relative linearity of the DS1267 is ±0.3 MI typical.

LINEARITY MEASUREMENT CONFIGURATION Figure 5



NOTE:
In this setup, a ±2% delta in total resistance R0 to R1 would cause a ±2.5 MI error.

DS1267 ABSOLUTE AND RELATIVE LINEARITY Figure 6



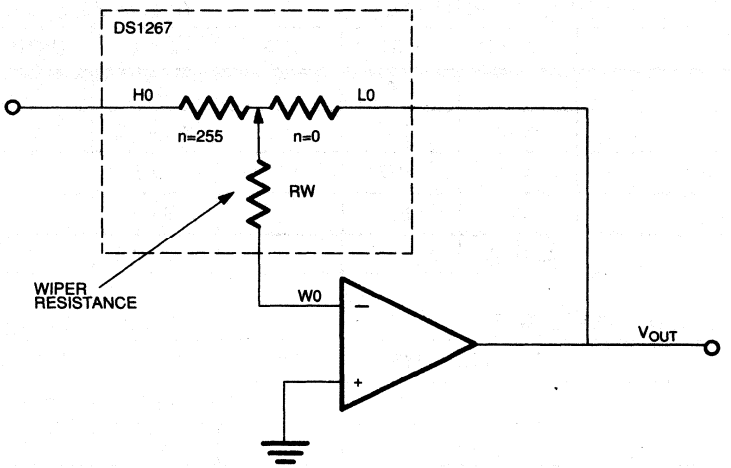
TYPICAL APPLICATION CONFIGURATIONS

Figures 7 and 8 show two typical application configurations for the DS1267. By connecting the wiper terminal of the part to a high impedance load, the effects of the wiper resistance is minimized, since the wiper resistance can vary from 400 to 1000 ohms depending on wiper voltage. Figure 7 presents the device connected in an inverting variblegain amplifier. The gain of the circuit on Figure 7 is given by the following equation:

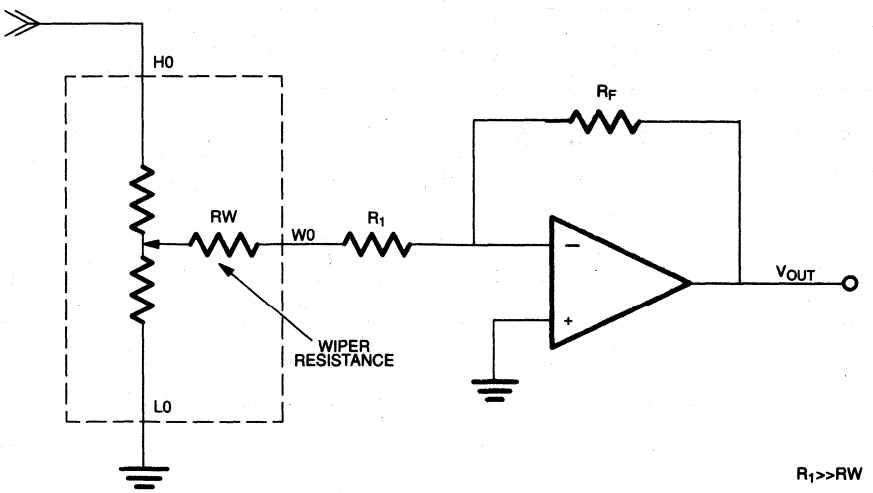
$$Av = -n/(255-n); \text{ where } n = 0 \text{ to } 255$$

Figure 8 shows the deivce operaing in a fixed gain attenuator where the potentiometer is used to attenuate an incoming signal. Note the resistance R1 is chosen to be much greater than the wiper resistance to minimize its effect on circuit gain.

INVERTING VARIABLE GAIN AMPLIFIER Figure 7



FIXED GAIN ATTENUATOR Figure 8



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground (VB=GND)	–1.0V to +7.0V
Voltage on Resistor Pins when VB=–5.5V	–5.5V to +7.0V
Voltage on V_B	–5.5 to GND
Operating Temperature	0°C to 70°C commercial; –40°C to +85°C industrial
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5		5.5	V	1
Input Logic 1	V_{IH}	2.0		V_{CC}+0.5	V	1, 2
Input Logic 0	V_{IL}	–0.5		+0.8	V	1, 2
Substrate Bias	V_B	–5.5		GND	V	1
Resistor Inputs	L, H, W	V_B–0.5		V_{CC}+0.5	V	2

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}		22	650	µA	12
Input Leakage	I_{LI}	–1		+1	µA	
Wiper Resistance	R_W		400	1000	Ω	
Wiper Current	I_W			1	mA	
Output Leakage	I_{LO}	–1		+1	µA	
Logic 1 Output @ 2.4 Volts	I_{OH}	–1			mA	8, 9
Logic 0 Output @ 0.4 Volts	I_{OL}			4	mA	8, 9
Standby Current	I_{STBY}		22		µA	

ANALOG RESISTOR CHARACTERISTICS

(0°C to 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
End–to–End Resistor Tolerance		–20		+20	%	
Absolute Linearity			±0.75		LSB	4
Relative Linearity			±0.3		LSB	5
–3 dB Cutoff Frequency	F_{CUTOFF}				Hz	7
Noise Figure						11
Temperature Coefficient			±800		ppm/C	

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	3
Output Capacitance	C_{OUT}			7	pF	3

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5.0V ± 10%)

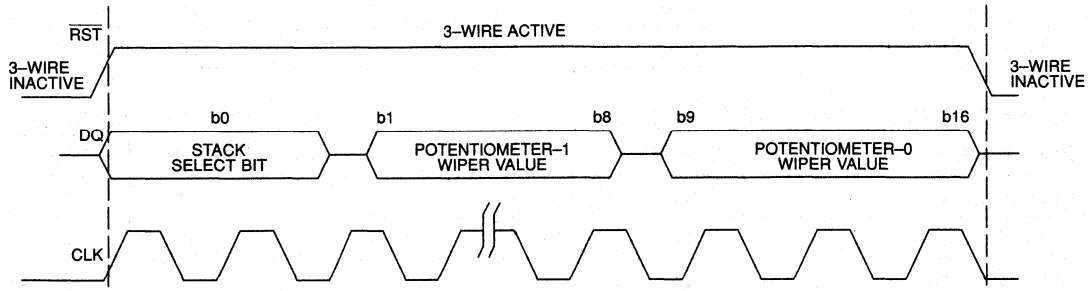
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CLK Frequency	f_{CLK}	DC		10	MHz	10
Width of CLK Pulse	t_{CH}	50			ns	10
Data Setup Time	t_{DC}	30			ns	10
Data Hold Time	t_{CDH}	10			ns	10
Propagation Delay Time Low to High Level Clock to Output	t_{PLH}			50	ns	10
Propagation Delay Time High to Low Level	t_{PLH}			50	ns	10
$\overline{RST}$ High to Clock Input High	t_{CC}	50			ns	10
$\overline{RST}$ Low from Clock Input High	t_{HLT}	50			ns	10
$\overline{RST}$ Inactive	t_{RLT}	125			ns	
Clock Low to Data Valid on a Read	t_{CDD}			30	ns	10
CLK Rise Time, CLK Fall Time	t_{CR}			50	ns	10

NOTES:

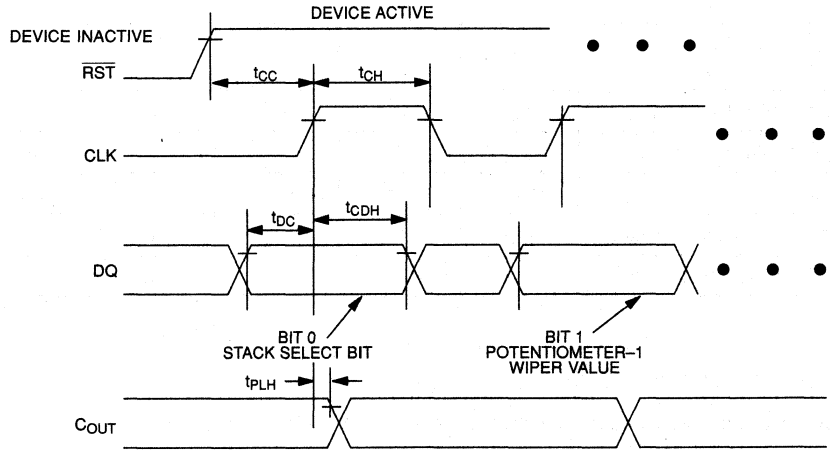
1. All voltages are referenced to ground.
2. Resistor inputs cannot exceed the substrate bias voltage, Vb, in the negative direction.
3. Capacitance values apply at 25°C.
4. Absolute linearity is used to determine wiper voltage versus expected voltage as determined by wiper position. Device test limits ±1.6 LSB.
5. Relative linearity is used to determined the change in voltage between successive tap positions. Device test limits ±0.5 LSB.
6. Typical values are for ta = 25°C and nominal supply voltage.
7. –3 dB cutoff frequency characteristics for the DS1267 depend on potentiometer total resistance: DS1267–010; 1 MHz, DS1267–050; 200 KHz, DS1267–100; 100 KHz.
8. Cout is active regardless of the state of $\overline{RST}$.
9. V_{REF}= 1.5 volts .
10. See Figure 9(a), (b), and (c).
11. Noise < –120 dB/√Hz. Reference 1 volt (thermal).
12. See Figure 11.

TIMING DIAGRAMS Figure 9

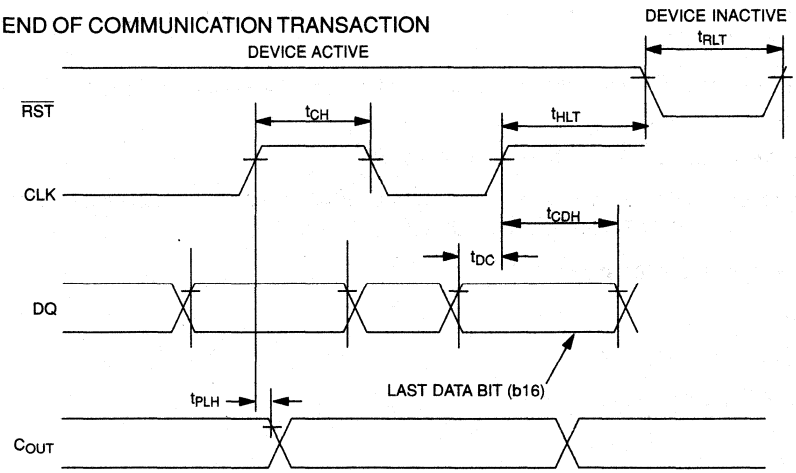
(A) 3–WIRE SERIAL INTERFACE GENERAL OVERVIEW



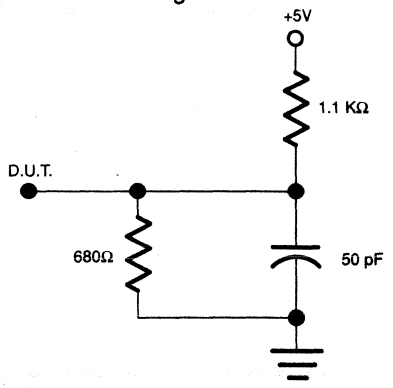
(B) START OF COMMUNICATION TRANSACTION



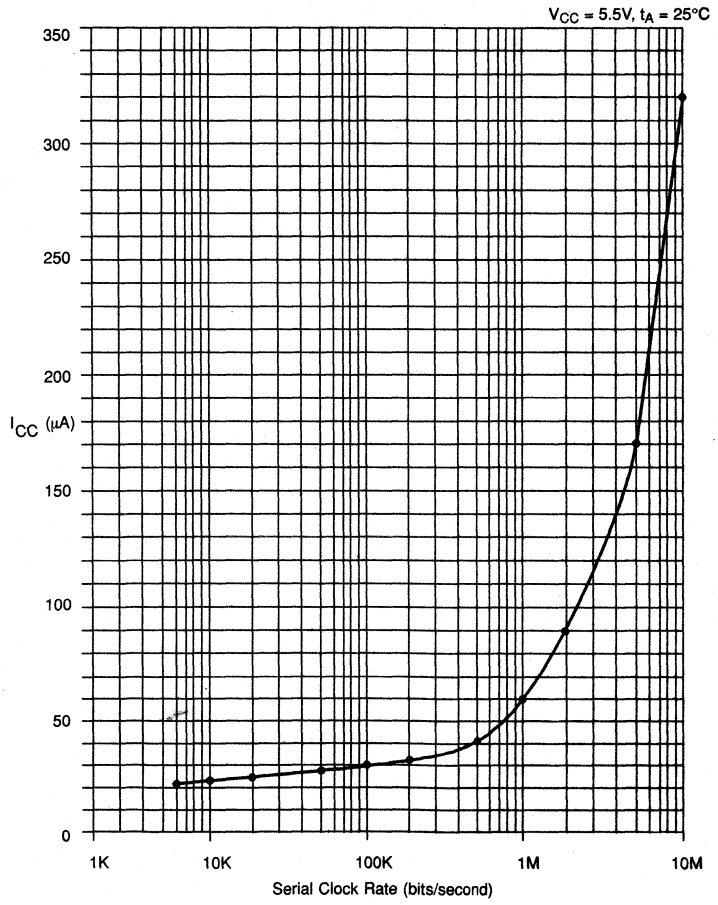
(C) END OF COMMUNICATION TRANSACTION



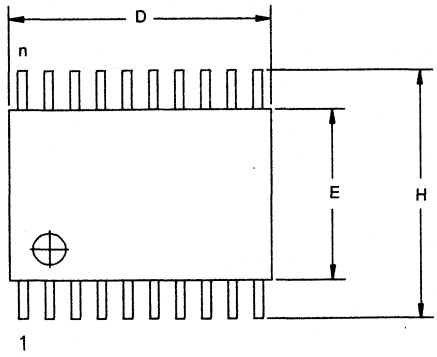
DIGITAL OUTPUT LOAD SCHEMATIC Figure 10

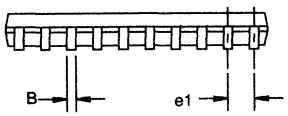


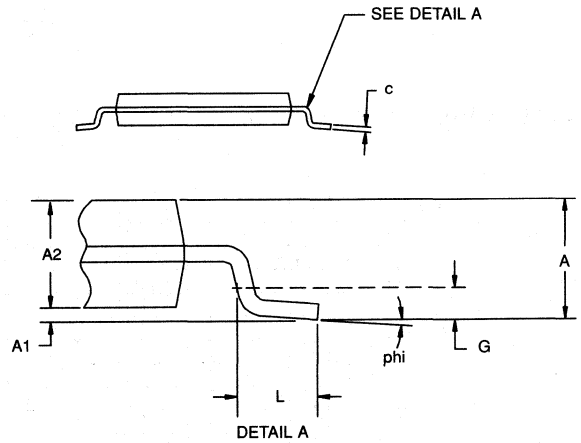
TYPICAL SUPPLY CURRENT VS. SERIAL CLOCK RATE Figure 11



DS1267E 20-PIN TSSOP







DIM	MIN	MAX
A MM	–	1.10
A1 MM	0.05	–
A2 MM	0.75	1.05
C MM	0.09	0.18
L MM	0.50	0.70
e1 MM	0.65 BSC	
B MM	0.18	0.30
D MM	6.40	6.90
E MM	4.40 NOM	
G MM	0.25 REF	
H MM	6.25	6.55
phi	0°	8°

DALLAS SEMICONDUCTOR

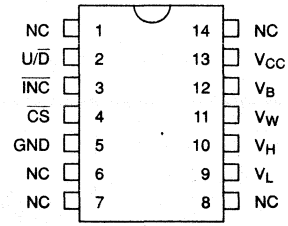
DS1666, DS1666S
Audio Digital Resistor

FEATURES

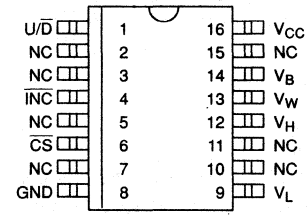
- 128 position, digitally controlled potentiometer
- Operates from a +5 volts power supply with TTL signal inputs
- Wide analog voltage range of ±5 volts
- Resistive elements are temperature compensated to ±20 percent end to end
- Low–power CMOS
- 14–pin DIP or 16–pin SOIC for surface mount applications
- Default position on power up sets wiper position at 10%
- Operating temperature range
  - 0°C to 70°C; commercial version
  - –40°C to +85°C; industrial version

		Resolution/Step		
Resistance values		Low End	High End	-3dB Point
DS1666-10	10KΩ	24Ω	152Ω	1.1 MHz
DS1666-50	50KΩ	122Ω	759Ω	200 KHz
DS1666-100	100KΩ	243Ω	1.519KΩ	100 KHz

PIN ASSIGNMENT



14-Pin DIP (300 Mil)
See Mech. Drawing – Pg. 480



16-Pin SOIC (300 Mil)
See Mech. Drawing – Pg. 484

PIN DESCRIPTION

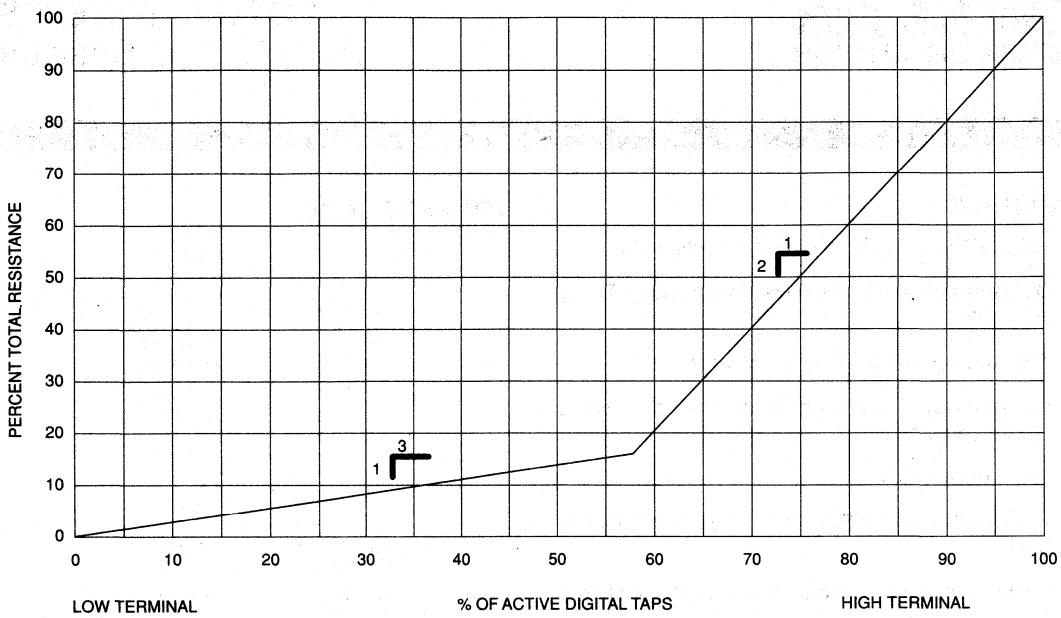
V_H	-	High Terminal of Resistor
V_L	-	Low Terminal of Resistor
V_W	-	Wiper Terminal of Resistor
$\overline{U/D}$	-	Up/Down Control
$\overline{INC}$	-	Wiper Movement Control
$\overline{CS}$	-	Chip Select for Wiper Movement
NC	-	No Connection
V_{CC}	-	+5 Volts
GND	-	Ground
V_B	-	0 to –5 Volts

DESCRIPTION

The DS1666 is a solid–state potentiometer which is set to value by digitally controlled resistive elements. The potentiometer is composed of 127 resistive sections. Between each resistive section and both ends of the potentiometer are TAP points accessible to the wiper. The position of the wiper on the resistance array is controlled by the $\overline{CS}$, $\overline{U/D}$ and $\overline{INC}$ inputs. The position of the wiper defaults to the 10% position on power up. The resolution of the DS1666 is shown in Figure 1.

The DS1666 Digital Audio Resistor is uniquely designed to provide a potentiometer that is logarithmic rather than linear across its entire range. The lower half of the potentiometer advances 1% of total resistance for each 3% of scale advanced, providing for precise amplification of low volume signals. The upper half of the potentiometer advances 2% of resistance for every 1% of scale advanced, providing for the lower resolution gain required for high volume amplification.

GRAPH OF AUDIO TAPER Figure 1



OPERATION

The $\overline{CS}$, U/$\overline{D}$ and $\overline{INC}$ inputs control the position of the wiper along the resistor array (Figure 1). When $\overline{CS}$ is active (low), a high to low transition on the $\overline{INC}$ will increment or decrement an internal counter depending on the level of the U/$\overline{D}$ pin. When the U/$\overline{D}$ pin is low, the counter will decrement. When the U/$\overline{D}$ pin is high, the counter will increment. The state of the U/$\overline{D}$ pin can be changed while $\overline{CS}$ is active allowing for precise adjustment during calibration. The output of the counter is decoded to set the position of the wiper. When the $\overline{CS}$ input transitions to the high (inactive) level, the value of the counter is stored and the wiper position is maintained until power (V_{CC}) is lost. When power is restored, the DS1666 returns to the default setting and positions the wiper to 10 percent. The value of the end-to-end and end-to-wiper position is indeterminate while V_{CC} is not applied.

The DS1666 has a resistor array that resembles an audio taper potentiometer as shown in Figure 1 1. Since the taper is not linear, exact resistance values for each of the 128 positions of the resistor is not specified. However, the end-to-end resistance is specified to be within ±20 percent of the stated resistor value over a temperature range of 0°C to 70°C for commercial version and –40°C to +85°C for industrial version of the part.

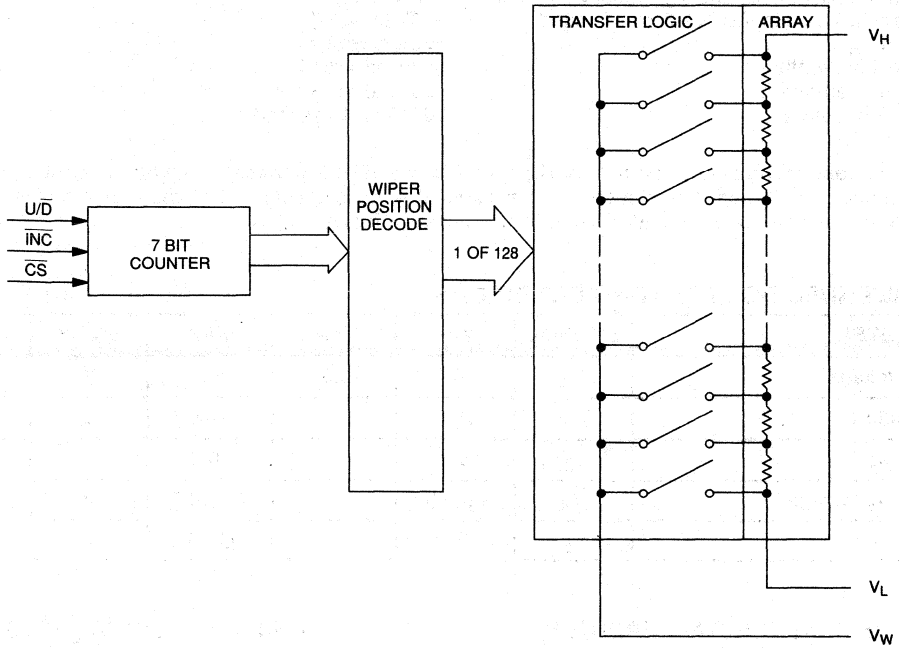
ANALOG CHARACTERISTICS

End-to-End Resistance Tolerance = ±20 percent
Typical Noise = <120 dB/Hz REF:IV
Temperature Coefficient = ±800 PPM/°C typical
Resistance at tap #74=18% ± 2% of total resistance.

PIN DESCRIPTIONS

V_H	The high end of the potentiometer. This terminal is capable of handling input voltages between ±5 volts.
V_L	The Low end of the potentiometer. This terminal is capable of handling input voltages between ±5 volts.
V_W	The wiper terminal of the potentiometer. The value of the wiper is controlled by the U/$\overline{D}$ and the $\overline{INC}$ pins.
Up/Down (U/$\overline{D}$)	The U/$\overline{D}$ input controls the direction of the wiper movement when setting the potentiometer.
Increment ($\overline{INC}$)	Toggling $\overline{INC}$ will move the potentiometer wiper by either incrementing or decrementing the counter.
Chip Select ($\overline{CS}$)	The device is selected when $\overline{CS}$ input is low. The current counter value is stored when CS is returned high.

BLOCK DIAGRAM Figure 2



MODE SELECTION Figure 3

$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	MODE
L	↓	H	WIPER UP
L	↓	L	WIPER DOWN
↓	H	X	STORE WIPER POSITION

ABSOLUTE MAXIMUM RATINGS*

Voltage on $\overline{CS}$, $\overline{INC}$, $U/\overline{D}$, and V_{CC} Relative to Ground	–0.5V to +7.0V
Voltage on V_H, V_L, and V_W Relative to Ground	-6.5V to +6.5V
Voltage on V_B	-6.5V to Ground
Operating Temperature	–40°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	+4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.0		V_{CC}+0.5	V	1
Input Logic 0	V_{IL}	-0.5		+0.8	V	1
V_H, V_L, V_W Voltage	V_R	V_B-0.3		V_{CC}+0.3	V	1
V_B Voltage	V_B	-5.5		GND	V	1

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC} = 5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}		0.1	5	mA	3
Input Leakage	I_{LI}	-1		+1	µA	2
Wiper Resistance	R_W		350	650	Ω	
Wiper Current	I_W			1	mA	3

CAPACITANCE

(t_A = 25°C)

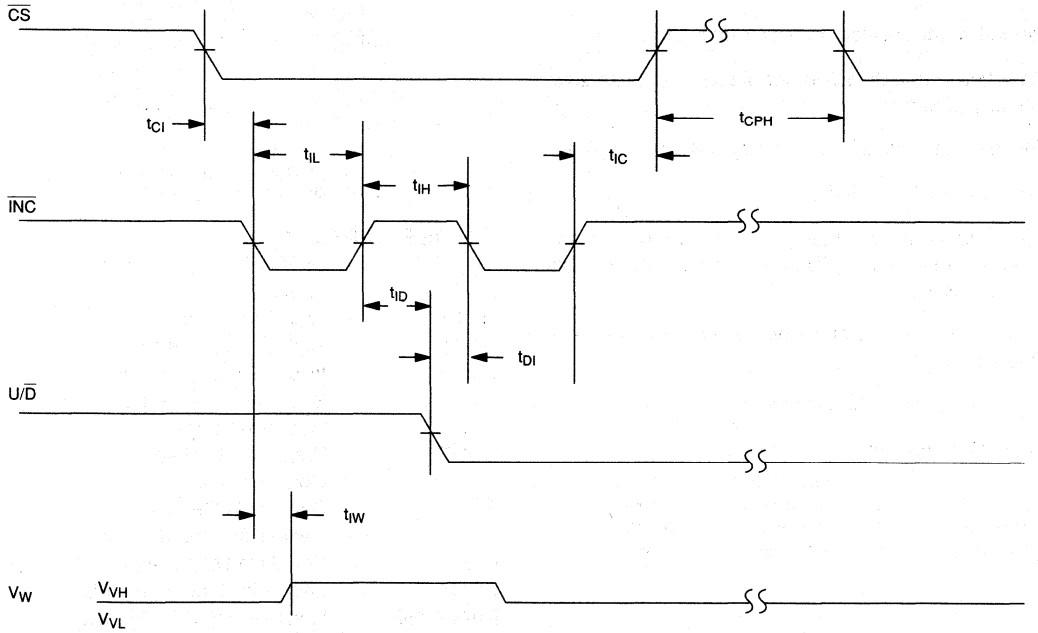
PARAMETER	SYMBOL	CONDITION	TYP	MAX	UNITS	NOTES
Capacitance	C_{IN}	t_A=25°C	6	10	pF	2

AC ELECTRICAL CHARACTERISTICS

(t_A=–40°C to +85°C; V_{CC}=+5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CS}$ to $\overline{INC}$ Setup	t_{CI}	100			ns	
$\overline{INC}$ High to U/$\overline{D}$ Change	t_{ID}	100			ns	
U/$\overline{D}$ to $\overline{INC}$ Setup	t_{DI}	1			µs	
$\overline{INC}$ Low Period	t_{IL}	500			ns	
INC High Period	t_{IH}	1			µs	
$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	t_{IC}	500			ns	
$\overline{CS}$ Deselect Time	t_{CPH}	100			ns	

AC TIMING Figure 4



NOTES:

1. All voltages are referenced to ground.
2. This parameter is periodically sampled and not 100% tested.
3. Typical values are for t_A = 25°C and nominal supply voltages.
4. Wiper output open circuited.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10 ns
Input Level	1.5V

DALLAS SEMICONDUCTOR

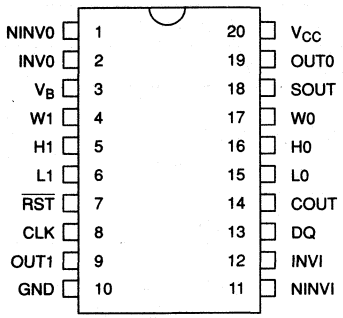
DS1667
Digital Resistor with OP AMP

FEATURES

- Two digitally controlled 256-position potentiometers
- Serial port provides means for setting and reading both potentiometers
- Resistors can be connected in series to provide additional resolution
- Default wiper position on power up is 50%
- Resistive elements are temperature compensated to ±20% end to end
- Two high gain wide bandwidth operational amplifiers
- Low power CMOS design
- Applications include analog–to–digital and digital–to–analog converters, variable oscillators, and variable gain amplifiers
- 20–pin DIP package or optional 20–pin SOIC surface mount package
- Operating temperature range of 0°C to 70°C
- Resistance Values

		RESOLUTION	-3 dB POINT
DS1667-10:	10K	39 ohms	1.1 MHz
DS1667-50:	50K	195 ohms	200 kHz
DS1667-100:	100K	390 ohms	100 kHz

PIN ASSIGNMENT



20-Pin DIP (300 Mil) and 20-Pin SOIC
See Mech. Drawings – Pgs.480 & 484

PIN DESCRIPTION

V_{CC}	-	+5 Volt Supply
GND	-	Ground
L0, L1	-	Low End of Resistor
H0, H1	-	High End of Resistor
W0, W1	-	Wiper End of Resistor
V_B	-	Substrate Bias and OP AMP Negative Supply
SOUT	-	Wiper for Stacked Configuration
$\overline{RST}$	-	Serial Port Reset Input
DQ	-	Serial Port Input/Output
CLK	-	Serial Port Clock Input
COUT	-	Cascade Serial Port Output
NINV0, NINVI	-	Noninverting OP AMP Input
INV0, INVI	-	Inverting OP AMP Input
OUT0, OUT1	-	OP AMP Outputs

DESCRIPTION

The DS1667 is a dual–solid state potentiometer that is adjustable by digitally selected resistive elements. Each potentiometer is composed of 256 resistive elements. Between each resistive section of each potentiometer are tap points accessible to the wiper. The position of the wiper on the resistive array is set by an 8–bit register that controls which tap point is connected to the wiper output. Each 8–bit register can be read or written by sending or receiving data bits over a 3–wire serial port. In addition, the resistors can be stacked such that a single potentiometer of 512 sections results. When two separate potentiometers are used, the resolution of the DS1667 is equal to the resistance value divided by 256. When the potentiometers are stacked end to end, the resistance value is doubled while the resolution remains the same. The DS1667 also contains two high gain wide bandwidth operational amplifiers. Each amplifier has both the inverting and non-inverting inputs and the output available for user configuration. The operational amplifiers can be paired with the resistive ele-

ments to perform such functions as analog to digital conversion, digital to analog conversion, variable gain amplifiers, and variable oscillators.

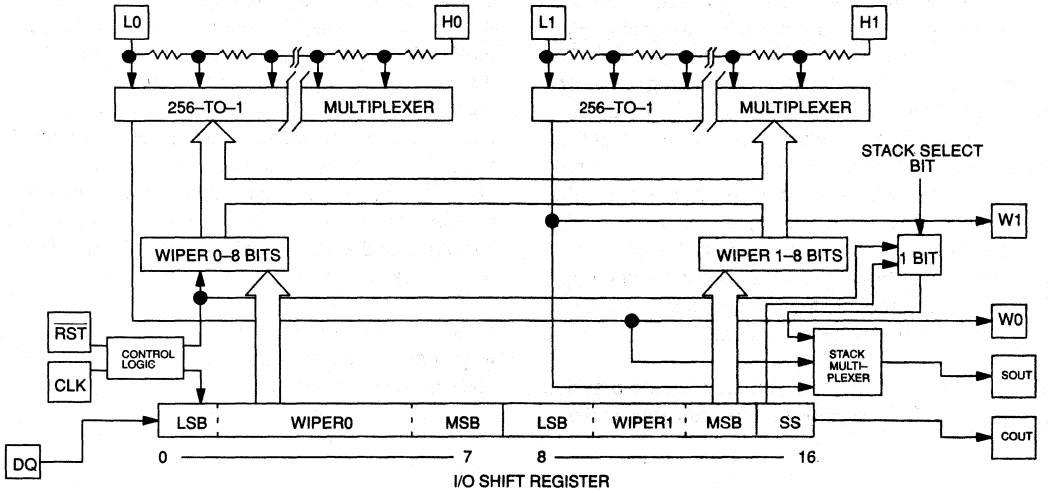
OPERATION - DIGITAL RESISTOR SECTION

The DS1667 contains two potentiometers, each of which has its wiper set by a value contained in an 8 bit register (see Figure 1). Each potentiometer consists of 256 resistors of equal value with tap points between each resistor and at the low end.

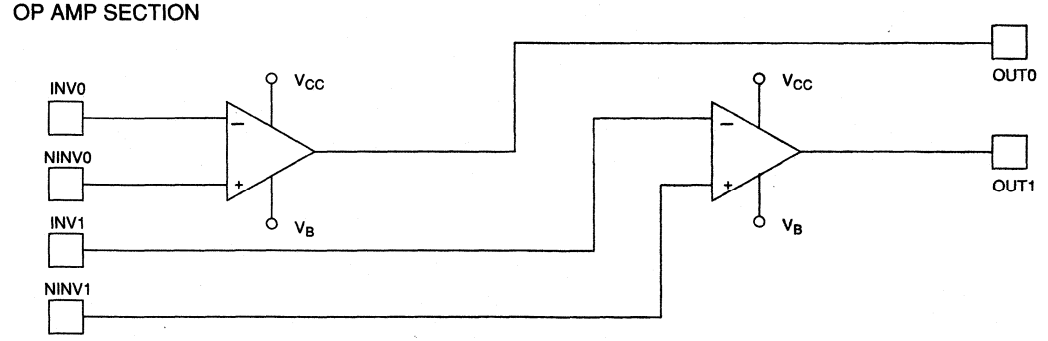
In addition, the potentiometer can be stacked by connecting them in series such that the high end of potentiometer 0 is connected to the low end of potentiometer 1. When stacking potentiometers, the stack select bit is used to select which potentiometer wiper will appear at the stack multiplexer output (SOUT). A zero written to the stack multiplexer will connect wiper 0 to the SOUT pin. This wiper will determine which of the 256 bottom taps of the stacked potentiometer is selected. When a 1 is written to the stack multiplexer, wiper 1 is selected and one of the upper 256 taps of the stacked potentiometer is presented at the SOUT pin.

BLOCK DIAGRAM Figure 1

RESISTOR SECTION



OP AMP SECTION



Information is written to and read from the wiper 0 and wiper 1 registers and the stack select bit via the 17-bit I/O shift register. The I/O shift register is serially loaded by a 3 wire serial port consisting of $\overline{RST}$, DQ, and CLK. It is updated by transferring all 17 bits (Figure 2). Data can be entered into the 17 bit shift register only when the $\overline{RST}$ input is at a high level. While at a high level, the $\overline{RST}$ function allows serial entry of data via the D/Q pin. The potentiometers always maintain their previous value until $\overline{RST}$ is taken to a low level, which terminates data transfer. While $\overline{RST}$ input is low, the DQ and CLK inputs are ignored.

Valid data is entered into the I/O shift register while $\overline{RST}$ is high on the low-to-high transition of the CLK input. Data input on the DQ pin can be changed while the clock input is high or low, but only data meeting the setup requirements will enter the shift register. Data is always entered starting with the value of the stack select bit. The next 8 bits to be entered are those specifying the wiper 1 setting. The MSB of these 8 bits is sent first. The next 8 bits to be entered are those specifying the wiper 0 setting, sent MSB first. The 17th bit to be entered, therefore, will be the least significant bit of the wiper 0 setting. If fewer than 17 bits are entered, the value of the potentiometer settings will result from the number of bits that were entered plus the remaining bits of the old value shifted over by the number of bits sent. If more than 17 bits are sent, only the last 17 bits are left in the shift register. Therefore, sending other than 17 bits can produce indeterminate potentiometer settings.

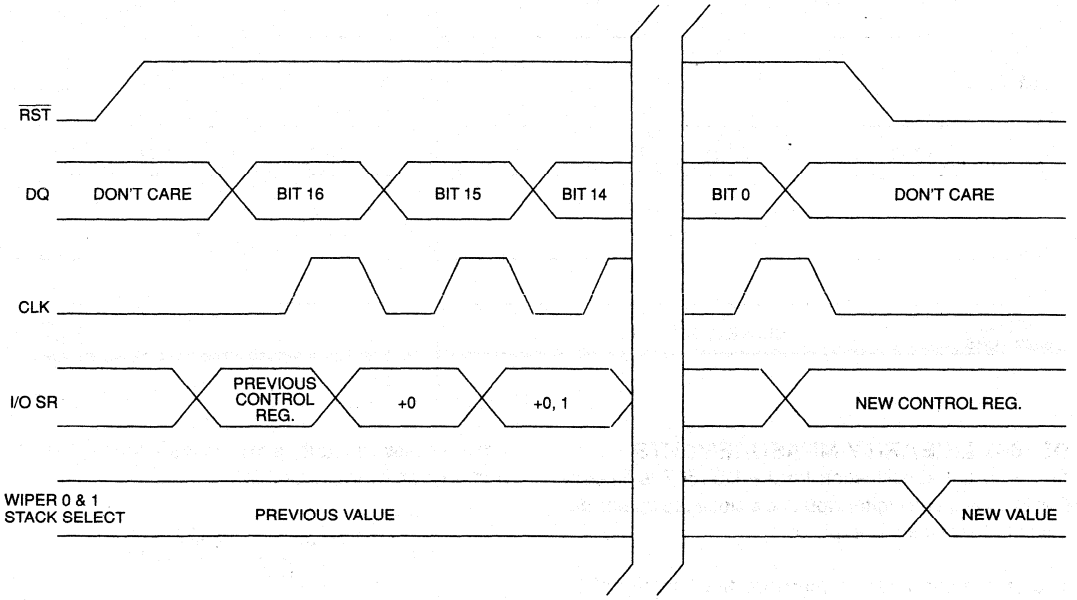
As bits are entered into the shift register, the previous value is shifted out bit by bit on the cascade serial port pin (COUT). By connecting the COUT pin to the DQ pin of a second DS1667, multiple devices can be daisy chained together as shown in Figure 3.

When connecting multiple devices, the total number of bits sent is always 17 times the number of DS1667s in the daisy chain. In applications where it is desirable to read the settings of potentiometers, the COUT pin of the last device connected in a daisy chain must be connected back to the DQ input of the first device through a resistor with a value of 1K to 10K. This resistor provides isolation between COUT and DQ when writing to the device (see Figure 3).

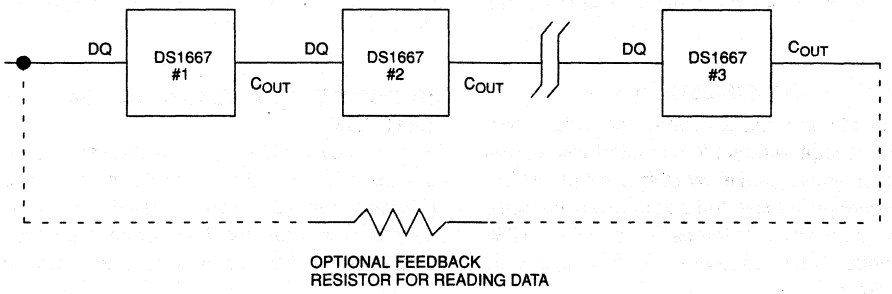
When reading data, the DQ line is left floating by the reading device. When $\overline{RST}$ is held low, bit 17 is always present on the COUT pin, which is fed back to the input DQ pin through the resistor (see Figure 4).This data bit can now be read by the reading device. The $\overline{RST}$ pin is then transitioned high to initiate a data transfer. When the CLK input transitions low to high, bit 17 is loaded into the first position of the I/O shift register and bit 16 becomes present on COUT and DQ. After 17 bits (or 17 times the number of devices for a daisy chain), the data has shifted completely around and back to its original position. When $\overline{RST}$ is transitioned back low to end data transfer, the value (the same as before the read occurred) is loaded into the wiper 0 and wiper 1 registers and the stack select bit.

When power is applied to the DS1667, the device always has the wiper settings at half position and the stack select bit is at zero.

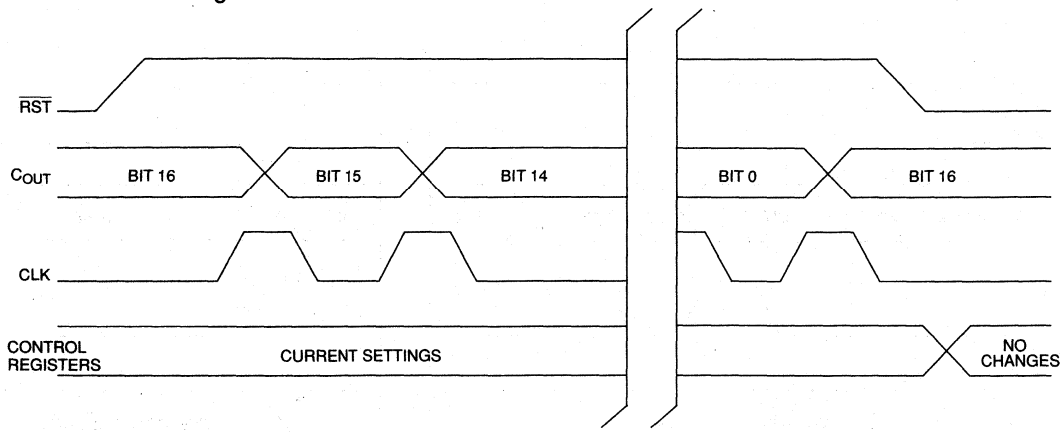
WRITING DATA Figure 2



CASCADING MULTIPLE DEVICES Figure 3



READING DATA Figure 4



DS1667 LINEARITY MEASUREMENTS

An important specification for the DS1667 is linearity, that is, for a given digital input, how close the analog output is to that which is expected.

The test circuit used to measure the linearity of the DS1667 is shown in Figure 5. Note that to get an accurate output voltage it is necessary to assure that the output current is 0, in order to negate the effects of wiper impedance RW which is typically 400 ohms. For any given setting N for the pot, the expected voltage output at SOUT is:

$$VO = -5 + [10 \times (N/256)] \text{ (in volts)}$$

Absolute linearity is a comparison of the actual measured output voltage versus the expected value given by the equation above, and is given in terms of an LSB, which is the change in expected output when the digital input is incremented by 1. In this case the LSB is 10/256 or 0.03906 volts. The equation for the absolute linearity of the DS1667 is:

$$\frac{V_O(\text{actual}) - V_O(\text{expected})}{LSB} = AL \text{ (in LSBs)}$$

The specification for absolute linearity of the DS1667 is ± 1 LSB typical.

Relative linearity is a comparison of the difference of actual output voltages of two successive taps and the difference of the expected output voltages of two successive taps. The expected difference of output voltages is 1 LSB or 0.03906V for the measurement system of Figure 5. Relative linearity is expressed in terms of an LSB and is given by the equation:

$$\frac{\Delta V_O(\text{actual}) - LSB}{LSB} = RL$$

The specification for relative linerity of the DS1667 is ± 0.5 LSB typical.

Figure 6 is a plot of absolute linearity (AL) and relative linearity (RL) versus wiper setting for a typical DS1667 at 25°C.

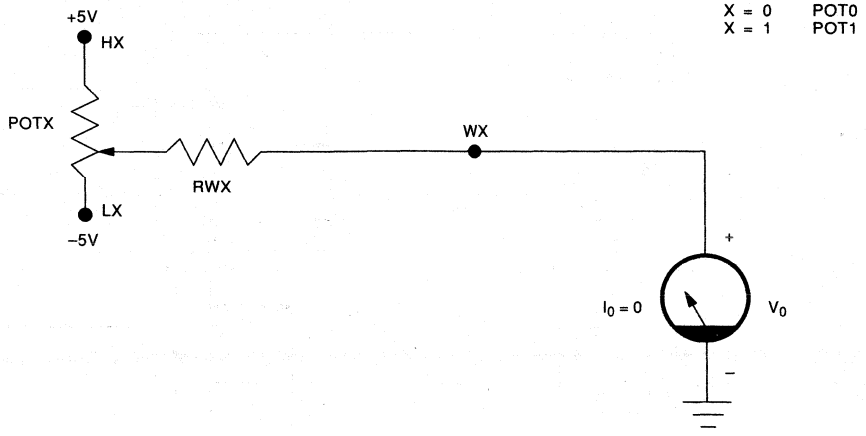
DESCRIPTION AND OPERATION - OP AMP SECTION

The DS1667 contains two operational amplifiers which are ideal for operation from a single 5V supply and ground or from ±5V supplies (see Figure 1). An internal resistor divider defines the internal reference of the op amp to be halfway between the power supplies, i.e.:

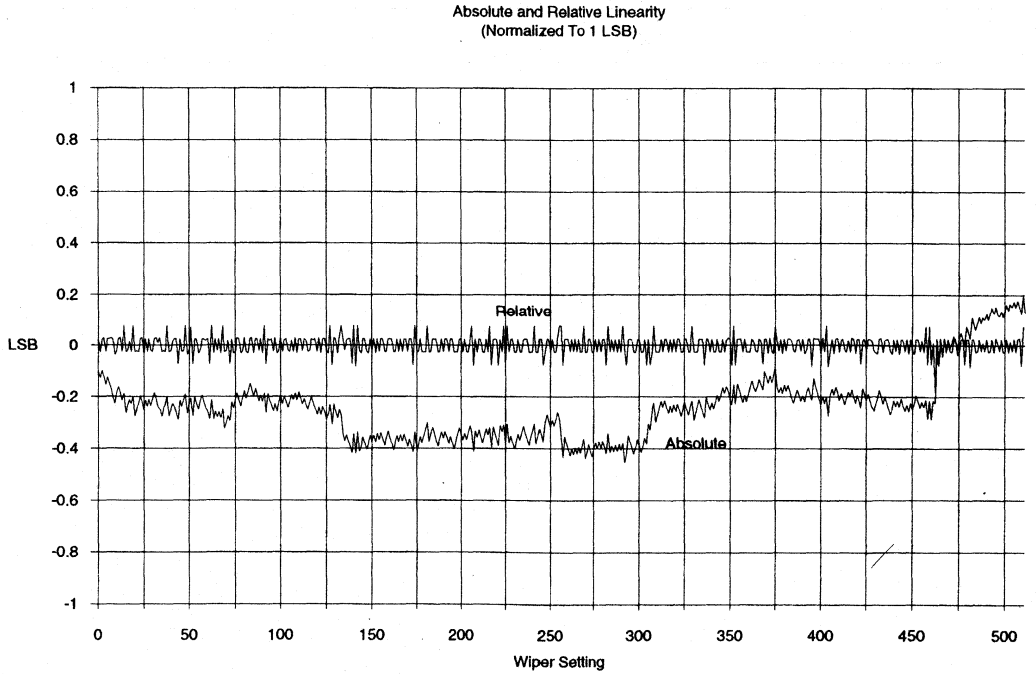
$$\frac{V_{DD} + V_B}{2}$$

For optimal performance, choose analog ground to be this value. The operational amplifiers feature rail to rail output swing in addition to an input common mode range that includes the positive rail. Performance features include broad band noise immunity as well as voltage gain into realistic loads specified at both 600 ohms and 2K ohms. High voltage gain is produced with low input offset voltage and low offset voltage drift. Current consumption is less than 1.9 mA per amplifier and the device is virtually immune to latchup.

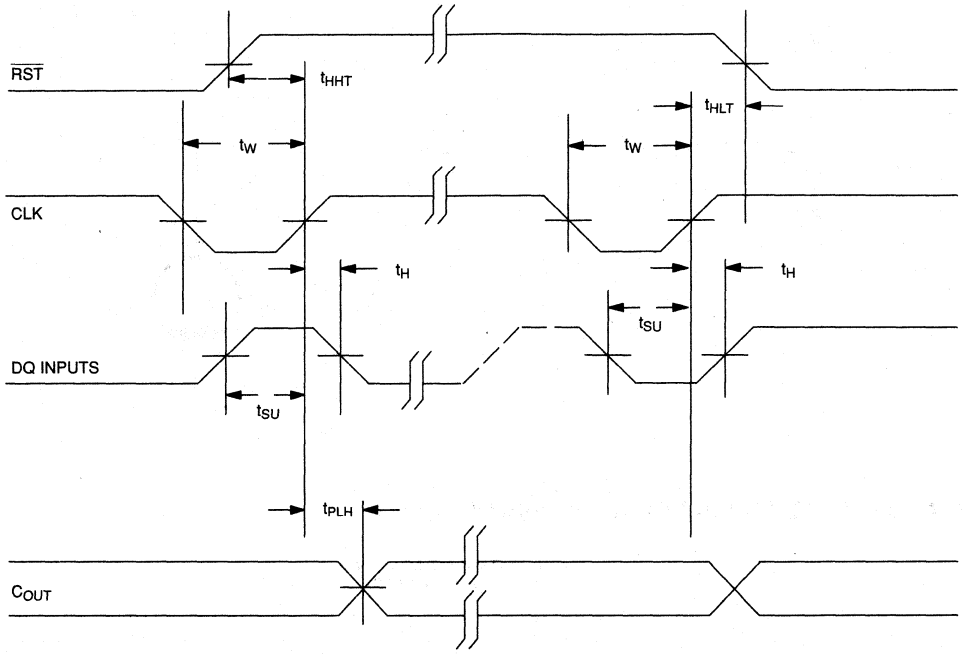
LINEARITY MEASUREMENT CONFIGURATION Figure 5



DS1667 ABSOLUTE AND RELATIVE LINEARITY Figure 6



TIMING DIAGRAM: RESISTOR SECTION Figure 7



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground (V_B = GND)	–0.5V to +7.0V
Voltage on Resistor Pins when V_B = -5.5V	-5.5V to +7.0V
Voltage on V_B	-5.5V to GND
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS RESISTOR SECTION

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Positive Supply Voltage	V_{CC}	+4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.0		V_{CC}+0.5	V	1
Input Logic 0	V_{IL}	-0.5		+0.8	V	1
Negative Supply Voltage	V_B	-5.5		GND	V	1
Resistor Inputs	L, H, W	V_B - 0.5		V_{CC} + 0.5	V	2

DC ELECTRICAL CHARACTERISTICS RESISTOR SECTION

(0°C to 70°C; V_{CC} = 5.0V ± 10%, V_B = -5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Positive Supply Current	I_{CC}		3	5	mA	
Negative Supply Current	I_B		3	5	mA	
Input Leakage	I_U	–1		+1	µA	
Wiper Resistance	R_W		400	1000	ohms	
Wiper Current	I_W			1	mA	
Output Leakage	I_{LO}	–1		+1	µA	
Logic 1 Output @ 2.4 Volts	I_{OH}	–1.0			mA	
Logic 0 Output @ 0.4 Volts	I_{OL}			4	mA	
End–to–End Resistor Tolerance	TOL_R	–20		+20	%	
Noise (ref: 1V)	N		–120		$\frac{dB}{\sqrt{Hz}}$	
Absolute Linearity	AL		1.0		LSB	
Relative Linearity	RL		0.5		LSB	
Resistor Temperature Coefficient	TC_R			850	$\frac{ppm}{°C}$	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS RESISTOR SECTION

(0°C to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CLK Frequency	f_{CLK}			10	MHz	
Width of CLK Pulse	t_W	50			ns	
Data Setup Time	t_{SU}	30			ns	
Data Hold Time	t_H	10			ns	
Propagation Delay Time Low to High Level Clock to Output	t_{PLH}			50	ns	3
$\overline{RST}$ High to Clock Input High	t_{HHT}	50			ns	
$\overline{RST}$ Low from Clock Input High	t_{HLT}	50			ns	

OPERATIONAL AMPLIFIER SECTION
DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 10%, V_B = -5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Offset Voltage	V_{OS}		5	10	mV	
Input Offset Voltage Drift	V_{OSD}		10		uV/°C	
Common Mode Rejection	CM_R		62		dB	
Positive Power Supply Rejection	$+PS_R$		62		dB	
Negative Power Supply Rejection	$-PS_R$		62		dB	
Input Common Mode Voltage Range	C_{CCM}	V_B+1.5V		V_{CC}	V	
Large Signal Voltage Gain			106		dB	R_L=2KΩ
Large Signal Voltage Gain			96		dB	R_L=600KΩ
Output Swing	V_{SWGH}	4.6	4.7		V	R_L=2KΩ to GND
Output Swing	V_{SWGL}		–4.7	–4.6	V	V_B = –5V
Output Swing	V_{SWGH}	4.5	4.6		V	R_L=600KΩ to GND
Output Swing	V_{SWGL}		–4.6	–4.5	V	V_B = –5V
Output Current	$V_{O,SOURCE}$	13	58		mA	V_O = 0V
Output Current	$V_{O,SINK}$	13	63		mA	V_O = +5V

OPERATIONAL AMPLIFIER SECTION
AC ELECTRICAL CHARACTERISTICS

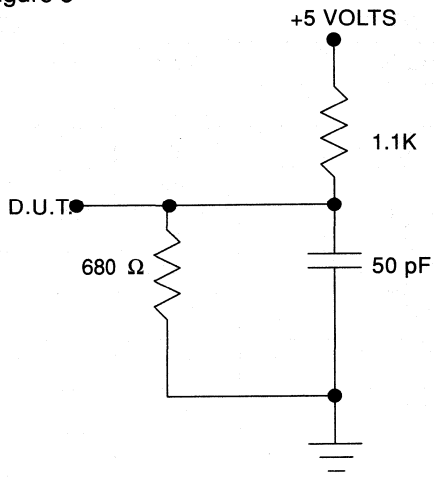
(0°C to 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Slew Rate	V_{SL}	0.7	2		V/µs	6
Gain Bandwidth Product	GBP		2.5		MHz	5
Phase Margin	PM		75		deg	5
Gain Margin	GM		20		dB	5
Amp–to–Amp Isolation	AAI		130		dB	
Input Referred Voltage Noise	IRVF		100		$nV/\sqrt{Hz}$	F=1 KHz
Input Referred Current Noise	IRV1		.0002		$pA/\sqrt{Hz}$	F=1 KHz
Total Harmonic Distortion	HD		0.1		%	F=10 KHz AV=–10 RL=2KΩ V_O=1V_{PP}

NOTES:

1. All voltages are referenced to ground.
2. Resistor inputs cannot exceed the substrate bias voltage in the negative direction
3. Measured with a load as shown in Figure 8.
4. Over a frequency range of 0 - 1 KHz.
5. Load is R_L = 600 Ω C_L = 10 pF
6. V_{DD} = +5.0V V_B = -5.0V connected as voltage follower with 10V step input and R_L = ∞.
7. To achieve best op amp performance, V_{DD} = +5.0V V_B = -5.0V and analog ground = 0V. In general analog ground = $\frac{V_{DD} + V_B}{2}$.
8. OP AMPS idle, no load.

LOAD SCHEMATIC Figure 8



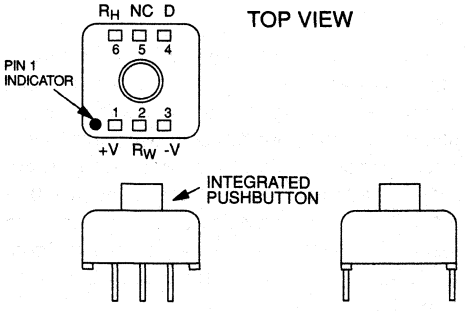
DALLAS SEMICONDUCTOR

DS1668, DS1669, DS1669S
Dallastat™ Electronic Digital Rheostat

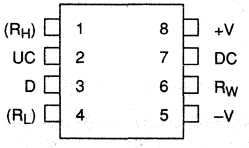
FEATURES

- Replaces mechanical variable resistors
- Available as the DS1668 with manual interface or the DS1669 integrated circuit
- Human engineered interface provides easy control with DS1668
- Electronic interface provided for digital as well as manual control
- Wide differential input voltage range between 4.5 and 8 volts
- Wiper position is maintained in the absence of power
- Low cost alternative to mechanical controls
- Applications include volume, tone, contrast, brightness, and dimmer control
- 8–pin SOIC and 8–pin DIP packages for DS1669
- Standard resistance values for Dallastat
  - DS1668/DS1669–10 ~ 10KΩ
  - DS1668/DS1669–50 ~ 50KΩ
  - DS1668/DS1669–100 ~ 100KΩ
- Operating Temperature Range
  - Commercial: 0°C to 70°C; DS1668, DS1669
  - Industrial: –40°C to +85°C; DS1669

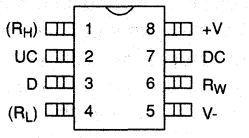
PIN ASSIGNMENT DS1668



PIN ASSIGNMENT DS1669



8-Pin DIP (300 Mil)
See Mech. Drawing
Pg. 480



8-Pin SOIC (200 Mil)
See Mech. Drawing
Pg. 483

PIN DESCRIPTION DS1669

R_H	-	Resistor High End
R_W	-	Resistor Wiper
R_L	-	Resistor Low End
-V, +V	-	Voltage Inputs
UC	-	Up Contact Input
D	-	Digital Input
DC	-	Down Contact Input

PIN DESCRIPTION DS1668

+V	-	Positive Voltage Input
-V	-	Negative Voltage
R_W	-	Resistor Wiper
D	-	Digital Input
R_H	-	Resistor High End
NC	-	No Connection - Pin Missing

DESCRIPTION

The DS1668 and DS1669 Dallastats are digital rheostats or potentiometers. These units provide 64 possible uniform tap points over the resistive range and are available in standard versions of 10K, 50K, and 100K ohms. The Dallastats can be controlled by either a mechanical–type contact closure input or a digital source input such as a CPU. Wiper position is maintained in the absence of power which is accomplished through the use of a EEPROM memory cell array. The EEPROM cell array is specified to accept greater than 80,000 writes.

The DS1668 and DS1669 differ in the type packages in which they are offered. The DS1668 is only available in a custom 6–pin package with a single integrated pushbutton as shown in the package drawing. The single integrated pushbutton provides the mechanical control input of the wiper position. In addition, a digital source input, D, allows the potentiometer to be controlled by a microcontroller or processor. Other package pins include the positive voltage input, +V, the negative voltage input, –V, the resistor wiper terminal, R_W, and the high resistor terminal, R_H. The DS1668 is rated for commercial temperature usage only (0°C to 70°C).

The DS1669 is offered in two standard IC packages which include an 8–pin 300 mil DIP and an 8–pin 200 mil SOIC. Like the DS1668, the DS1669 can be configured to operate using a single pushbutton or digital source input. This is illustrated in Figure 1. Additionally, the DS1669 can be configured to operate in a dual pushbutton configuration which is shown in Figure 2. The DS1669 pinouts allow access to both ends of the potentiometer R_L, R_H, and the wiper, R_W. Control inputs include the digital source input, D, the up contact input, UC, and the down contact input, DC. Other package pinouts include the positive,+V, and negative, –V , supply inputs. The DS1669 is available in commercial or industrial temperature versions.

OPERATION

The DS1668/DS1669 Dallastats are controlled through a contact closure input or by a digital source input. The DS1668 is configured to operate from a single contact closure (pushbutton) input which is integrated in the custom 6–pin package or the device can be driven from the digital source input (D). The DS1669 can be controlled using a single pushbutton input, dual pushbutton, or using the digital source input.

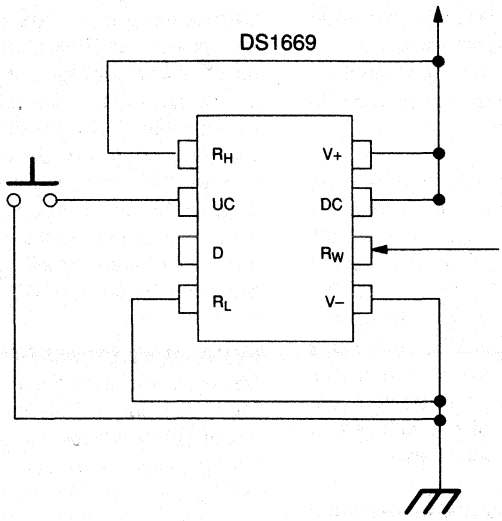
Figure 3 illustrates the single pushbutton configuration of the DS1668. Internally, the low end resistor terminal is connected to the negative supply input terminal. The integrated pushbutton has one side connected to the negative supply input while the other side is connected to the up contact terminal (UC). The digital source input (D) is accessible through pin 4 of the package. The (D) input has an internal pull–up resistor and can be allowed to float when not in use. The down contact input (DC) is not accessible externally. However, this control input is internally connected to the positive input supply.

When powered, the DS1668 assumes a single pushbutton mode of operation. Pressure applied to the integrated pushbutton will cause contact closure which in turn will move the wiper position upward or downward depending on the previous wiper direction. Single pushbutton mode is accomplished in the same manner for the DS1669. However, for the DS1669, all connections must be made by the user since no internal connections exist (see Figure 1). Note that single pushbutton control is accomplished when 1) the (DC) input is connected to the positive supply input and 2) the (D) input is allowed to float. These two conditions must exist from the time of device power–up. The UC input controls both upward and downward movement of the device wiper position in single pushbutton mode of operation.

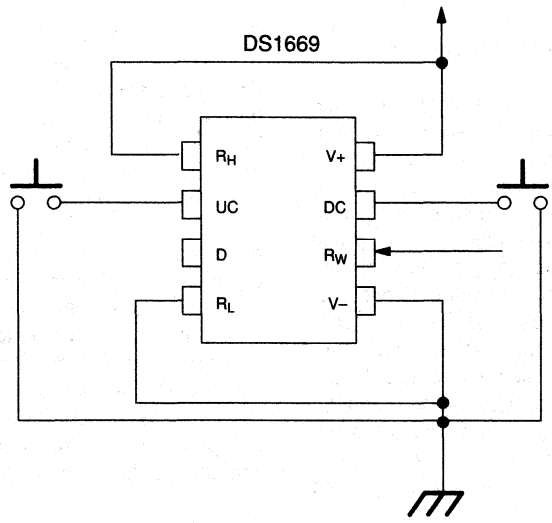
Dual pushbutton operation is only available when using the DS1669. The DS1668, by design, only supports the single pushbutton mode of operation and digital source input control. Figure 2 provides a typical application example of the dual pushbutton configuration for the DS1669. In dual–pushbutton mode, the up–contact input (UC) is used solely to provide upward movement of the wiper position and the down–contact input (DC) is used to provide downward movement of the wiper position. For dual pushbutton configuration, all control inputs (UC, DC, and D) must remain open on device power–up.

The digital source input, D, was designed for microprocessor or controller applications. This control input manipulates the device in the same manner as the single pushbutton configuration; controlling movement of the wiper position in both upward and downward directions. One added feature over the single pushbutton configuration is the ability to increment or decrement wiper position at a faster rate. Digital source input control is available regardless of the type of pushbutton configuration.

DS1669 SINGLE PUSHBUTTON CONFIGURATION (TYPICAL EXAMPLE) Figure 1



DS1669 DUAL PUSHBUTTON CONFIGURATION (TYPICAL APPLICATION) Figure 2



Dallastats interpret input pulse widths as the means of controlling wiper movement. A single pulse width input over the UC, DC, or D terminals will cause the wiper position to move 1/64th of the total resistance. All inputs, UC, DC, or D, are inactive when in the high state. A transition from a high to low on these inputs is considered the beginning of pulse activity.

A single pulse is defined as being greater than 1 ms but lasting no longer than a second when using the contact closure inputs UC and DC. When using the D input a single pulse is defined as being greater than 1 µs but lasting no longer than 1 second. This is shown in Figures 4a and 6a. Repetitive pulsed inputs can be used to step through each resistive position of the device (see Figures 4a and 6b). The requirement for repetitive pulsed inputs is that pulses must be separated by a minimum time of 1 ms. If not, the Dallastat will interpret repetitive pulses as a single continuous pulse.

Pulse inputs lasting longer than 1 second will cause the wiper to move one position every 100 ms following the initial 1 second hold time. The total time to transcend the entire potentiometer using a continuous input pulse is given in the equation below:

1 (second) + 63 X 100 ms = 7.3 (seconds)

In single pushbutton mode or when using the digital source input, as the wiper reaches the end of the potentiometer its direction of movement reverses. This will occur whether or not the input is a continuous pulse or a sequence of repetitive pulses. Changing the direction of wiper movement in single pushbutton mode or digital source mode is also accomplished by a period of inactivity on the UC or D inputs for (minimum) 1 second or greater. In dual pushbutton mode, the direction is controlled by the UC and DC inputs. No wait states are required to change wiper direction in dual pushbutton mode. Additionally, in dual pushbutton mode as the wiper reaches the end of the potentiometer, the direction of wiper movement will not change. Wiper position will remain at the potentiometers' end until an opposite direction input is given.

All control inputs, UC, DC, and D, are internally pulled up with a 100K ohm resistance. Additionally, the UC and DC inputs are internally debounced and require no external components for input signal conditioning.

The DS1668/DS1669 are provided with two supply inputs –V and +V. The maximum voltage difference between the two supply inputs is + 8.0 volts while the minimum voltage difference is +4.5 volts. All input levels are referenced to the negative supply input, –V. The voltage applied to any Dallastat terminal must not exceed the negative supply voltage (–V) by –0.5 or the positive supply voltage (+V) by + 0.5 volts. The minimum logic high level must be +2.4 volts with reference to the –V supply voltage input. A logic low level with reference to the –V supply voltage has a maximum value of +0.8 volts. Dallastats exhibit a typical wiper resistance of 400 ohms with a maximum wiper resistance of 1000 ohms. The maximum wiper current allowed through the Dallastat is specified at 1 milliamps (see DC Electrical Characteristics).

NONVOLATILE WIPER SETTINGS

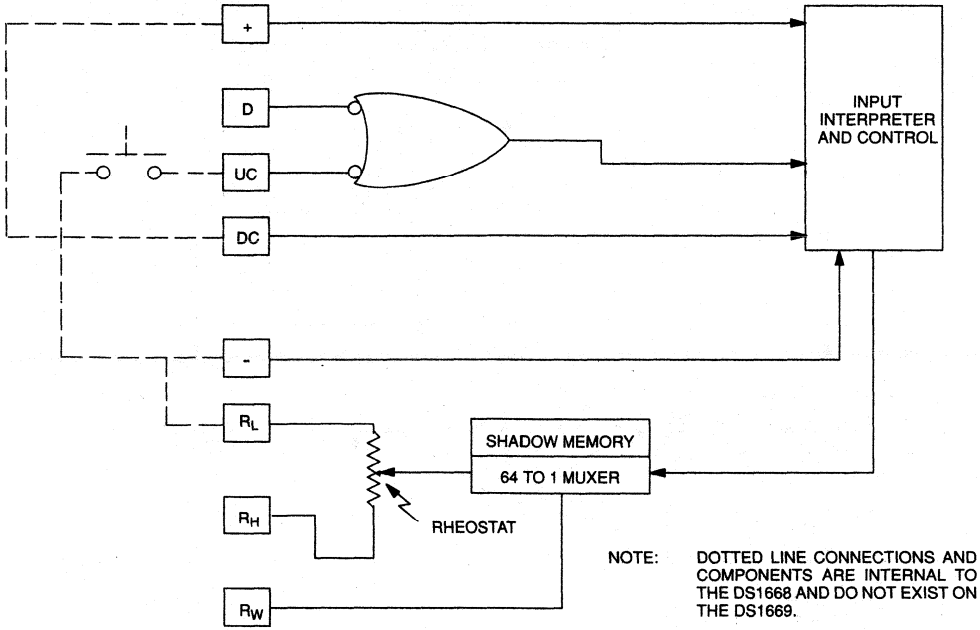
Dallastats maintain the position of the wiper in the absence of power. This feature is provided through the use of EEPROM type memory cell arrays. During normal operation the position of the wiper is determined by the input multiplexer. Periodically, the multiplexer will update the EEPROM memory cells. The manner in which an update occurs has been optimized for reliability, durability, and performance. Additionally, the update operation is totally transparent to the user.

When power is applied to the Dallastat, the wiper setting will be the last recorded in the EEPROM memory cells. If the Dallastat setting is changed after power is applied, the new value will be stored after a delay of 2 seconds. The initial storage of a new value after power–up, occurs when the first change is made, regardless of when this change is made.

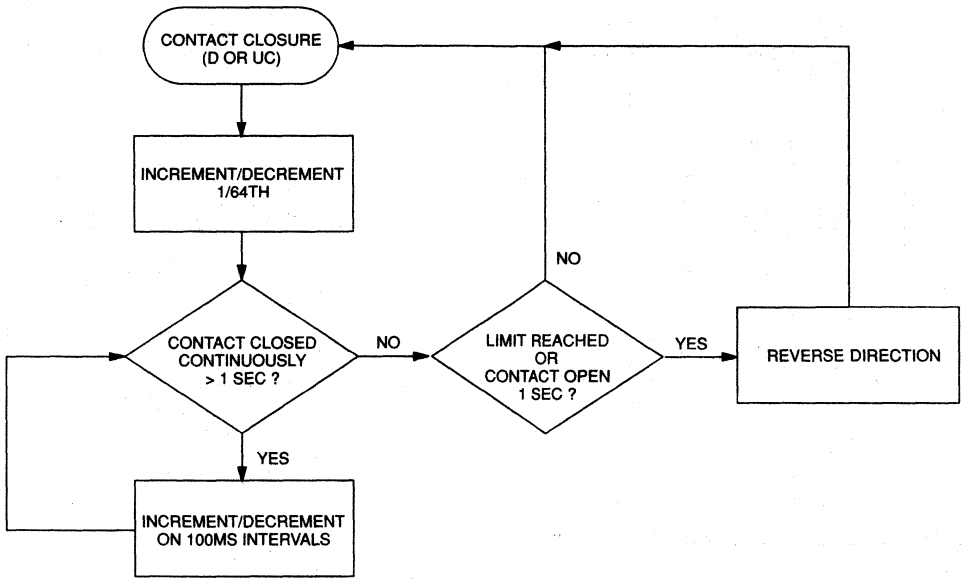
After the initial change on power–up, subsequent changes in the Dallastat EEPROM memory cells will occur only if the wiper position of the part is moved greater than 12.5% of the total resistance range. Any wiper movement after initial power–up which is less than 12.5% will not be recorded in the EEPROM memory cells. Since the Dallastat contains a 64–to–1 multiplexer, a change of greater than 12.5% corresponds to a change of the fourth LSB.

Changes or storage to the EEPROM memory cells must allow for a 2 second delay to guarantee that updates will occur. The EEPROM memory cells are specified to accept greater than 80,000 writes before a wear–out condition. If the EEPROM memory cells do reach a wear–out condition, the Dallastat will still function properly while power is applied. However, on power–up the device's wiper position will be that of the position last recorded before memory cell wear out.

DS1668 DALLASTAT™ BLOCK DIAGRAM Figure 3

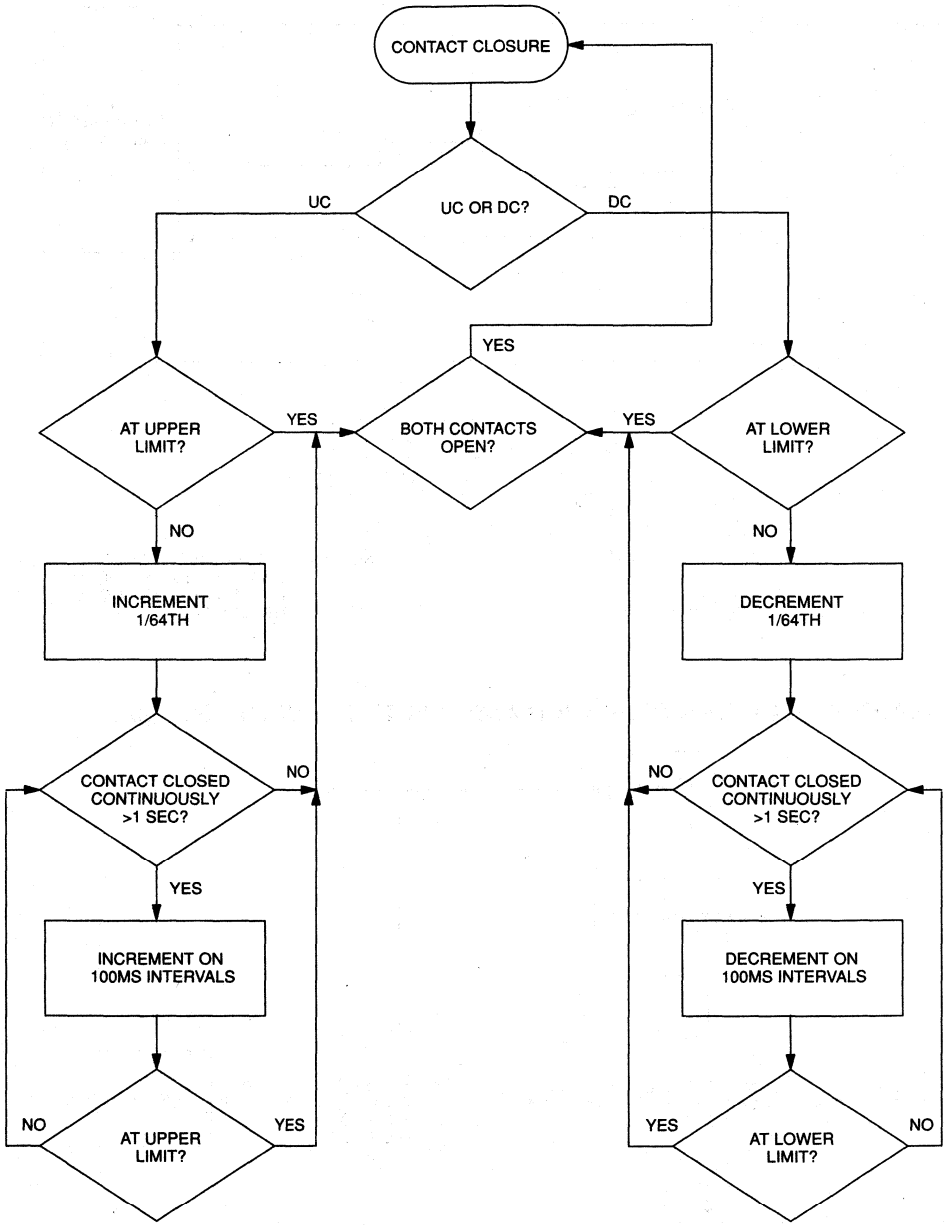


FLOWCHART: ONE BUTTON OPERATION AND ELECTRICAL CONTROL Figure 4



CONTACT OPEN AND CONTACT CLOSURE TIMING IS 1s ± 10%

FLOWCHART: TWO BUTTON OPERATION Figure 5



CONTACT OPEN AND CONTACT CLOSURE TIMING IS 1 sec. ± 10%

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to -V	-V –0.5V + 8.0V
Operating Temperature	0°C to 70°C commercial; –40°C to +85°C industrial
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 15 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
+ Supply Voltage	+V	-V + 4.5		-V + 8.0	V	
- Supply Voltage	-V	+V - 8.0		+V - 4.5	V	
Rheostat Inputs	R_H,R_W,R_L	-V - 0.5		+V + 0.5	V	
Logic Input 1	V_{IH}	+2.4			V	1, 2
Logic Input 0	V_{IL}			+0.8	V	1, 2

DC ELECTRICAL CHARACTERISTICS

(-40°C to +85°C; -V to +V = 4.5V to 8.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
+, - Supply Current	I_{CC1}		1	2	mA	3
Supply Current, Idle State	I_{CC2}			100	nA	9
Wiper Resistance	R_W		400	1000	Ω	
Wiper Current	I_W			1	mA	5
Rheostat Current	I_H, I_L			1	mA	5
Power–Up Time	t_{PU}			10	µs	10

AC ELECTRICAL CHARACTERISTICS

(-40°C to +85°C; -V to+V = 4.5V to 8.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Digital Input Pulse Width	t_{DPW}	1		DC	µs	1, 7, 8
Contact Pulse Width	t_{CPW}	1		DC	ms	1, 7, 8
Repetitive Input Pulse High Time	t_{HPW}	1		DC	ms	1, 7, 8
Continuous Input Pulse	t_{CCP}	1		DC	s	1, 7, 8

ANALOG RESISTOR CHARACTERISTICS

(-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
End–to–End Resistor Tolerance		–20		+20	%	
Absolute Linearity		–0.75		+0.75	LSB	11
Relative Linearity		–0.3		+0.3	LSB	12
–3 dB Cutoff Frequency Noise Figure	fcutoff				Hz	13
Temperature Coefficient		–800		+800	ppm/C	

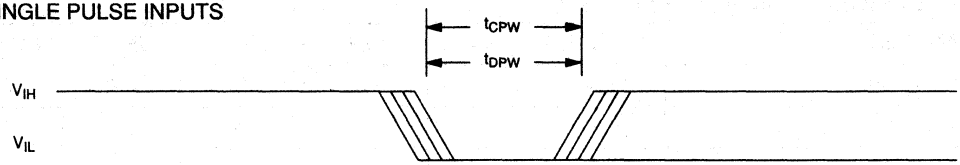
CAPACITANCE

(t_A=25°C)

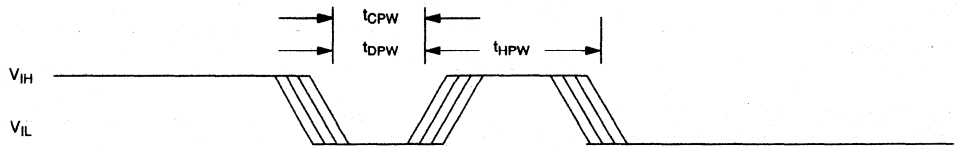
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	6
Output Capacitance	C_{OUT}			7	pF	6

TIMING DIAGRAMS Figure 6

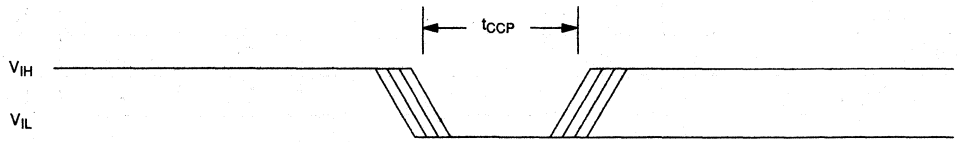
(A) SINGLE PULSE INPUTS



(B) REPETITIVE PULSE INPUTS



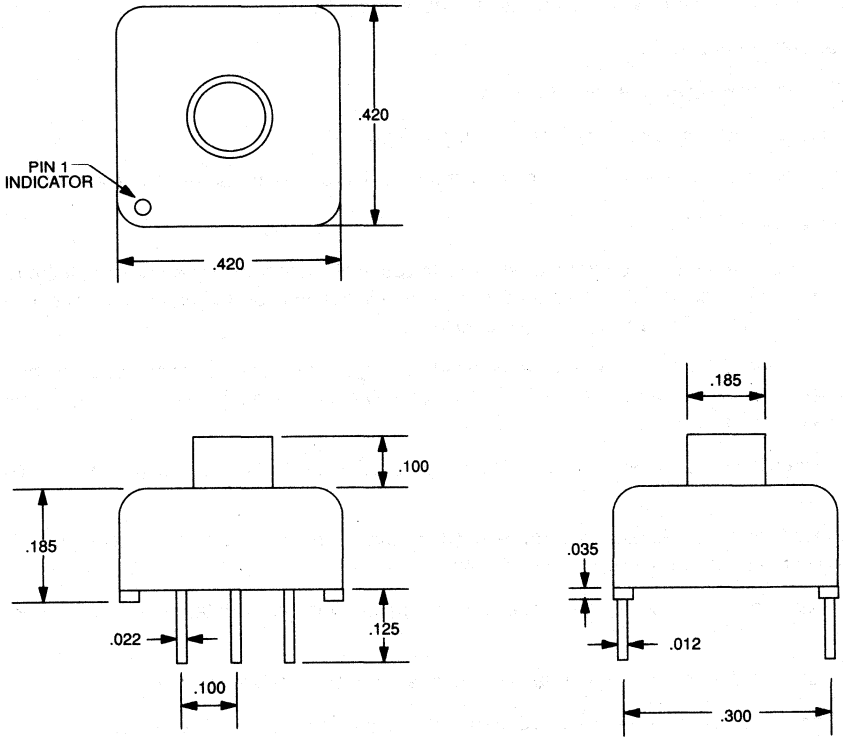
(C) CONTINUOUS PULSE INPUTS



NOTES:

1. All inputs; UV, DC, and D are internally pulled up with a resistance of 100KΩ.
2. Input logic levels are referenced to -V.
3. I_{CC} is the internal current that flows between -V and +V.
4. Input leakage applies to contact inputs UC and DC and digital input (D).
5. Wiper current and rheostat currents are the maximum current which can flow in the resistive elements.
6. Capacitance values apply at 25°C.
7. Input pulse width is the minimum time required for an input to cause an increment or decrement. If the UC, DC or D input is held active for longer than 1 second, subsequent increments or decrements will occur on 100 ms intervals until the inputs UC, DC, and/or D is released to V_{IH}.
8. Repetitive pulsed inputs on UC, DC, or D will be recognized as long as the pulse repetition occurs within 1 second of each other. Pulses occurring faster than 1 ms apart may not be recognized as individual inputs but can be interpreted a constant input.
9. Idle state supply current is measured with no pushbutton depressed and with the wiper. R_W tied to a CMOS load.
10. Maximum time required for the Dallastat to determine single or dual push button operation after input supply has reached 10% recommended supply operating conditions.
11. Aboslute linearity is used to determine wiper voltage versus expected voltage as determined by wiper position.
12. Relative linearity is used to determine the change in voltage between successive tap positions.
13. –3 dB cutoff frequency characteristics for the DS1669 depend on potentiometer total resistance: DS1669–010; 1 MHz, DS1669–050; 200 KHz, DS1669–100; 100 KHz.

DS1668 PUSHBUTTON DIMENSIONS



PRODUCT PREVIEW

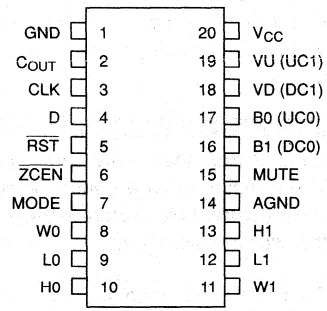
DALLAS SEMICONDUCTOR

DS1802
Dual Audio Taper Potentiometer with Pushbutton Control

FEATURES

- Ultra–low power consumption
- Operates from 3V or 5V supplies
- Two digitally controlled, 65–position potentiometers including mute
- Logarithmic resistive characteristics (1 dB per step)
- Zero–crossing detection eliminates noise caused by wiper movement
- Digital or mechanical push–button wiper control
- Serial port provides means for setting and reading both potentiometer wipers
- 20–pin SOIC and 20–pin TSSOP for surface mount applications
- Temperature:
  - Commercial: 0°C to 70°C
- Software and hardware mute

PIN ASSIGNMENT



20–PIN DIP (300 MIL)
20–PIN SOIC (300 MIL)
20–PIN TSSOP (173 MIL)
See Mech. Drawings
Pgs. 480, 484 & 485

PIN DESCRIPTION

L0, L1	–	Low End of Resistor
H0, H1	–	High End or Resistor
W1, W2	–	Wiper End of Resistor
V_{CC}	–	3V/5V Power Supply Input
$\overline{RST}$	–	Serial Port Reset Input
D	–	Serial Port Data Input
CLK	–	Serial Port Clock Input
MODE	–	Mode Select Input
UC0, UC1	–	Up Control Pushbutton Inputs
DC0, DC1	–	Down Control Pushbutton Inputs
VU, VD	–	Volume Up/Volume Down Inputs
B0, B1	–	Balance Pot–0, Pot–1 Inputs
GND	–	Digital Ground
MUTE	–	Mute
AGND	–	Analog Ground
$\overline{ZCEN}$	–	Zero Crossing Detect
C_{OUT}	–	Cascade Output

DESCRIPTION

The DS1802 is a dual audio taper–potentiometer having logarithmic resistive characteristics over the device range. Each potentiometer provides 65 wiper positions with a 1 dB increment per step and device mute. The DS1802 has two methods of device control which include contact closure (push–button) inputs and a 3–wire serial interface for wiper positioning. The push–button control inputs provide a simple interface for device control without the need for a CPU. While the 3–wire serial interface, using a CPU, provides the user the ability of reading or writing exact wiper positions of the two potentiometers. The DS1802 can also be configured to operate in either independent or "stereo" modes, when using pushbutton control. Independent mode of operation allows for independent wiper control and stereo mode of operation provides single input control over both potentiometer wiper positions. The DS1802 is offered in commercial temperature versions. Packages for the part include a 20–pin DIP, 20–pin SOIC, and 20–pin TSSOP.

OPERATION

The DS1802 provides two 65–position potentiometers per package; each having a logarithmic resistive characteristic as shown in Table 1. The DS1802 can be controlled either digitally, or mechanically using a 3–wire serial interface or contact closure input, respectively. The push–button interface allows for a simple mechanical control method for incrementing or decrementing wiper position. The 3–wire serial interface is designed for CPU controlled applications and allows the potentiometer's exact wiper position to be read or written. Additionally, the DS1802 can be daisy chained for multi–device environments.

Figure 1 presents a block diagram of the DS1802. As shown, the inputs from the 3–wire serial interface and contact closure inputs drive a command/control unit. The command/control unit interprets these inputs for control of the two potentiometers.

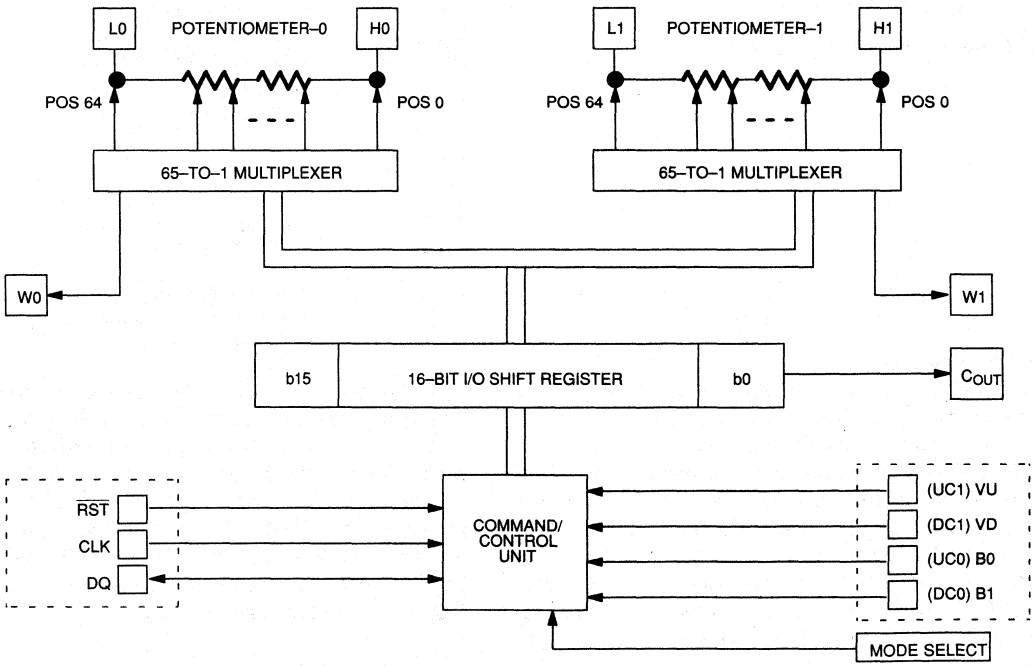
The MODE input is used for contact closure operation. This input allows the user to choose between independent mode control and stereo mode control. The MODE input is discussed in detail under the contact closure interface control.

On power–up the serial port is stable and active within 10 microseconds. The contact closure control interface inputs are active after 50 ms. The wiper position on power–up will be at position 63, the low end of the potentiometer. Position 64 is the mute level.

RESISTANCE CHARACTERISTICS Table 1

POSITION	OUTPUT LEVEL (dB)
0	0
1	–1
2	–2
3	–3
4	–4
5	–5
•	•
•	•
•	•
63	–63
64	< –90

DS1802 BLOCK DIAGRAM Figure 1



CONTACT CLOSURE INTERFACE CONTROL

The DS1802 can be configured to operate from contact closure inputs sometimes referred to as push–button control. There exist a total of four physical contact closure terminals on the device package. When combined with the MODE input, these contact closure inputs provide a total of eight different contact closure functions. These eight contact closure functions are listed in Table 2.

CONTACT CLOSURE INPUTS Table 2

CONTACT INPUT	DESCRIPTION
UC0*	Up contact potentiometer–0
UC1*	Up contact potentiometer–1
DC0*	Down contact potentiometer–0
DC1*	Down contact potentiometer–1
VU**	Volume up
VD**	Volume down
B0**	Balance Pot–0
B1**	Balance Pot–1

* independent mode control
** stereo mode control

The MODE input terminal is used to select the mode of wiper control using contact closure. There exist two modes of wiper control which include independent mode control and stereo mode control. As shown in the pin assignment diagram, the contact closure inputs share pins. Input functionality is determined by the state of the MODE input at power–up.

Independent mode control allows the user to independently control each potentiometers wiper position. For independent mode control, the MODE input should be in a high state. For stereo mode control, the MODE input should be in a low state. The input should always be tied to a well defined logic state.

The contact closure inputs which affect independent mode control include UC0, UC1, DC0, and DC1. As outlined in Table 2, the UC0 and UC1 inputs are used to move the potentiometers wipers towards the high–end of the potentiometer (H0, H1) terminals. And the DC0 and DC1 inputs control movement towards the low–end terminals (L0, L1). Note that UC0 and DC0 control potentiometer–0 wiper movement while UC1 and DC1 control potentiometer–1 movement.

An additional feature of the contact closure interface is the ability to control both directions of wiper movement with only the UC0 and UC1 contact closure inputs. This feature is referred to as single pushbutton operation. Figure 2(a) and (b) illustrates both configurations for single pushbutton and dual pushbutton operation.

Stereo Mode Control

Stereo mode control allows for the simultaneous positioning of both potentiometer wipers from a single control input. Stereo mode control is entered when the MODE select input is in a low state at power–up. The functionality available when operating in stereo mode control includes: 1) volume–up, 2) volume–down, 3) balance–0, and 4) balance–1.

Volume Control Inputs

Volume–up and volume–down allow the user to move both wipers either up or down the resistor array without changing the relative balance or distance between the wipers. For example, if potentiometer–0's wiper is set at position 28 and potentiometer–1's wiper is set at position 20, the position distance of eight is maintained when using either of these functions. Additionally, the balance between both wipers is preserved if either reaches the end of its resistor array.

Balance Control Inputs

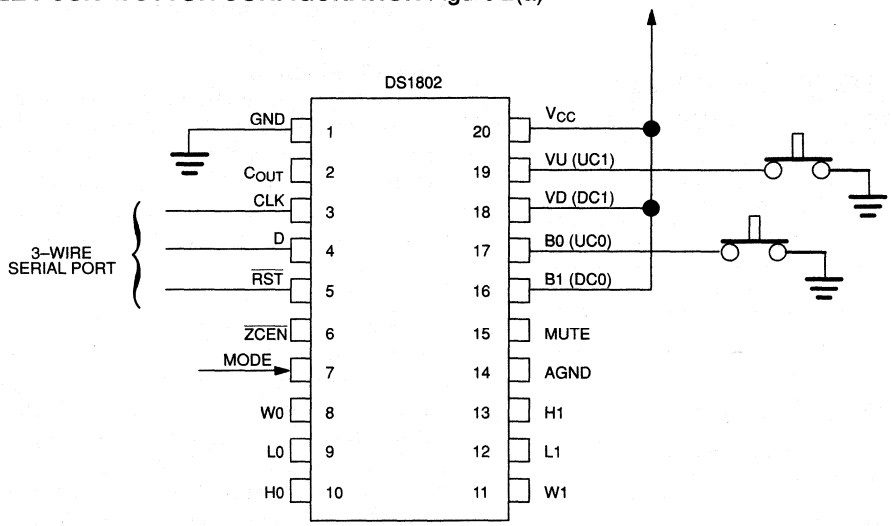
Balance control inputs allow the user to control the distance or offset between potentiometer–0 and potentiometer–1 wiper position settings. The two input controls for balance include B0 and B1. The balance control inputs attempt to maximize their respective wiper's position on the resistor array. When the DS1802 first receives a balance control input, the position of the wiper closest to the high end terminal, H_X, is stored. Wiper position movement is then governed by this stored value.

For example, if the B0 input is used, the wiper position of potentiometer–0 will change only if its position on the resistor array is less than the wiper position of potentiometer–1. The direction of movement for the potentiometer–0 wiper will be towards the high end of the resistor array. Upward movement of the wiper–0 will only stop once its value is equal to that of wiper–1. At this point, continued input activity on the B0 input will cause the wiper position of potentiometer–1 to move down its resis-

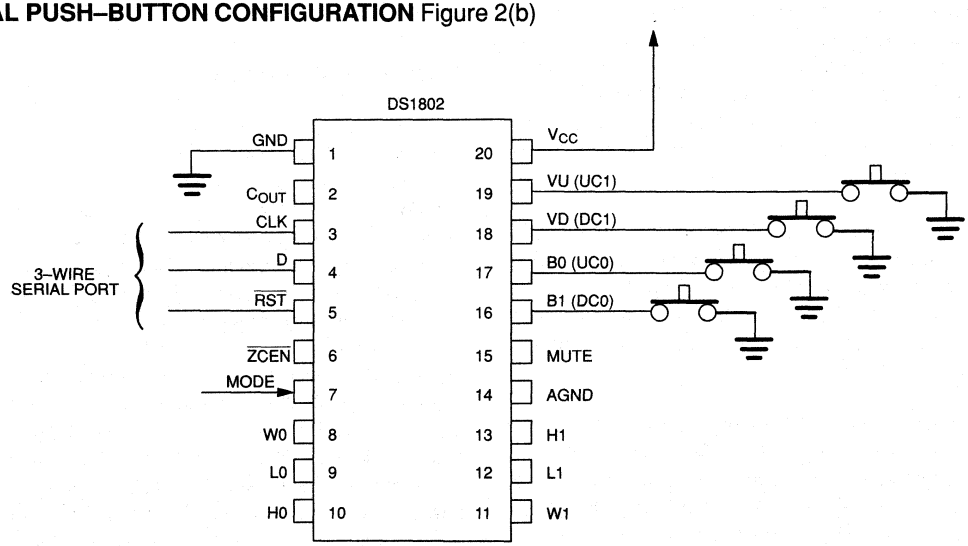
tor array. Note that if the wiper of potentiometer–1 peaks at the bottom of its array, continued B0 input activity will cause no change in the wiper positions of the device. A B1 input will be required to change the balance of the two wipers if the potentiometer wiper peaks in this case.

In the case where both wiper positions are at the bottom of their resistor arrays, no movement of the wipers will take place when using the balance controlled inputs. A volume–up control input is required to move the wiper positions from the bottom of the resistor arrays. Balance control operation is presented in Figure 3.

SINGLE PUSH–BUTTON CONFIGURATION Figure 2(a)



DUAL PUSH–BUTTON CONFIGURATION Figure 2(b)



Contact closure is defined as the transition from a high level to a low level on the contact closure input terminals. The DS1802 interprets input pulse widths as the means of controlling wiper movement. A single pulse input over the UCx or DCx input terminals will cause the wiper to move one position. A transition from high to low on these inputs is considered the beginning of pulse activity or contact closure. A single pulse is defined as being greater than 1 ms but lasting no longer than a second. This is shown is Figure 4(a).

Repetitive pulsed inputs can be used to step through each resistive position of the device in a relatively fast manner (see Figure 4(b)). The requirement for repetitive pulsed inputs is that pulses must be separated by a minimum time of 1 ms. If not, the DS1802 will interpret repetitive pulses as a single pulse.

Pulse inputs lasting longer than 1 second will cause the wiper to move one position every 100 ms following the initial 1 second hold time. The total time to transcend the entire potentiometer using a continuous input pulse is given by the formula below:

1 (second) + 63 X 100 ms =7.3 (seconds)

Single Contact Closure

Single contact closure operation allows the user to control wiper movement in either direction from a single push–button input. Figure 2(a), as mentioned, presents a typical single push–button configuration.

In independent mode control, the UC0 and UC1 inputs are used to increment and decrement each respective wiper position for single push–button mode of operation. The DC0 and DC1 inputs provide no functionality in the single push–button configuration but must be connected to the positive supply voltage (V_{CC}). In stereo mode control, the VU and B0 inputs are used to control volume and balance. The VD and B1 inputs provide no functionality in the single push–button configuration but must be connected to the positive supply voltage (V_{CC}). The 3–wire serial port inputs ($\overline{RST}$, CLK, and D) must be grounded when not used.

On device power–up, the configuration shown in Figure 2(a) must exist in order to enter the single contact closure mode of operation; especially and specifically, the (DC0, DC1, VD, and B1) input's connection to the positive supply voltage (V_{CC}).

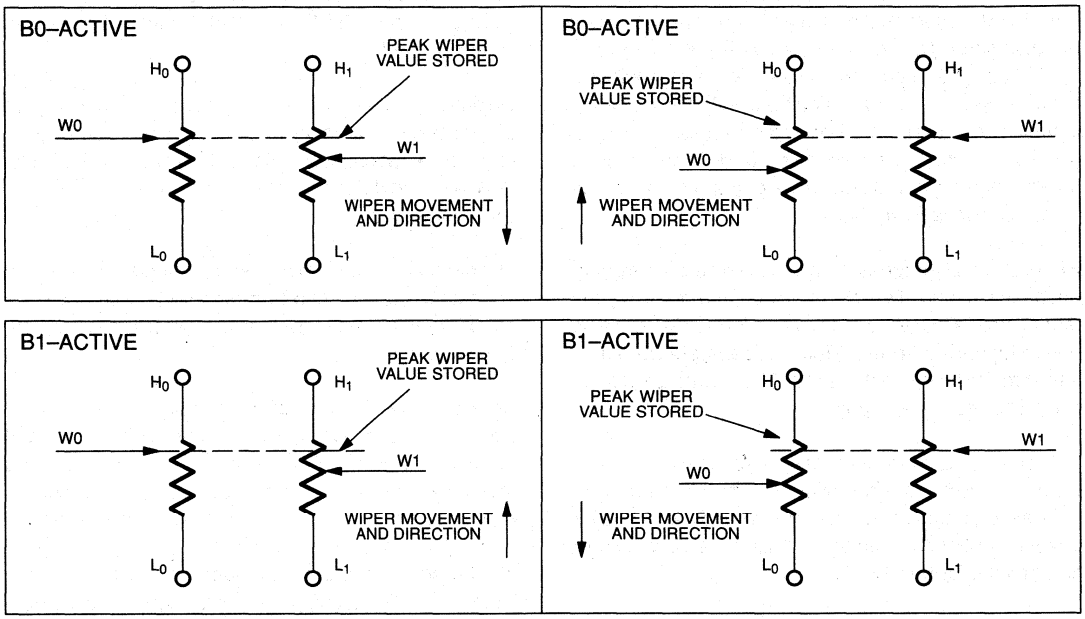
The direction of wiper movement, in single push–button operation, is determined by prior activity; with the direction of wiper movement being opposite to that of the previous activity.

Changing the direction of wiper movement in single push–button configuration is accomplish by a period of inactivity on the controlling input of a (minimum) 1 second or greater. For example, when operating from independent mode control, an inactivity of 1 second or greater on the UC0 input will cause the direction of the potentiometer–0 wiper to reverse. The same is true for the UC1 input. Also, in independent mode control and single push–button configuration, as the wiper reaches the end of the potentiometer range its direction of movement reverses. This will occur regardless if the input is a continuous pulse, a sequence of repetitive pulses or a single pulse.

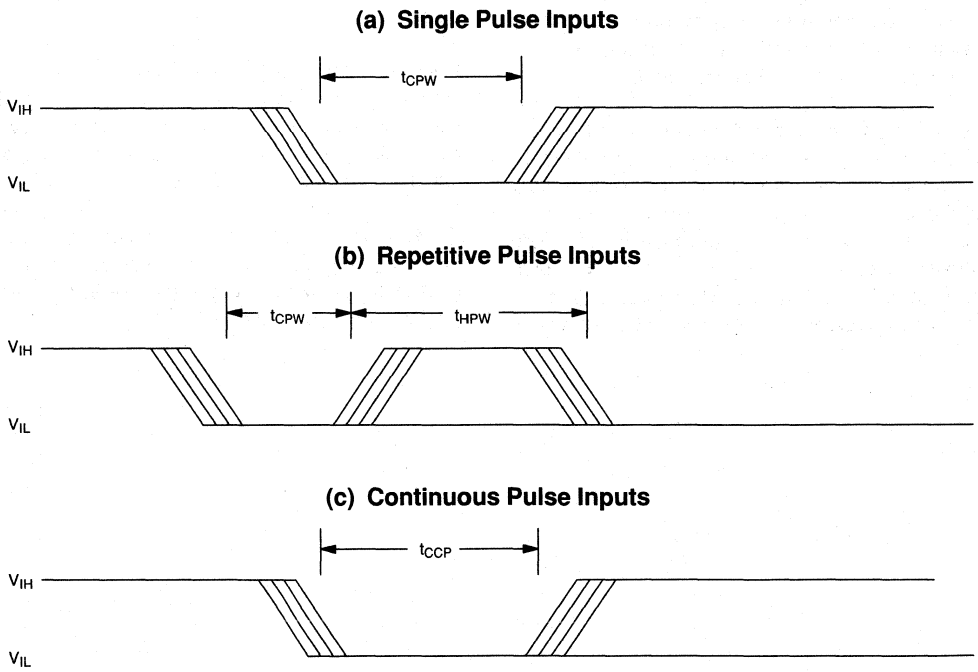
In stereo mode control, the VU input is responsible for both directions of wiper movement. Again, a period of inactivity will allow the direction of volume to be reversed. Additionally, if either wiper reaches a peak position, the direction of movement will automatically reverse.

For balance mode control, the B0 input will be responsible for wiper movement. A period of inactivity lasting 1 second or more will cause a switch in balance movement (i.e. balance–0 to balance–1).

DS1802 BALANCING EXAMPLE Figure 3



CONTACT CLOSURE TIMING (UC, DC) Figure 4



Dual Contact Closure

In dual push–button mode, each direction is controlled by the respective control inputs. No wait states are required to change wiper direction, balance, or volume in dual push–button mode. Additionally, in dual push–button mode as the wiper position reaches the end of the potentiometer, the direction of wiper movement will not change. Wiper position will remain at the potentiometers' end until an opposite direction input is given.

All contact closure control inputs, UC0, UC1, DC0, DC1, VU, VD, B0 and B1 are internally pulled–up by a 50KΩ resistance. The UC0, UC1, DC0 DC1, VU, VD, B0, and B1 inputs are internally debounced and require no external components for input signal conditioning.

3–WIRE SERIAL INTERFACE CONTROL

One method of communication and control of the DS1802 is accomplished through a 3–wire serial port interface that drives an internal control logic unit. The 3–wire serial interface is designed for microprocessor or microcontroller applications. The interface consists of three input signals which include $\overline{RST}$, CLK and D.

The $\overline{RST}$ control signal is used to enable 3–wire serial port write operations. The CLK signal terminal is a clock signal input that provides synchronization for data I/O while the D signal input serves to transfer potentiometer wiper position settings to the device.

As shown in Figure 5, a 3–wire serial port operation begins with a transition of the $\overline{RST}$ signal input to a high state. Once the 3–wire port has been activated, data is clocked into the part on the low to high transition of the CLK signal input. Data input via the D line is transferred in order of the desired potentiometer–0 value followed by the potentiometer–1 value.

The DS1802 contains two 65–position potentiometers whose wiper positions are set by an 8–bit value. These two 8–bit values are written to the 16–bit I/O shift register which is used to store wiper position during powered conditions. Because the potentiometer has 65–positions, only seven bits of data are needed to set wiper position. A detailed diagram of the 16–bit I/O shift register is shown in Figure 5. Bits 0 through 7 are reserved for the potentiometer–0 control while bits 8 through 15 are reserved for control of potentiometer–1.

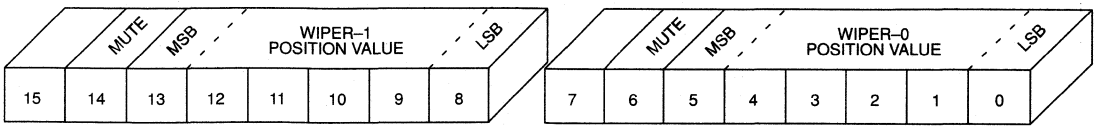
Bits 0 through 5 are used for actual wiper positioning for potentiometer–0. Bit 6 is used to mute potentiometer–0. If this bit has value "1", the potentiometer–0 wiper will be connected to the low end of the resistive array. The mute feature of the DS1802 will be discussed in the section entitled "Mute Operation of DS1802". The value of bit 7 is a don't care and will not affect operation of the DS1802 or potentiometer–0.

Bits 8 through 13 are used for wiper positioning of potentiometer–1. Bit 14 is used for muting of the potentiometer–1 wiper output. Bit 15, like bit 7, is a don't care and will not affect operation of the DS1802.

Data for the DS1802 is transmitted LSB first starting with bit 0. A complete transmission of 16 bits of data is required to insure proper setting of each potentiometer's wiper. An incomplete transmission may result in undesired wiper settings.

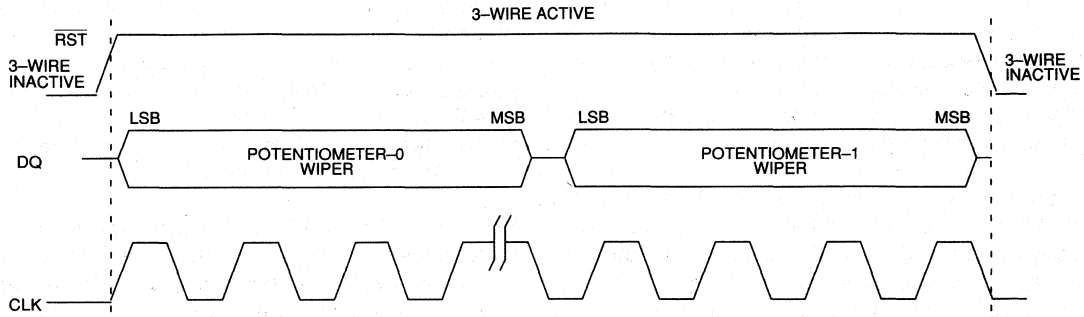
Once the complete 16 bits of information has been transmitted and the $\overline{RST}$ signal input transitions to a low state, the new wiper positions are loaded into the part.

16–BIT I/O SHIFT REGISTER Figure 5

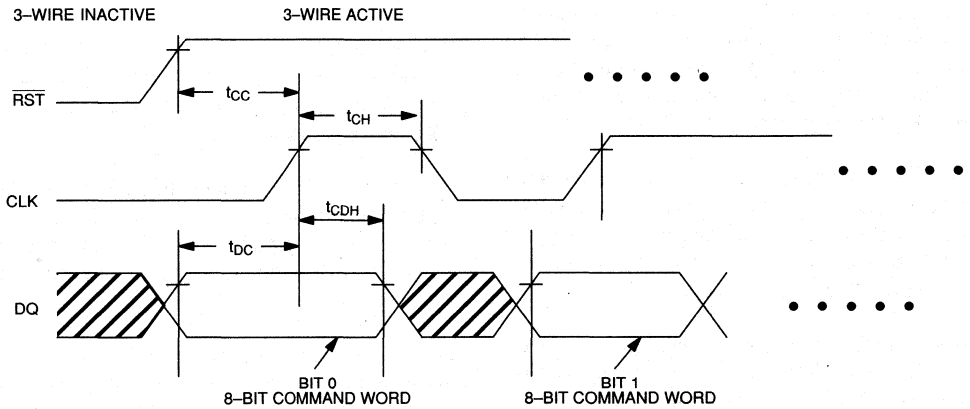


TIMING DIAGRAMS Figure 6

(a) 3–Wire Serial Interface General Overview

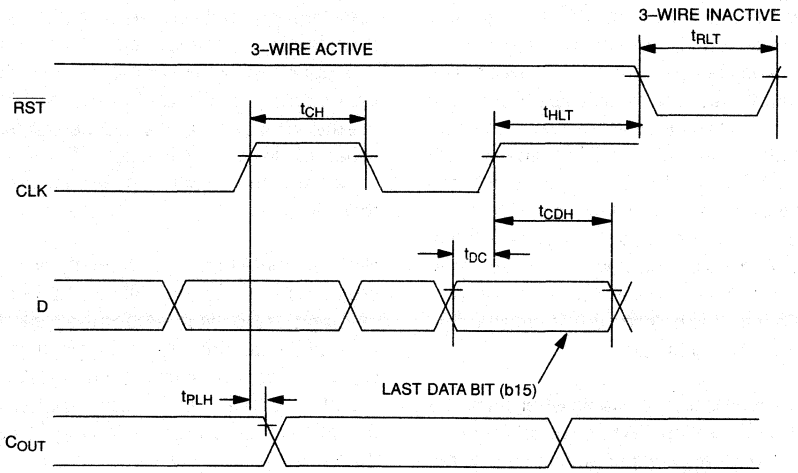


(b) Start of Communication Transaction



TIMING DIAGRAMS Figure 6 (cont'd)

(c) End of Communication Transaction



CASCADE OPERATION

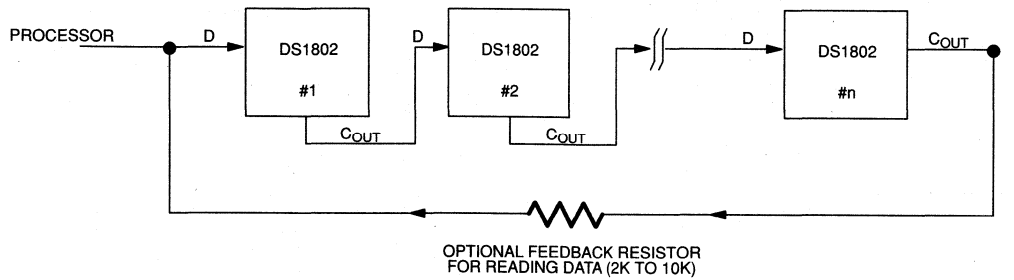
A feature of the DS1802 is the ability to control multiple devices from a single processor. Multiple DS1802s can be linked or daisy chained as shown in Figure 6. As a data bit is entered into the I/O shift register of the DS1802 it will appear at the C_{OUT} output after a maximum delay of 50 nanoseconds.

The C_{OUT} output of the DS1802 can be used to drive the D input of another DS1802. When connecting multiple devices, the total number of bits sent is always 16 times the number of DS1802s in the daisy chain.

An optional feedback resistor can be placed between the C_{OUT} terminal of the last device and the D input of the first DS1802 thus allowing the controlling processor to read, as well as write data, or circularly clock data through the daisy chain. The value of the feedback or isolation resistor should be in the range from 2K to 10K ohms.

When reading data via the C_{OUT} pin and isolation resistor, the D line is left floating by the reading device. When $\overline{RST}$ is driven high, bit 0 is present on the C_{OUT} pin, which is fed back to the input D pin through the isolation resistor. When the CLK input transitions low to high, bit 0 is loaded into the first position of the I/O shift register and bit 1 becomes present on C_{OUT} and D of the next device. After 16 bits (or 16 times the number of DS1802s in the daisy chain), the data has shifted completely around and back to its original position. When $\overline{RST}$ transitions to the low state to end data transfer, the value (the same as before the read occurred) is loaded into the wiper–0 and wiper–1.

CASCADING MULTIPLE DEVICES Figure 7



Zero Crossing Detection

The DS1802 provides a zero–crossing detection capability when using the 3–Wire Serial interface. Zero–crossing detection provides a means for minimizing any audible noise that may result from sizable discrete wiper transitions when using the part in audio applications. The zero crossing detect feature allows independent wiper changes only when the two terminals of the potentiometer have equal potentials and within a 50 ms time window from the fall of the $\overline{RST}$ signal. If at 50 ms the DS1802 has not detected a zero crossing, the wiper position of the potentiometer(s) will change regardless of the state of the input signal. Zero–crossing detection is activated when the $\overline{ZCEN}$ input level is in a low–state. When high, the $\overline{ZCEN}$ input deactivates both the 50 ms time requirement and zero–detection crossing.

Zero crossing detection is also available when using the part in push–button operation. When a pushbutton is activated, the part will change wiper position during the first detected zero–crossing or at the end of a 50 ms time window.

When operating in push–button operation with a continuous input pulse, the wiper position will change once during the initial 1 second time period. This change is dictated by a detected zero–crossing or 50 ms time window. Subsequent changes when operating with continuous input pulse occur on 100 ms time intervals and are dependent on zero crossing or 50 ms timeouts.

MUTE CONTROL

The DS1802 provides a mute control feature which can be accessed by the user through hardware or software. Hardware control of the device is achieved through the MUTE input pin. This pin is internally pulled–up through a 50KΩ resistor. When this input is driven low, the wiper outputs of both potentiometers will be internally connected to the low terminal of their respective potentiometers. This input performs as a toggle input, with the first activity on this pin connecting the wiper outputs to the low end of the resistive array on each potentiometer. The next input activity on this pin will return the wiper position to the previous state before the muting occurred. Also, if operating in pushbutton mode, mute will be deactivated if an input is received over the VU, VD, UC0, UC1, DC0, DC1 inputs. This input, like the pushbutton inputs, is internally debounced and requires no external circuitry. When the device powers up, the first activity on the mute pin will internally connect the wipers to the low end of the resistor array.

Software mute control was briefly discussed in 3–wire protocol and operation. Bits 6 and 14 of the 16–bit I/O shift register are reserved for mute control of potentiometer–0 and potentiometer–1, respectively. Unlike hardware mute control, software muting allows the user individual control of each potentiometer (i.e., potentiometer–0 and potentiometer–1 can be independently muted). Software muting of potentiometer–0 would require bit 6 to have a value of 1 while for potentiometer–1, bit 14 should have a value 1. When the user desires to release the mute of any potentiometer through software the complete 16–bit I/O shift register must be rewritten with the desired potentiometer wiper settings and bits 6 and 14 having zero value.

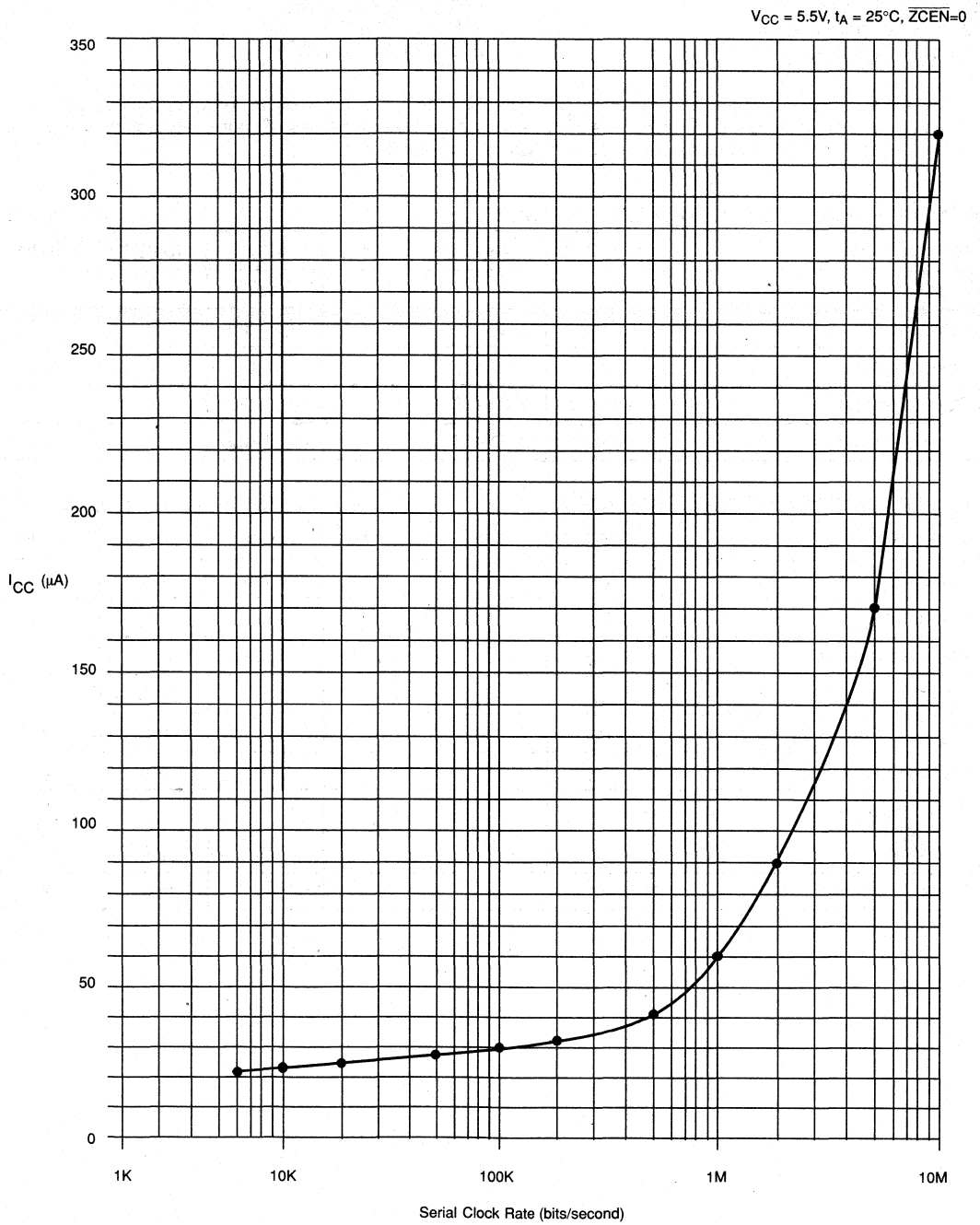
3–Wire Serial Port Vs Pushbutton Operation

In applications where both the 3–Wire Serial port and the pushbutton inputs will be used to control the part, there may exist times when activity is present on both control interfaces simultaneously. This section describes how the DS1802 handles these situations.

In all instances, the DS1802 3–Wire serial port takes precedence over pushbutton input control.

The DS1802 will allow pushbutton inputs to change wiper position during 3–Wire serial port activity.

TYPICAL SUPPLY CURRENT VS. SERIAL CLOCK RATE Figure 8



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground and AGND	–0.7V to +6.2V
Operating Temperature	0°C to 70°C commercial
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	+2.7		5.5	V	
Input Logic 1	V_{IH}	2.0		V_{CC}+0.5	V	1, 2
Input Logic 0	V_{IL}	–0.5		+0.8	V	1, 2
Resistor Inputs	L, H, W	GND–0.5		V_{CC}+0.5	V	2
Analog Ground	AGND	GND–0.5		GND +0.5	V	14

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=3V and 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}		10	2000	µA	12
Input Leakage	I_{LI}	–1		+1	µA	3
Wiper Resistance	R_W		400	1000	Ω	
Wiper Current	I_W			1	mA	
Logic 1 Output @ 2.4 Volts	I_{OH}	–1.0			mA	2
Logic 0 Output @ 0.4 Volts	I_{OL}			4	mA	2
Standby Current 3 Volts 5 Volts			10	 38	 µA µA	15
Power–Up Time	t_{PU}		50		ms	9

ANALOG RESISTOR CHARACTERISTICS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Total Resistance		40	50	60	KΩ	
Absolute Tolerance		–1		+1	dB	11, 16
Inter–ChannelMatching		–0.5		+0.5	dB	6, 16
Tap–to–Tap Tolerance		–0.25		+0.25	dB	7, 16
–3 dB Cutoff Frequency	f_{CUTOFF}		50 KHz		Hz	
TemperatureCoefficient			±800		ppm/°C	
Total Harmonic Distortion (V_{IN}=1V_{RMS}, 20 Hz to 20 KHz)	THD			0.010	%	16
Output Noise (20 Hz to 20 KHz, Grounded Input, Gain=1)					μV_{RMS}	
Digital Feedthrough (20 Hz to 20 KHz, Peak Component)				–80	dB	16
Interchannel Isolation (20 Hz to 20 KHz)			–110	–100	dB	16
Mute Control Active	Mute		–90		dB	

CAPACITANCE

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
InputCapacitance	C_{IN}			5	pF	8
OutputCapacitance	C_{OUT}			7	pF	8

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CLK Frequency	f_{CLK}	DC		10	MHz	10, 13
Width of CLK Pulse	t_{CH}	50			ns	10, 13
Data Setup Time	t_{DC}	30			ns	10, 13
Data Hold Time	t_{CDH}	10			ns	10, 13
Propagation Delay Time Low to High Level Clock to Output	t_{PLH}			50	ns	10, 13
Propagation Delay Time High to Low Level	t_{PLH}			50	ns	10, 13
$\overline{RST}$ High to Clock Input High	t_{CC}	50			ns	10, 13
$\overline{RST}$ Low from Clock Input High	t_{HLT}	50			ns	10, 13
CLK Rise Time	t_{CR}			50	ns	10, 13
$\overline{RST}$ Inactive	t_{RLT}	200			ns	10, 13

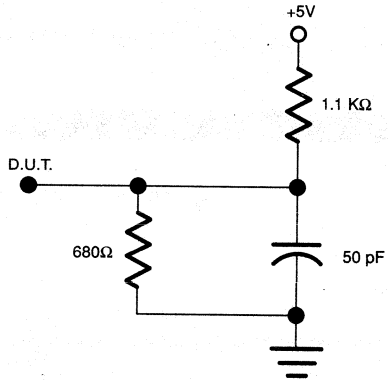
AC ELECTRICAL CHARACTERISTICS (PUSHBUTTON INPUTS) (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Single Pulse Input	t_{CPW}	1		DC	ms	3, 5, 13
Repetitive Input Pulse High Time	t_{HPW}	1		DC	ms	3, 5, 13
Continuous Input Pulse	t_{CCP}	1		DC	s	3, 5, 13

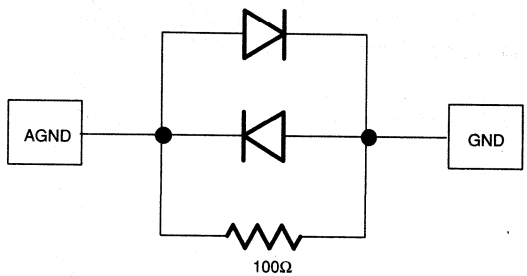
NOTES:

1. All voltages are referenced to ground.
2. Valid for V_{CC}=5V only.
3. Both UCx and DCx inputs are internally pulled up with a 50KΩ resistance.
4. Capacitance values apply at 25°C.
5. Input pulse width is the minimum time required for an input to cause an increment or decrement. If the UCx or DCx inputs is held active for longer than 1 second, subsequent increments or decrements will occur on 100 ms intervals until the inputs UCx, DCx are released to V_{IH}. Timing tolerances for pushbutton control is ±30%.
6. Inter–Channel Matching is used to determine the relative voltage difference in dB between the same tap position on each potentiometer. The DS1802 is specified for ±0.5 dB inter–channel matching.
7. Tap–to–Tap tolerance is used to determine the change in voltage between successive tap positions. The DS1802 is specified for ±0.25 dB tap–to–tap tolerance.
8. Typical values are for t_A=25°C and nominal supply voltage.
9. Power–up time is the time for all pushbutton inputs to be stable and active once power has reached a valid level, 2.7V min.
10. See Figure 6.
11. Absolute tolerance is used to determine measured wiper voltage vs. expected wiper voltage as determined by wiper position. The DS1802 is bounded by a ±1 dB absolute tolerance.
12. Maximum current specifications are based on clock rate, active zero–crossing detection, and push–button activation. See Figure 8 for clock rate vs. current specification.
13. Valid for V_{CC}=3V or 5V.
14. See Figure 10.
15. Standby current levels apply when all inputs are driven to appropriate supply levels.
16. These parameters are characterized and not 100% tested.

DIGITAL OUTPUT LOAD Figure 9



INTERNAL GROUND CONNECTIONS Figure 10



NOTE: GND and AGND must be tied to the same voltage level.

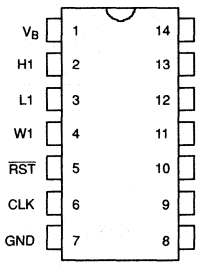
DALLAS SEMICONDUCTOR

DS1867
Dual Digital Potentiometer with EEPROM

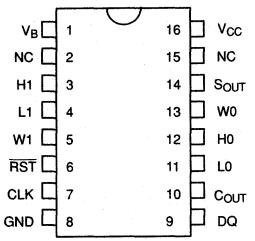
FEATURES

- Nonvolatile version of the popular DS1267
- Low power consumption, quiet, pumpless design
- Operates from single 5V or ±5V supplies
- Two digitally controlled, 256–position potentiometers
- Wiper position is maintained in the absence of power
- Serial port provides means for setting and reading both potentiometers
- Resistors can be connected in series to provide increased total resistance
- 16–pin SOIC and 20–pin TSSOP for surface mount applications
- Standard resistance values:
  - DS1867–10 ~ 10KΩ
  - DS1867–50 ~ 50KΩ
  - DS1867–100 ~ 100KΩ
- Temperature:
  - Commercial: 0°C to 70°C
  - Industrial: –40°C to +85°C

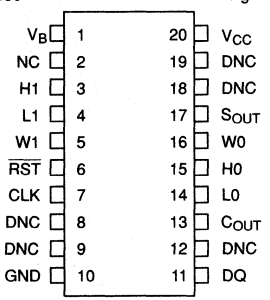
PIN ASSIGNMENT



14–PIN DIP (300 MIL)
See Mech. Drawing
Pg. 480



16–PIN SOIC (300 MIL)
See Mech. Drawing
Pg. 484



20–PIN TSSOP (173 MIL)
See Mech. Drawing
Pg. 485

DESCRIPTION

The DS1867 is the nonvolatile version of the popular DS1267 Dual Digital Potentiometer. The DS1867 consists of two digitally controlled potentiometers having 256–position wiper settings. Wiper position is maintained in the absence of power through the use of EEPROM memory cell arrays. Communication and control of the device is accomplished over a 3–wire serial port which allows reads and writes of the wiper position. Both potentiometers can be stacked for increased total resistance with the same resolution. For multiple device–single processor environments, the DS1867 can be cascaded for control over a single 3–wire bus. The DS1867 is offered in three standard resistance values and commercial and industrial temperature versions.

PIN DESCRIPTION

L0, L1	–	Low End of Resistor
H0, H1	–	High End of Resistor
W1, W2	–	Wiper End of Resistor
V_B	–	Substrate Bias
S_{OUT}	–	Wiper for Stacked Configuration
$\overline{RST}$	–	Serial Port Reset Input
DQ	–	Serial Port Data Input
CLK	–	Serial Port Clock Input
C_{OUT}	–	Cascade Serial Port Output
V_{CC}	–	+5 Volt Supply Input
GND	–	Ground
NC	–	No Internal Connection
DNC	–	Do Not Connect

OPERATION

The DS1867 contains two 256–position potentiometers whose wiper positions are set by an 8–bit value. These two 8–bit values are written to a 17–bit I/O shift register which is used to store wiper position and the stack select bit when the device is powered. An additional memory area, the shadow memory, stores the 17–bit I/O shift register during a power–down sequence which provides for wiper nonvolatility. A block diagram of the DS1867 is presented in Figure 1.

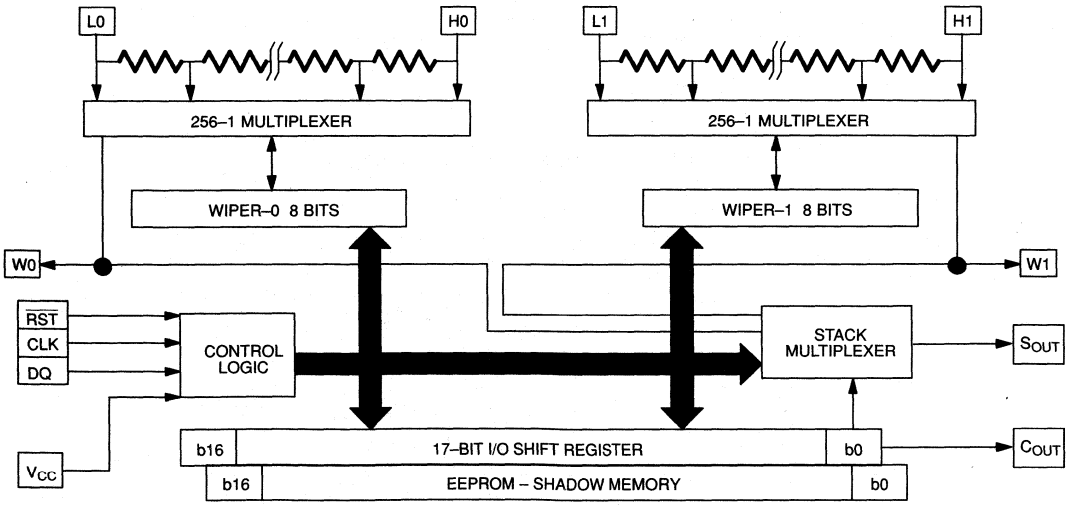
Communication and control of the DS1867 is accomplished through a 3–wire serial port interface that drives an internal control logic unit. The 3–wire serial interface consists of the three input signals: $\overline{RST}$, CLK, and DQ.

The $\overline{RST}$ control signal is used to enable 3–wire serial port operation of the device. The $\overline{RST}$ signal is an active high input and is required to begin any communication to the DS1867. The CLK signal input is used to provide timing synchronization for data input and output. The DQ signal line is used to transmit potentiometer wiper settings and the stack select bit configuration to the 17–bit I/O shift register of the DS1867.

Figure 2(a) presents the 3–wire serial port protocol. As shown, the 3–wire port is inactive when the $\overline{RST}$ signal input is low. Communication with the DS1867 requires the transistion of the $\overline{RST}$ input from a low state to a high state. Once the 3–wire port has been activated, data is latched into the part on the low to high transition of the CLK signal input. Three–wire serial timing requirements are provided in the timing diagrams of Figure 2(b) and (c).

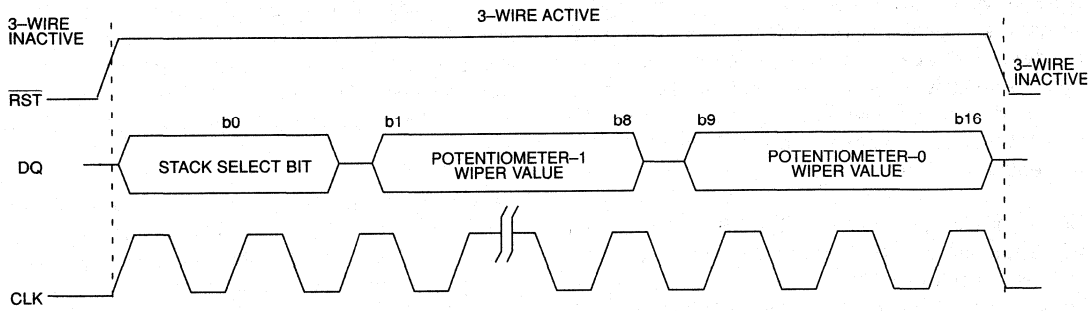
Data written to the DS1867 over the 3–wire serial interface is stored in the 17–bit I/O shift register (see Figure 2). The 17–bit I/O shift register contains both 8–bit potentiometer wiper position values and the stack select bit. The composition of the I/O shift register is presented in Figure 2. Bit 0 of the I/O shift register contains the stack select bit. This bit will be discussed in the section entitled Stacked Configuration. Bits 1 through 8 of the I/O shift register contain the potentiometer–1 wiper position value. Bit 1 will contain the MSB of the wiper setting for potentiometer–1 and bit 8 the LSB for the wiper setting. Bits 9 through 16 of the I/O shift register contain the value of the potentiometer–0 wiper position with the MSB for the wiper position occupying bit 9 and the LSB bit 16.

DS1867 BLOCK DIAGRAM Figure 1

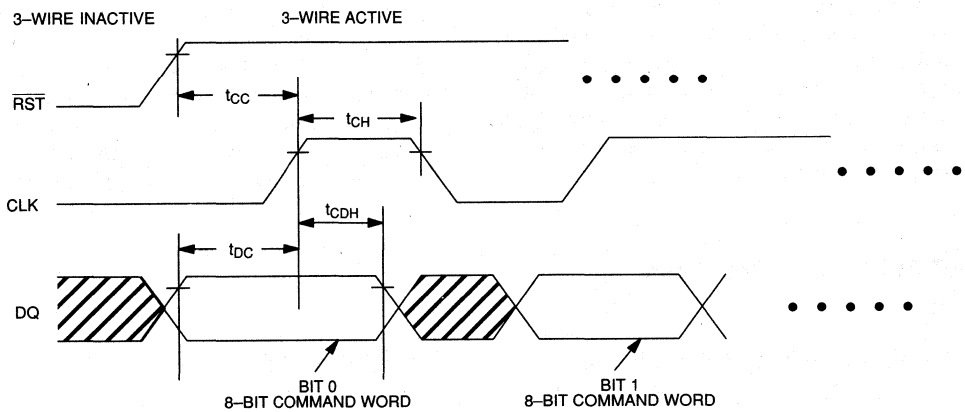


TIMING DIAGRAMS Figure 2

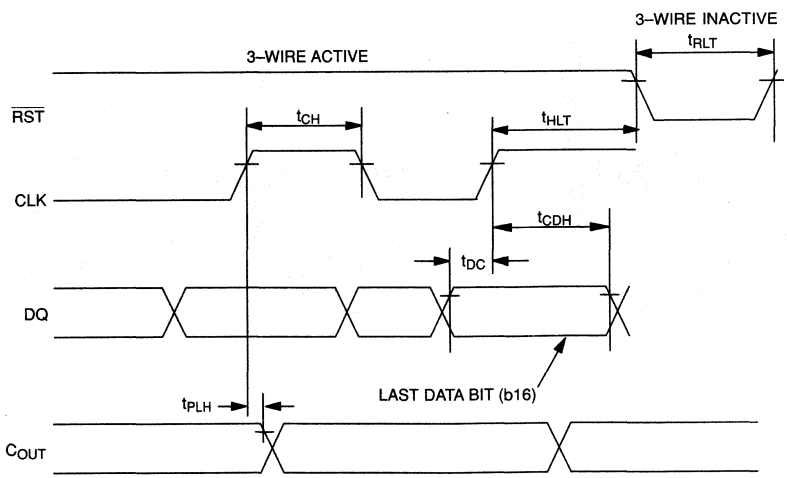
(a) 3–Wire Serial Interface General Overview



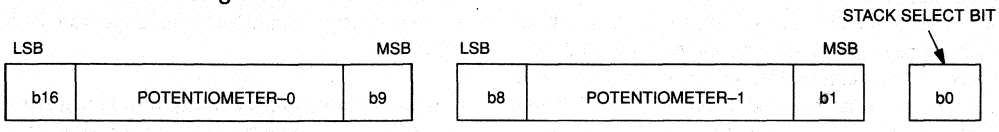
(b) Start of Communication Transaction



(c) End of Communication Transaction



I/O SHIFT REGISTER Figure 3



17–BIT I/O SHIFT REGISTER

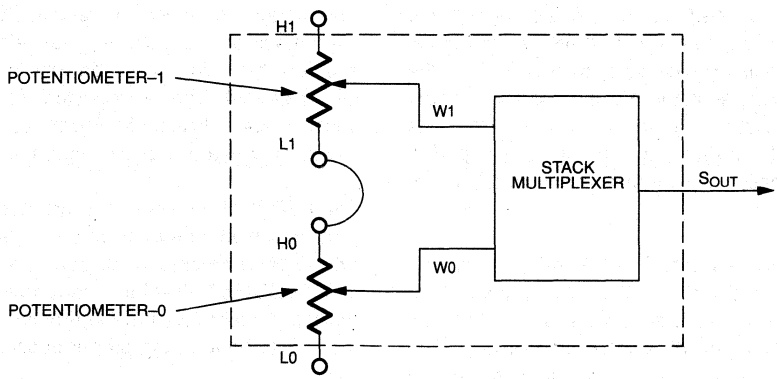
Transmission of data always begins with the stack select bit followed by the potentiometer–1 wiper position value and lastly the potentiometer–0 wiper position value (see Figure 2(a)).

When wiper position data is to be written to the DS1867, 17 bits (or some integer multiple) of data should always be transmitted. Transactions which do not send a complete 17 bits (or multiple) will leave the register incomplete and possibly an error in desired wiper position. After a communication transaction has been completed the $\overline{RST}$ signal input should be taken to a low state to prevent any inadvertent changes to the device shift register. Once $\overline{RST}$ has reached a low state, the contents of the I/O shift register are loaded into the respective multiplexers for setting wiper position. A new wiper position will only engage pending a $\overline{RST}$ transition to the low state.

STACKED CONFIGURATION

The potentiometers of the DS1867 can be connected in series as shown in Figure 3. This is referred to as the stacked configuration and allows the user to double the total end–to–end resistance of the part. The resolution of the combined potentiometers will remain the same as a single potentiometer but with a total of 512 wiper positions available. Device resolution is defined as $R_{TOT}/256$ (per potentiometer); where R_{TOT} is equal to the device resistance value. The wiper output for the combined stacked potentiometer will be taken at the Sout pin, which is the multiplexed output of the wiper of potentiometer–0 (W0) or potentiometer–1 (W1). The potentiometer wiper selected at the Sout output is governed by the setting of the stack select bit (bit–0) of the 17–bit I/O shift register. If the stack select bit has value 0, the multiplexed output, Sout, will be that of the potentiometer–0 wiper. If the stack select bit has value 1, the multiplexed output, Sout, will be that of the potentiometer–1 wiper.

STACKED CONFIGURATION Figure 4



CASCADE OPERATION

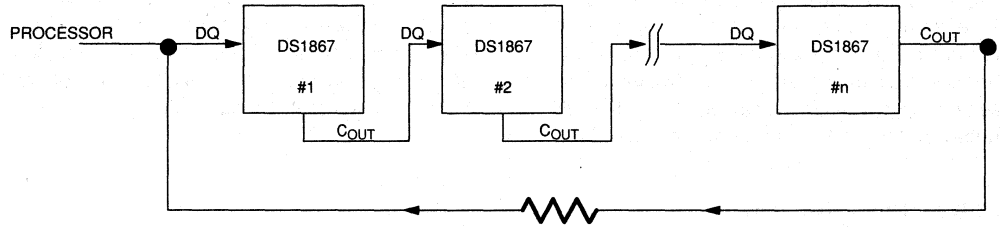
A feature of the DS1867 is the ability to control multiple devices from a single processor. Multiple DS1867s can be linked or daisy chained as shown in Figure 4. As a data bit is entered into the I/O shift register of the DS1867 it will appear at the Cout output after a maximum delay of 70 nanoseconds.

The Cout output of the DS1867 can be used to drive the DQ input of another DS1867. When connecting multiple devices, the total number of bits sent is always 17 times the number of DS1867s in the daisy chain.

An optional feedback resistor can be placed between the Cout terminal of the last device and the DQ input of the first DS1867, thus allowing the controlling processor to read, as well as, write data or circularly clock data through the daisy chain. The value of the feedback or isolation resistor should be in the range from 2K to 10K ohms.

When reading data via the Cout pin and isolation resistor, the DQ line is left floating by the reading device. When $\overline{RST}$ is driven high, bit 17 is present on the Cout pin, which is fed back to the input DQ pin through the isolation resistor. When the CLK input transitions low to high, bit 17 is loaded into the first position of the I/O shift register and bit 16 becomes present on Cout and DQ of the next device. After 17 bits (or 17 times the number of DS1867s in the daisy chain), the data has shifted completely around and back to its original position. When $\overline{RST}$ transitions to the low state to end data transfer, the value (the same as before the read occurred) is loaded into the wiper–0, wiper–1, and stack select bit I/O register.

CASCADING MULTIPLE DEVICES Figure 5



OPTIONAL FEEDBACK RESISTOR
FOR READING DATA (2K TO 10K)

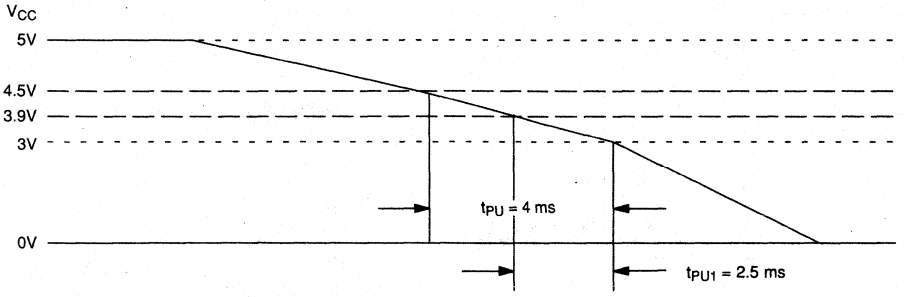
NONVOLATILE WIPER SETTINGS

The DS1867 maintains the position of the wiper in the absence of power. This feature is provided through the use of EEPROM type memory cell arrays. During normal operation, the position of the wiper is determined by the device multiplexers and stored in the shadow memory (EEPROM). The manner in which an update occurs has been optimized for reliability, durability, and performance. Additionally, the update operation is totally transparent to the user.

When power is applied to the DS1867, wiper settings will be the last recorded in the EEPROM memory cells or shadow memory before the last power–down. Changes to the EEPROM memory cells occur during a predefined power–down sequence. If the DS1867 detects a voltage transistion to 4.5 volts or less, on the power supply input, the part initiates an automatic wiper storage sequence. This storage sequence will save in EEPROM memory the contents of the I/O shift register before a total power–shutdown; provided specific power–down timing requirements are met. The minimum total power down time is specified at 4 milliseconds. Power–down timing requirements on V_{CC} are shown in Figure 6.

The EEPROM memory cells are specified to accept greater than 50,000 writes before a wear–out condition. If the EEPROM memory cells do reach a wear–out condition, the DS1867 will still function properly while power is applied. A minimum time of 4 ms between 4.5V and 3V is required to perform the proper position storage of the wiper.

POWER–DOWN EEPROM TIMING REQUIREMENTS Figure 6



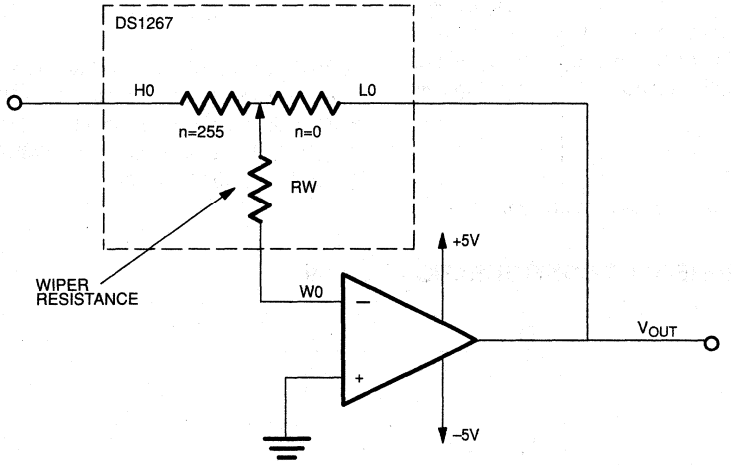
TYPICAL APPLICATION CONFIGURATIONS

Figures 7 and 8 show two typical application configurations for the DS1867. By connecting the wiper terminal of the part to a high impedance load, the effects of the wiper resistance is minimized, since the wiper resistance can vary from 400 to 1000 ohms depending on wiper voltage. Figure 7 presents the device connected in an inverting varible gain amplifier. The gain of the circuit on Figure 7 is given by the following equation:

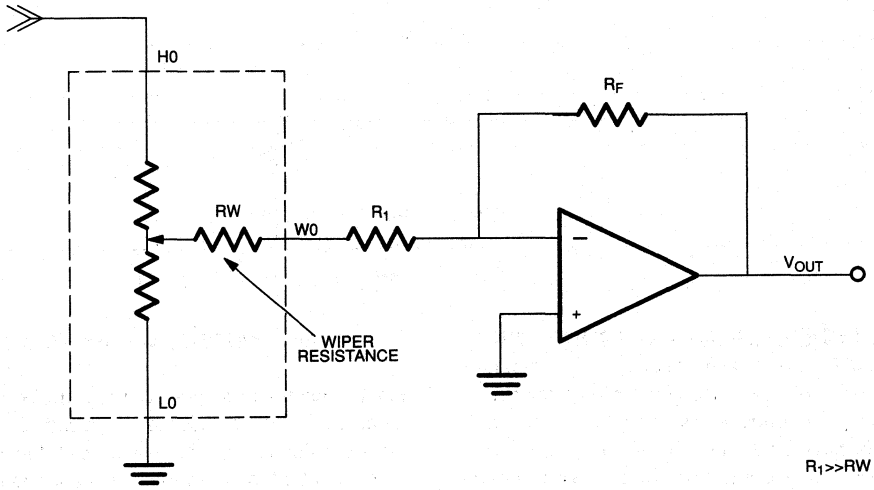
Av = –n/(255–n); where n = 0 to 255

Figure 8 shows the deivce operaing in a fixed gain attenuator where the potentiometer is used to attenuate an incoming signal. Note the resistance R1 is chosen to be much greater than the wiper resistance to minimize its effect on circuit gain.

INVERTING VARIABLE GAIN AMPLIFIER Figure 7



FIXED GAIN ATTENUATOR Figure 8



ABSOLUTE AND RELATIVE LINEARITY

Absolute linearity is defined as the difference between the actual measured output voltage and the expected output voltage. Figure 5 presents the test circuit used to measure absolute linearity. Absolute linearity is given in terms of a minimum increment or expected output when the wiper position is moved one position. In the case of the test circuit, a minimum increment (MI) would equal 10/512 volts. The equation for absolute linearity is given in equation (1).

Eq: (1) Absolute Linearity

$$AL = \{Vo(actual) - Vo(expected)\}/MI$$

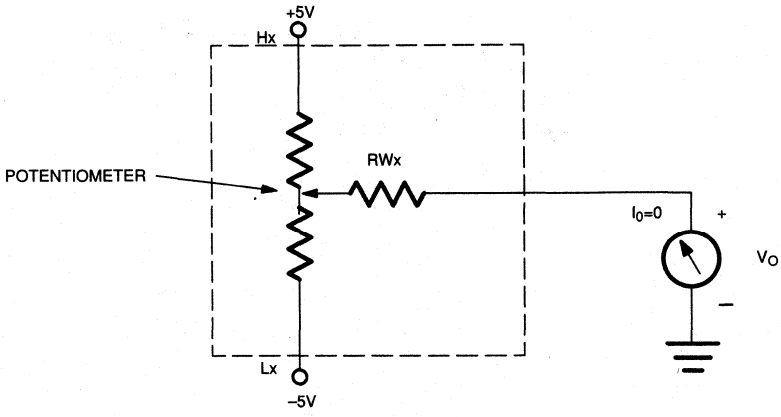
Relative Linearity is a measure of error between two adjacent wiper position points and is given in terms of MI by equation (2).

Eq: (2) Relative Linearity

$$RL = \{Vo(n+1) - Vo(n)\}/MI$$

Figure 10 is a plot of absolute linearity and relative linearity versus wiper position for the DS1867 at 25°C. The specification for absolute linearity of the DS1867 is ±0.75 MI typical. The specification for relative linearity of the DS1867 is ±0.30 MI typical.

LINEARITY MEASUREMENT CONFIGURATION Figure 9



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground (V_B=GND)	–1.0V to +7.0V
Voltage on Resistor Pins when V_B=–5.5V	–5.5V to +7.0V
Operating Temperature	0°C to 70°C commercial; –40°C to +85°C industrial
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5		5.0	V	
Input Logic 1	V_{IH}	2.0		V_{CC}+0.5	V	1, 2
Input Logic 0	V_{IL}	–0.5		+0.8	V	1, 2
Substrate Bias	V_B	–5.5		GND	V	
Resistor Inputs	L, H, W	V_B		V_{CC}+0.5	V	2

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}		250	900	µA	
Input Leakage	I_{LI}	–1		+1	µA	
Wiper Resistance	R_W		400	1000	Ω	
Wiper Current	I_W			1	mA	
Logic 1 Output @ 2.4 Volts	I_{OH}	–1.0			mA	8
Logic 0 Output @ 0.4 Volts	I_{OL}			4	mA	8
Standby Current	I_{STBY}		250		µA	
Power–Down Time	t_{PU} t_{PU1}	4 2.5			ms ms	9 10
Power Trip Point		3.9	4.2	4.5	V	
Recovery Time	t_{REC}	2	5	10	ms	11, 14

ANALOG RESISTOR CHARACTERISTICS

(–40°C to +85°C; V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
End–to–End Resistor Tolerance		–20		+20	%	
Absolute Linearity			±0.75		LSB	4
Relative Linearity			±0.30		LSB	5
–3 dB Cutoff Frequency	f_{CUTOFF}				Hz	7
Noise Figure			120		dB/(Hz)1/2	
Temperature Coefficient			+800		ppm/°C	

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	3, 6
Output Capacitance	C_{OUT}			7	pF	3, 6

AC ELECTRICAL CHARACTERISTICS

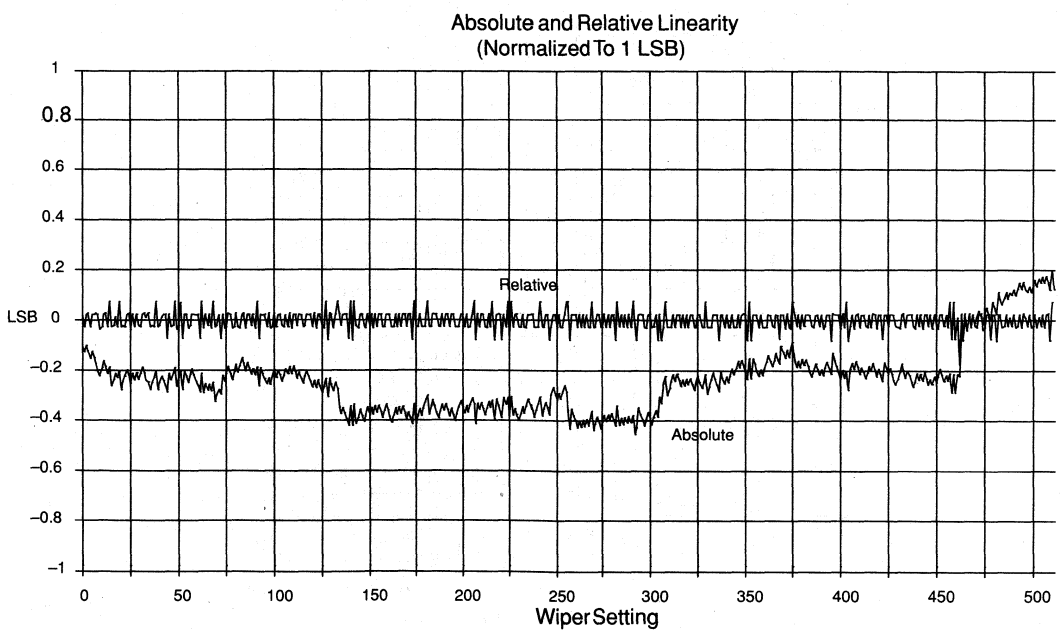
(–40°C to +85°C; V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CLK Frequency	f_{CLK}	DC		10	MHz	15
Width of CLK Pulse	t_{CH}	50			ns	15
Data Setup Time	t_{DC}	30			ns	15
Data Hold Time	t_{CDH}	10			ns	15
Propagation Delay Time Low to High Level Clock to Output	t_{PLH}			70	ns	13, 15
Propagation Delay Time High to Low Level Clock to Output	t_{PHL}			70	ns	13, 15
$\overline{RST}$ High to Clock Input High	t_{CC}	50			ns	15
$\overline{RST}$ Low from Clock Input High	t_{HLT}	50			ns	15
CLK Rise Time	t_{CR}			50	ns	15
$\overline{RST}$ Inactive Time	t_{RLT}	200			ns	15

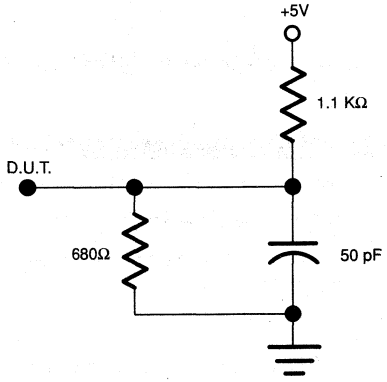
NOTES:

1. All voltages are referenced to ground.
2. Resistor inputs cannot exceed the substrate bias voltage, V_B, in the negative direction.
3. Capacitance values apply at 25°C.
4. Absolute linearity is used to determine wiper voltage versus expected voltage as determined by wiper position.
5. Relative linearity is used to determine the change in voltage between successive tap positions.
6. Typical values are for t_A=25°C and nominal supply voltage.
7. –3 dB cuttof frequency characteristics for the DS1867 depend on potentiometer total resistance: DS1867–010; 1 MHz, DS1867–050; 200 KHz, DS1867–100; 100 KHz.
8. C_{OUT} is active regardless of the state of $\overline{RST}$.
9. Power–down time is specified at a minimum of 4 ms. It is the time required for the DS1867 to guarantee wiper position storage as V_{CC} moves from 4.5V to 3.0V.
10. This is the time from power trip point min (3.9V) to 3.0V to guarantee wiper storage.
11. t_{REC} is the time required before the DS1867 stored wiper position becomes valid on power–up.
12. Power trip points reference required voltage necessary for DS1867 to restore the stored wiper position setting.
13. See Figure 11.
14. During power up the wiper position will be set at 80H.
15. See Figure 3.

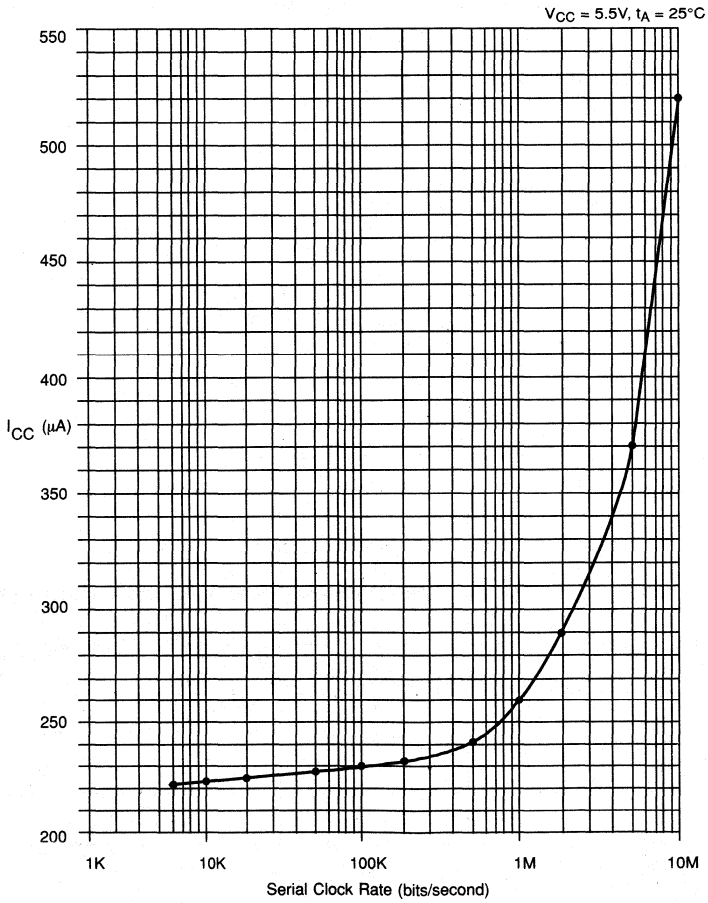
ABSOLUTE AND RELATIVE LINEARITY Figure 10



DIGITAL OUTPUT LOAD SCHEMATIC Figure 11



TYPICAL SUPPLY CURRENT VS. SERIAL CLOCK RATE Figure 12



DALLAS SEMICONDUCTOR

DS1868
Dual Digital Potentiometer Chip

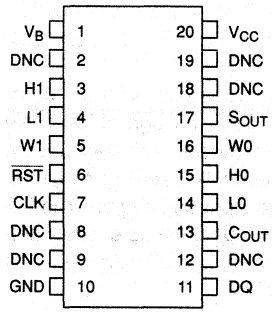
FEATURES
- Ultra–low power consumption, quiet, pumpless design
- Two digitally controlled, 256–position potentiometers
- Serial port provides means for setting and reading both potentiometers
- Resistors can be connected in series to provide increased total resistance
- 20–pin TSSOP package
- Resistive elements are temperature compensated to ±0.3 LSB relative linearity
- Standard resistance values:
  - DS1868–10 ~ 10KΩ
  - DS1868–50 ~ 50KΩ
  - DS1868–100 ~ 100KΩ
- +5V or ±3V operation
- Temperature range of 0°C to 70°C

DESCRIPTION
The DS1868 consist of two digitally controlled solid–state potentiometers. Each potentiometer is composed of 256 resistive sections. Between each resistive section and both ends of the potentiometer are tap points which are accessible to the wiper. The position of the wiper on the resistive array is set by an 8–bit value that controls which tap point is connected to the wiper output. Communication and control of the device is accomplished via a 3–wire serial port interface. This interface allows the device wiper position to be read or written.

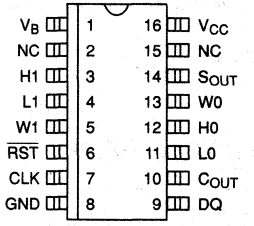
Both potentiometers can be connected in series (or stacked) for an increased total resistance with the same resolution. For multiple device–single processor environments, the DS1868 can be cascaded or daisy chained. This feature provides for control of multiple devices over a single 3–wire bus.

The DS1868 is offered in two standard resistance values which include 10K, 50K, and 100K ohm versions. The part is available in 16–pin SOIC (300 mil), 14–pin DIP, and 20–pin TSSOP packages.

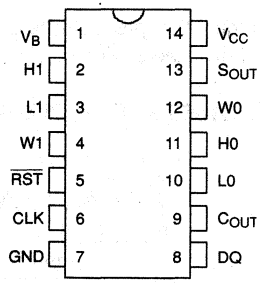
PIN ASSIGNMENT



20–Pin TSSOP (173 MIL)



DS1868S 16–Pin SOIC (300 MIL)
See Mech. Drawing
Pg. 484



14–Pin DIP (300 MIL)
See Mech. Drawing
Pg. 480

PIN DESCRIPTION

L0, L1	–	Low End of Resistor
H0, H1	–	High End of Resistor
W0, W1	–	Wiper Terminal of Resistor
S_{OUT}	–	Stacked Configuration Output
$\overline{RST}$	–	Serial Port Reset Input
DQ	–	Serial Port Data Input
CLK	–	Serial Port Clock Input
C_{OUT}	–	Cascade Port Output
V_{CC}	–	+5 Volt Supply
GND	–	Ground Connections
NC	–	No Internal Connection
V_B	–	Substrate Bias Voltage
DNC	–	Do Not Connect

*All GND pins must be connected to ground.

OPERATION

The DS1868 contains two 256–position potentiometers whose wiper positions are set by an 8–bit value. These two 8–bit values are written to a 17–bit I/O shift register which is used to store the two wiper positions and the stack select bit when the device is powered. A block diagram of the DS1868 is presented in Figure 1.

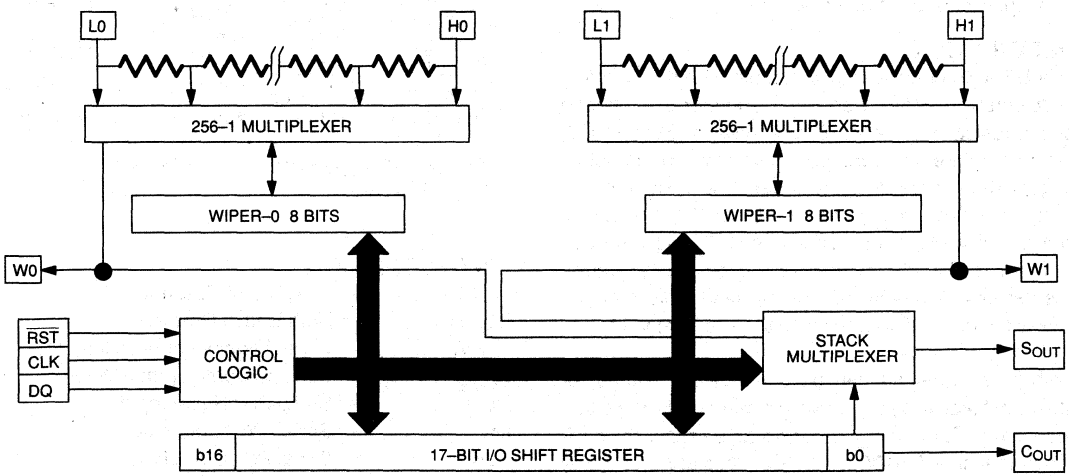
Communication and control of the DS1868 is accomplished through a 3–wire serial port interface that drives an internal control logic unit. The 3–wire serial interface consists of the three input signals: $\overline{RST}$, CLK, and DQ.

The $\overline{RST}$ control signal is used to enable the 3–wire serial port operation of the device. The $\overline{RST}$ signal is an active high input and is required to begin any communication to the DS1868. The CLK signal input is used to provide timing synchronization for data input and output. The DQ signal line is used to transmit potentiometer wiper settings and the stack select bit configuration to the 17–bit I/O shift register of the DS1868.

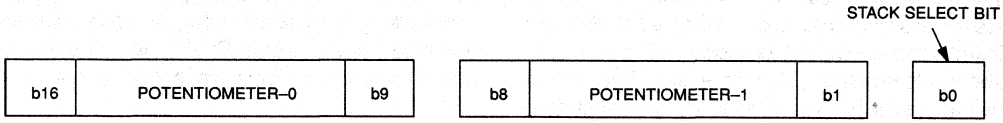
Figure 9(a) presents the 3–wire serial port protocol. As shown, the 3–wire port is inactive when the $\overline{RST}$ signal input is low. Communication with the DS1868 requires the transistion of the $\overline{RST}$ input from a low state to a high state. Once the 3–wire port has been activated, data is entered into the part on the low to high transistion of the CLK signal inputs. Three–wire serial timing requirements are provided in the timing diagrams of Figure 9(b),(c).

Data written to the DS1868 over the 3–wire serial interface is stored in the 17–bit I/O shift register (see Figure 2). The 17–bit I/O shift register contains both 8–bit potentiometerwiper position values and the stack select bit. The composition of the I/O shift register is presented in Figure 2. Bit 0 of the I/O shift register contains the stack select bit. This bit will be discussed in the section entitledStacked Configuration. Bits 1 through 8 of the I/O shift register contain the potentiometer–1 wiper position value. Bit 1 will contain the MSB of the wiper setting for potentiometer–1 and bit 8 the LSB for the wiper setting. Bits 9 through 16 of the I/O shift register contain the value of the potentiometer–0 wiper position with the MSB for the wiper position occupying bit 9 and the LSB bit 16.

DS1868 BLOCK DIAGRAM Figure 1



I/O SHIFT REGISTER Figure 2



17–BIT I/O SHIFT REGISTER

Transmission of data always begins with the stack select bit followed by the potentiometer–1 wiper position value and lastly the potentiometer–0 wiper position value.

When wiper position data is to be written to the DS1868, 17 bits (or some integer multiple) of data should always be transmitted. Transactions which do not send a complete 17–bits (or multiple) will leave the register incomplete and possibly an error in the desired wiper positions.

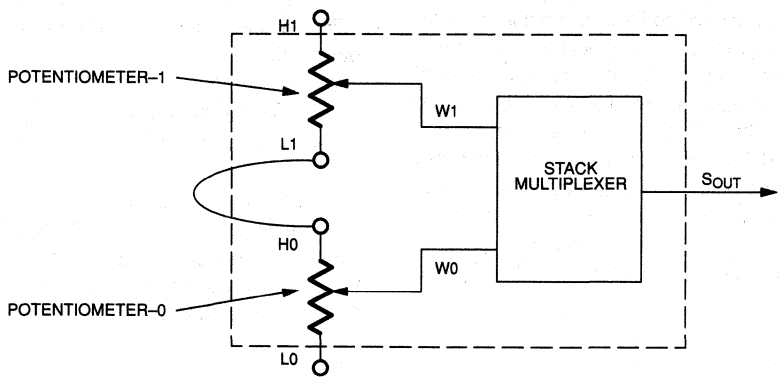
After a communication transaction has been completed the $\overline{RST}$ signal input should be taken to a low state to prevent any inadvertent changes to the device shift register. Once $\overline{RST}$ has reached a low state, the contents of the I/O shift register are loaded into the respective multiplexers for setting wiper position. A new wiper position will only engage after a $\overline{RST}$ transition to the inactive state. On device power–up, wiper position will be random.

STACKED CONFIGURATION

The potentiometers of the DS1868 can be connected in series as shown in Figure 3. This is referred to as the stacked configuration and allows the user to double the total end–to–end resistance of the part. The resolution of the combined potentiometers will remain the same as a single potentiometer but with a total of 512 wiper positions available. Device resolution is defined as $R_{TOT}/256$ (per potentiometer); where R_{TOT} equals the total potentiometer resistance.

The wiper output for the combined stacked potentiometer will be taken at the S_{OUT} pin, which is the multiplexed output of the wiper of potentiometer–0 (W0) or potentiometer–1 (W1). The potentiometer wiper selected at the S_{OUT} output is governed by the setting of the stack select bit (bit 0) of the 17–bit I/O shift register. If the stack select bit has value 0, the multiplexed output, S_{OUT}, will be that of the potentiometer–0 wiper. If the stack select bit has value 1, the multiplexed output, S_{OUT}, will be that of the potentiometer–1 wiper.

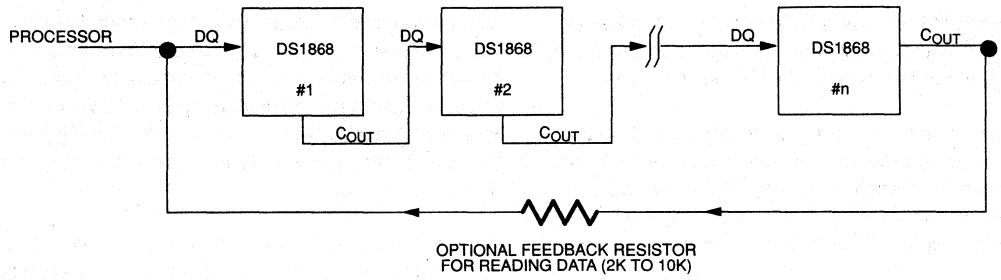
STACKED CONFIGURATION Figure 3



CASCADE OPERATION

A feature of the DS1868 is the ability to control multiple devices from a single processor. Multiple DS1868s can be linked or daisy chained as shown in Figure 4. As a data bit is entered into the I/O shift register of the DS1868 a bit will appear at the C_{OUT} output after a minimum delay of 50 nanoseconds. The stack select bit of the DS1868 will always be the first out the part at the beginning of a transaction. Additionally the C_{OUT} pin is always active regardless of the state of $\overline{RST}$. This allows one to read the I/O shift register without changing its value.

CASCADING MULTIPLE DEVICES Figure 4



The C_{OUT} output of the DS1868 can be used to drive the DQ input of another DS1868. When connecting multiple devices, the total number of bits transmitted is always 17 times the number of DS1868s in the daisy chain.

An optional feedback resistor can be placed between the C_{OUT} terminal of the last device and the first DS1868 DQ input thus allowing the controlling processor to read, as well as, write data, or circularly clock data through the daisy chain. The value of the feedback or isolation resistor should be in the range from 2K to 10K ohms.

When reading data via the C_{OUT} pin and isolation resistor, the DQ line is left floating by the reading device. When $\overline{RST}$ is driven high, bit 17 is present on the C_{OUT} pin, which is fed back to the input DQ pin through the isolation resistor. When the CLK input transitions low to high, bit 17 is loaded into the first position of the I/O shift register and bit 16 becomes present on C_{OUT} and DQ of the next device. After 17 bits (or 17 times the number of DS1868s in the daisy chain), the data has shifted completely around and back to its original position. When $\overline{RST}$ transitions to the low state to end data transfer, the value (the same as before the read occurred) is loaded into the wiper–0, wiper–1, and stack select bit I/O register.

ABSOLUTE AND RELATIVE LINEARITY

Absolute linearity is defined as the difference between the actual measured output voltage and the expected output voltage. Figure 5 presents the test circuit used to measure absolute linearity. Absolute linearity is given in terms of a minimum increment or expected output when the wiper is moved one position. In the case of the test circuit, a minimum increment (MI) or one LSB would equal 10/512 volts. The equation for absolute linearity is given as follows:

(1) ABSOLUTE LINEARITY

$$AL=\{V_O(actual) - V_O(expected)\}/MI$$

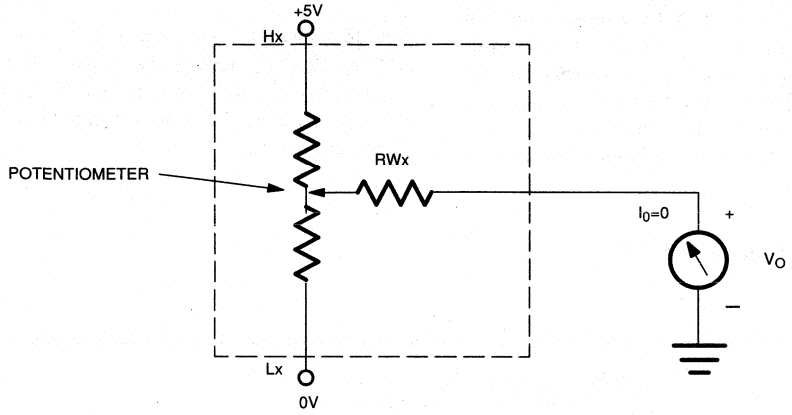
Relative Linearity is a measure of error between two adjacent wiper position points and is given in terms of MI by equation (2).

(2) RELATIVE LINEARITY

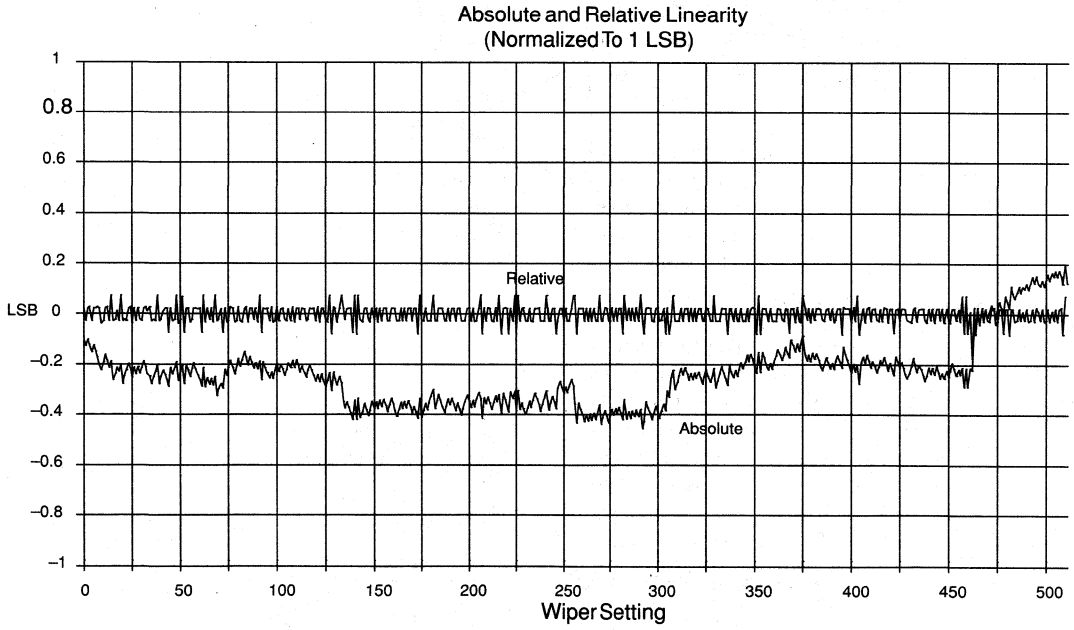
$$RL=\{V_O(n+1) - V_O(n)\}/MI$$

Figure 6 is a plot of absolute linearity and relative linearity versus wiper position for the DS1868 at 25°C. The specification for absolute linearity of the DS1868 is ±0.75 MI typical. The specification for relative linearity of the DS1868 is ±0.3 MI typical.

LINEARITY MEASUREMENT CONFIGURATION Figure 5



DS1868 ABSOLUTE AND RELATIVE LINEARITY Figure 6



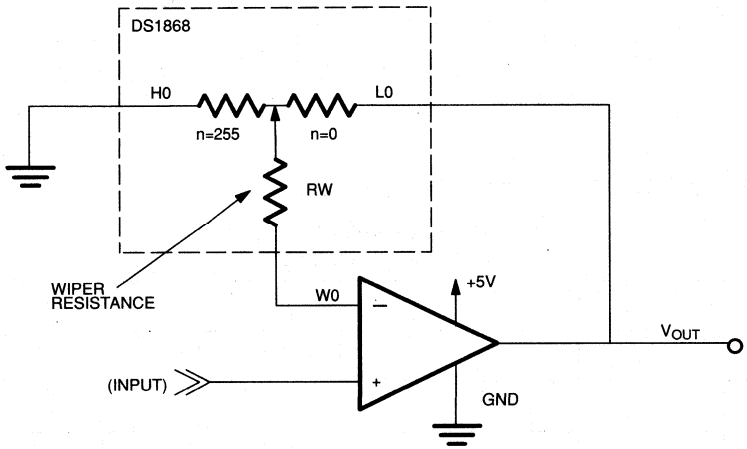
TYPICAL APPLICATION CONFIGURATIONS

Figures 7 and 8 show two typical application configurations for the DS1868. By connecting the wiper terminal of the part to a high impedance load, the effects of the wiper resistance is minimized, since the wiper resistance can vary from 400 to 1000 ohms depending on wiper voltage. Figure 7 presents the device connected in a varible gain amplifier. The gain of the circuit on Figure 7 is given by the following equation:

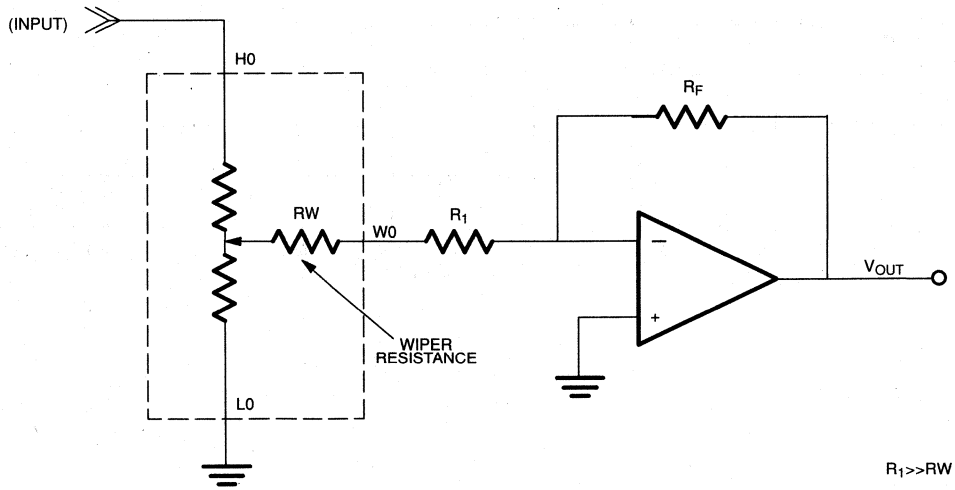
$$A_V = \frac{+256}{N+1} \quad \text{where N = 0 to 255}$$

Figure 8 shows the device operating in a fixed gain attenuator where the potentiometer is used to attenuate an incoming signal. Note the resistance R1 is chosen to be much greater than the wiper resistance to minimize its effect on circuit gain.

VARIABLE GAIN AMPLIFIER Figure 7



FIXED GAIN ATTENUATOR Figure 8



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground (V_B=GND)	–1.0V to +7.0V
Voltage on Any Pin when V_B=–3.3V	–3.3V to +4.7V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5 2.7		5.5 3.3	V	1 15
Input Logic 1	V_{IH}	2.0		V_{CC}+0.5	V	1, 2
Input Logic 0	V_{IL}	–0.5		+0.8	V	1, 2
Ground	GND	GND		GND	V	1
Resistor Inputs	L, H, W	V_B–0.5		V_{CC}+0.5	V	2, 15
Substrate Bias	V_B	–3.3		GND	V	1, 15

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}			400	µA	12
Input Leakage	I_{LI}	–1		+1	µA	
Wiper Resistance	R_W		400	1000	Ω	
Wiper Current	I_W			1	mA	
Logic 1 Output @ 2.4 Volts	I_{OH}	–1			mA	8, 9
Logic 0 Output @ 0.4 Volts	I_{OL}			4	mA	8, 9
Standby Current	I_{STBY}			1	µA	14

ANALOG RESISTOR CHARACTERISTICS

(0°C to 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
End–to–End Resistor Tolerance		–20		+20	%	
Absolute Linearity			±0.75		LSB	4
Relative Linearity			±0.3		LSB	5
–3 dB Cutoff Frequency	F_{CUTOFF}				Hz	7
Noise Figure						11
Temperature Coefficient			±800		ppm/C	

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	3, 6
Output Capacitance	C_{OUT}			7	pF	3, 6

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5.0V ± 10%)

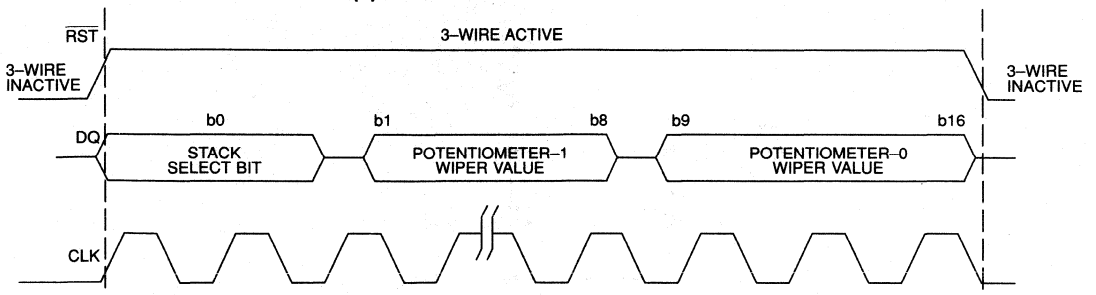
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CLK Frequency	f_{CLK}	DC		10	MHz	10
Width of CLK Pulse	t_{CH}	50			ns	10
Data Setup Time	t_{DC}	30			ns	10
Data Hold Time	t_{CDH}	10			ns	10
Propagation Delay Time Low to High Level Clock to Output	t_{PLH}			50	ns	10, 13
Propagation Delay Time High to Low Level	t_{PLH}			50	ns	10, 13
RST High to Clock Input High	t_{CC}	50			ns	10
$\overline{RST}$ Low from Clock Input High	t_{HLT}	50			ns	10
$\overline{RST}$ Inactive	t_{RLT}	125			ns	10
Clock Low to Data Valid on a Read	t_{CDD}			30	ns	10
CLK Rise Time, CLK Fall Time	t_{CR}			50	ns	10

NOTES:

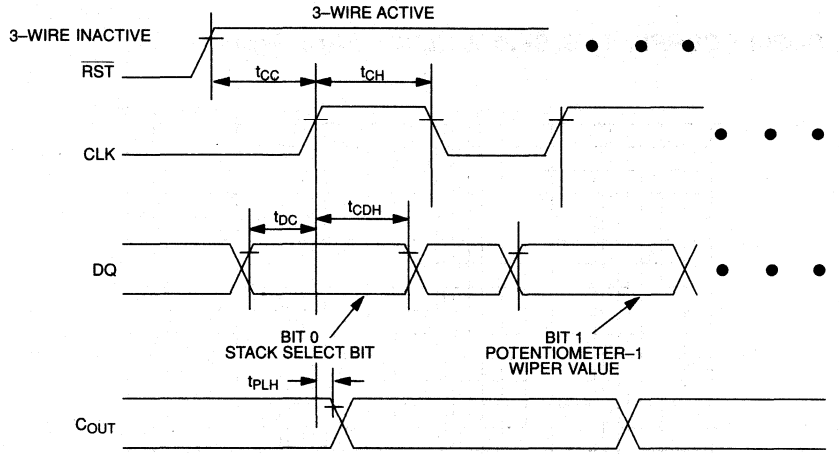
1. All voltages are referenced to ground.
2. Resistor inputs cannot exceed V_B – 0.5V in the negative direction.
3. Capacitance values apply at 25°C.
4. Absolute linearity is used to determine wiper voltage versus expected voltage as determined by wiper position. Device test limits ±1.6 LSB.
5. Relative linearity is used to determined the change in voltage between successive tap positions. Device test limits ±0.5 LSB.
6. Typical values are for t_A = 25°C and nominal supply voltage.
7. –3 dB cutoff frequency characteristics for the DS1868 depend on potentiometer total resistance: DS1868–010; 1 MHz, DS1868–050; 200 KHz; and DS1868–100; 80 KHz.
8. Cout is active regardless of the state of $\overline{RST}$.
9. V_{REF}= 1.5 volts .
10. See Figure 9(a), (b), and (c).
11. Noise < –120 dB/$\sqrt{Hz}$. Reference 1 volt (thermal).
12. Supply current is dependent on clock rate (see Figure 11).
13. See Figure 10.
14. Maximum standby current at 50°C is specified at 50 µA.
15. When biasing the substrate minimum V_B = –3.0V ± 10% and maximum V_{CC} = 3.0V ± 10%.

TIMING DIAGRAMS Figure 9

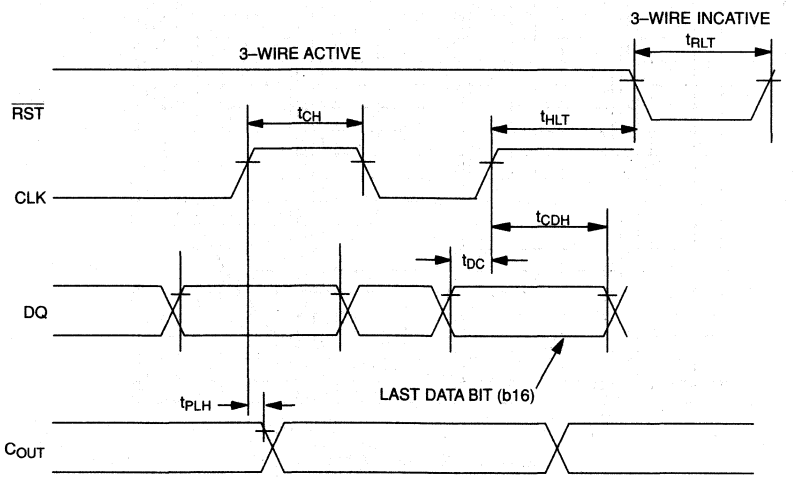
(a) 3–Wire Serial Interface General Overview



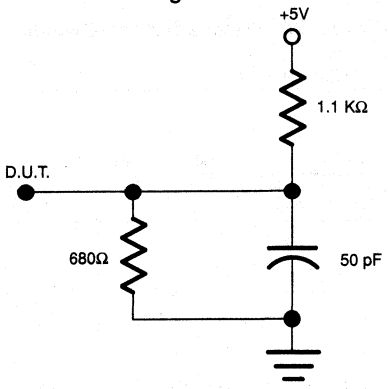
(b) Start of Communication Transaction



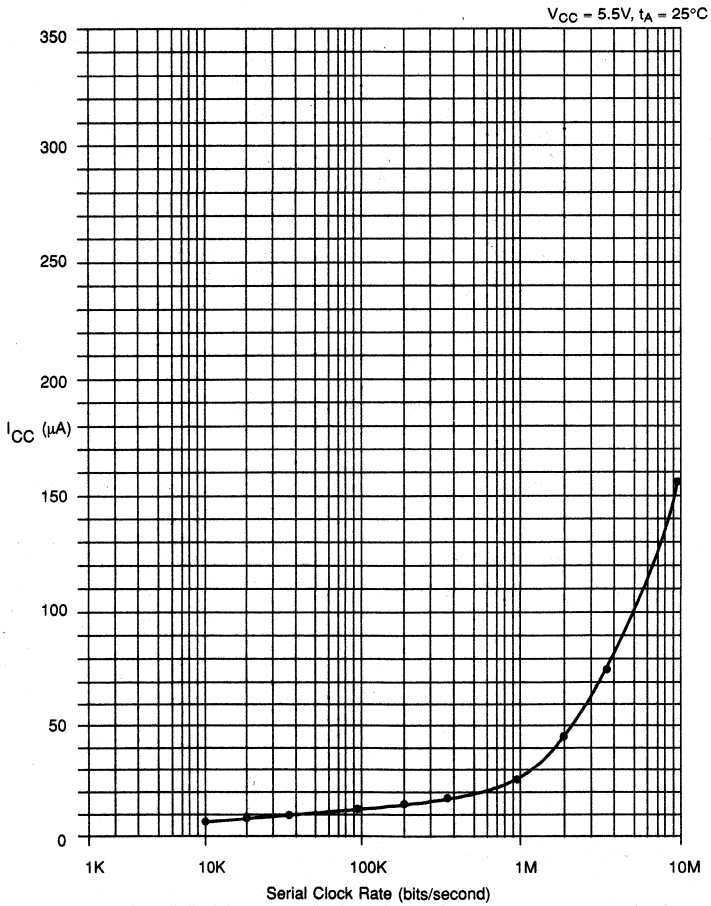
(c) End of Communication Transaction



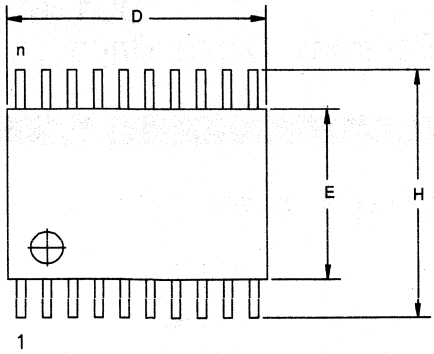
DIGITAL OUTPUT LOAD SCHEMATIC Figure 10

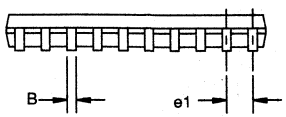


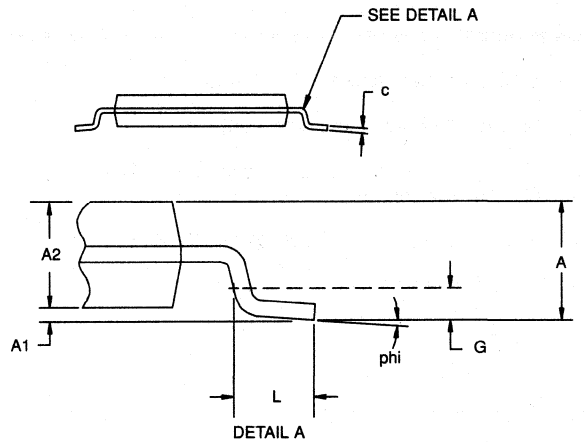
TYPICAL SUPPLY CURRENT VS. SERIAL CLOCK RATE Figure 11



DS1868 20-PIN TSSOP







DIM	MIN	MAX
A MM	–	1.10
A1 MM	0.05	–
A2 MM	0.75	1.05
C MM	0.09	0.18
L MM	0.50	0.70
e1 MM	0.65 BSC	
B MM	0.18	0.30
D MM	6.40	6.90
E MM	4.40 NOM	
G MM	0.25 REF	
H MM	6.25	6.55
phi	0°	8°

PRODUCT PREVIEW

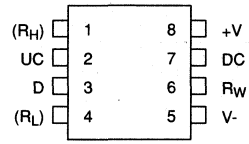
DALLAS SEMICONDUCTOR

DS1869
3V Dallastat™ Electronic Digital Rheostat

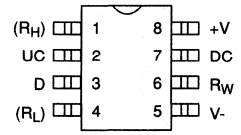
FEATURES

- Replaces mechanical variable resistors
- Operates from 3V or 5V supplies
- Electronic interface provided for digital as well as manual control
- Wiper position is maintained in the absence of power
- Low cost alternative to mechanical controls
- Applications include volume, tone, contrast, brightness, and dimmer control
- 8–pin SOIC and 8–pin DIP packages for DS1869
- Standard resistance values for Dallastat
  - DS1869–10 ~ 10KΩ
  - DS1869–50 ~ 50KΩ
  - DS1869–100 ~ 100KΩ
- Operating Temperature Range
  - Commercial: 0°C to 70°C
- 3V to 8V differential supplies operational range

PIN ASSIGNMENT DS1869



8-Pin DIP (300 Mil)
See Mech. Drawing
Pg. 480



8-Pin SOIC (200 Mil)
See Mech. Drawing
Pg. 483

PIN DESCRIPTION DS1869

R_H	-	Resistor High End (Option)
R_W	-	Resistor Wiper
R_L	-	Resistor Low End
-V, +V	-	Voltage Inputs
UC	-	Up Contact Input
D	-	Digital Input
DC	-	Down Contact Input

DESCRIPTION

The DS1869 Dallastat is a digital rheostat or potentiometer. This device provides 64 possible uniform tap points over the resistive range and is available in standard versions of 10K, 50K, and 100K ohms. The Dallastats can be controlled by either a mechanical–type contact closure input or a digital source input such as a CPU and the DS1869 operates from 3V or 5V supplies. Wiper position is maintained in the absence of power which is accomplished through the use of a EEPROM memory cell array. The EEPROM cell array is specified to accept greater than 50,000 writes.

The DS1869 is offered in two standard IC packages which include an 8–pin 300 mil DIP and an 8–pin 200 mil SOIC. The DS1869 can be configured to operate using a single pushbutton, dual pushbutton or digital source input. This is illustrated in Figure 1. The DS1869 pinouts allow access to both ends of the potentiometer RL, RH, and the wiper, RW. Control inputs include the digital source input, D, the up contact input, UC, and the down contact input, DC. Other pins include the positive,+V, and negative, –V , supply inputs. The DS1869 is available in commercial temperature versions.

OPERATION

The DS1869 can be configured to operate from a single contact closure, dual contact closure inputs or driven using a digital source input. Figures 1 and 2 illustrate both configurations, respectively. Contact closure is defined as the transition from a high level to a low level on the up contact (UC), down contact (DC), or digital source (D) inputs. These inputs are inactive when in the high state.

The DS1869 interprets input pulse widths as the means of controlling wiper movement. A single pulse input over the UC, DC, or D input terminals will cause the wiper position to move 1/64th of the total resistance. A transition from a high to low on these inputs is considered the beginning of pulse activity or contact closure. A single pulse is defined as being greater than 1 ms but lasting no longer than 1 second. This is shown is Figures 3, 4, and 5 (a).

Repetitive pulsed inputs can be used to step through each resistive position of the device in a relatively fast manner (see Figure 5b). The requirement for repetitive pulsed inputs is that pulses must be separated by a minimum time of 1 ms. If not, the DS1869 will interpret repetitive pulses as a single pulse.

Pulse inputs lasting longer 1 second will cause the wiper to move one position every 100 ms following the initial 1 second hold time. The total time to transcend the entire potentiometer using a continuous input pulse is given by the formula below:

$$\approx 1 \text{ second} + 63 \times 100 \text{ ms} = 7.3 \text{ (seconds)}$$

Single contact closure operation allows the user to control wiper movement in either direction from a single push–button input. Figure 1 presents a typical single push–button configuration. The UC input is used to increment and decrement wiper position for single push–button mode of operation. The DC input provides no functionality in this mode but must be connected to the positive supply voltage (V_{CC}). The digital source input (D) can be allowed to float.

On device power–up, the configuration shown in Figure 1 must exist in order to enter the single contact closure mode of operation; especially and specifically, the (DC) input's connection to the positive supply voltage (V_{CC}) .

The direction of wiper movement, in single push–button operation, is determined by prior activity; with the direction of wiper movement being opposite to that of the previous activity.

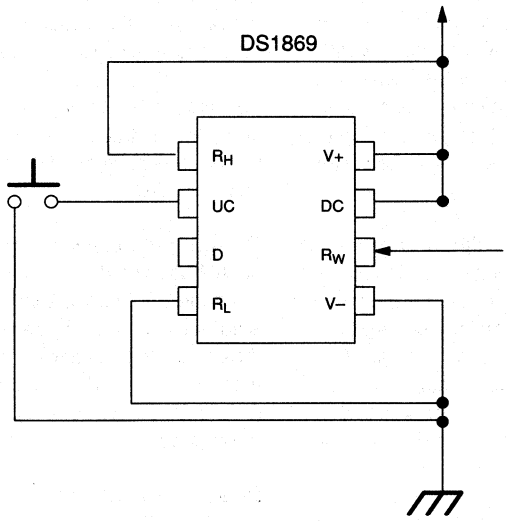
Changing the direction of wiper movement in single push–button mode is accomplish by a period of inactivity on the UC input of a (minimum) 1 second or greater. Also, in single push–button mode, as the wiper reaches the end of the potentiometer range its direction of movement reverses. This will occur, regardless, if the input is a continuous pulse, a sequence of repetitive pulses or a single pulse.

Dual push–button mode of operation is accomplished when the DC input is floated on power–up. If interfacing contact closure control inputs to digital logic, the DC input must be interfaced to an open drain drive which is high impedance during power–up. This will prevent the device from entering a single push–button mode of operation.

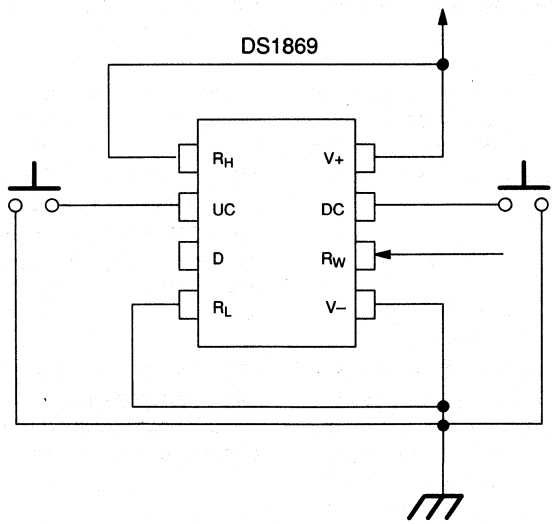
In dual push–button mode, each direction is controlled by the up contact (UC) and down contact (DC) inputs, respectively. No wait states are required to change wiper direction in dual push–button mode. In dual push–button mode, as the wiper position reaches the end of the potentiometer, the direction of wiper movement will not change. Wiper position will remain at the potentiometers' end until an opposite direction input is given.

All contact closure control inputs, UC, DC, and D are internally pulled–up by a 100K ohm resistance. The UC and DC inputs are internally debounced and require no external components for input signal conditioning.

DS1869 SINGLE PUSHBUTTON CONFIGURATION (TYPICAL EXAMPLE) Figure 1



DS1869 DUAL PUSHBUTTON CONFIGURATION (TYPICAL EXAMPLE) Figure 2



The DS1869 is provided with two supply inputs –V and +V. The maximum voltage difference between the two supply inputs is + 8.0 volts while the minimum voltage difference is 2.7 volts. All input levels are referenced to the negative supply input, –V. The voltage applied to any Dallastat terminal must not exceed the negative supply voltage (–V) by –0.5 or the positive supply voltage (+V) by + 0.5 volts. The minimum logic high level must be +2.4 volts with reference to the –V supply voltage input for +V=5V. A logic low level with reference to the –V supply voltage has a maximum value of +0.8 volts. Dallastats exhibit a typical wiper resistance of 400 ohms with a maximum wiper resistance of 1000 ohms. The maximum wiper current allowed through the Dallastat is specified at 1 milliamps (see DC Electrical Characteristics).

NONVOLATILE WIPER SETTINGS

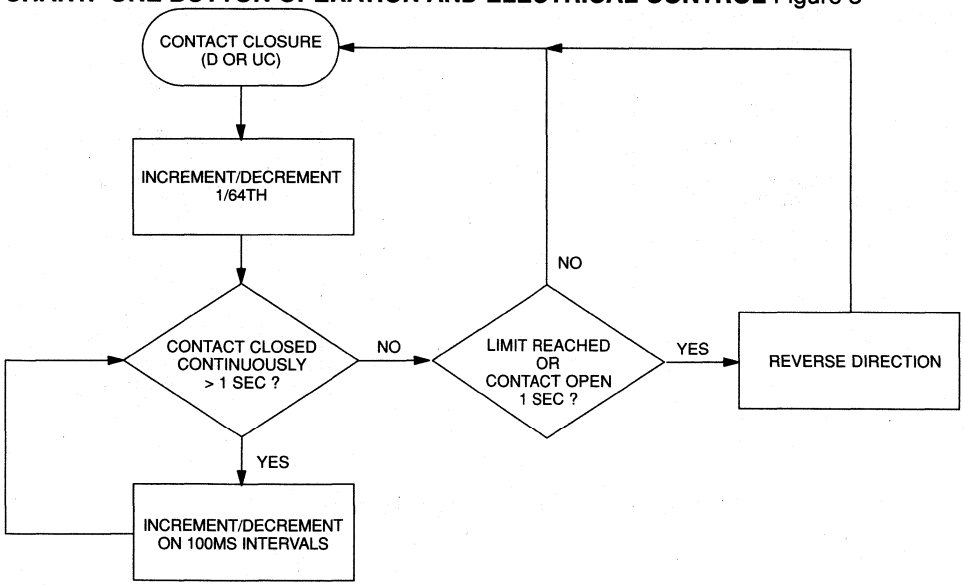
Dallastats maintain the position of the wiper in the absence of power. This feature is provided through the use of EEPROM type memory cell arrays. During normal operation the position of the wiper is determined by the input multiplexer. Periodically, the multiplexer will update the EEPROM memory cells. The manner in which an update occurs has been optimized for reliability, durability, and performance. Additionally, the update operation is totally transparent to the user.

When power is applied to the Dallastat, the wiper setting will be the last recorded in the EEPROM memory cells. If the Dallastat setting is changed after power is applied, the new value will be stored after a delay of 2 seconds. The initial storage of a new value after power–up occurs when the first change is made, regardless of when this change is made.

After the initial change on power–up, subsequent changes in the Dallastat EEPROM memory cells will occur only if the wiper position of the part is moved greater than 12.5% of the total resistance range. Any wiper movement after initial power–up which is less than 12.5% will not be recorded in the EEPROM memory cells. Since the Dallastat contains a 64–to–1 multiplexer, a change of greater than 12.5% corresponds to a change of the fourth LSB.

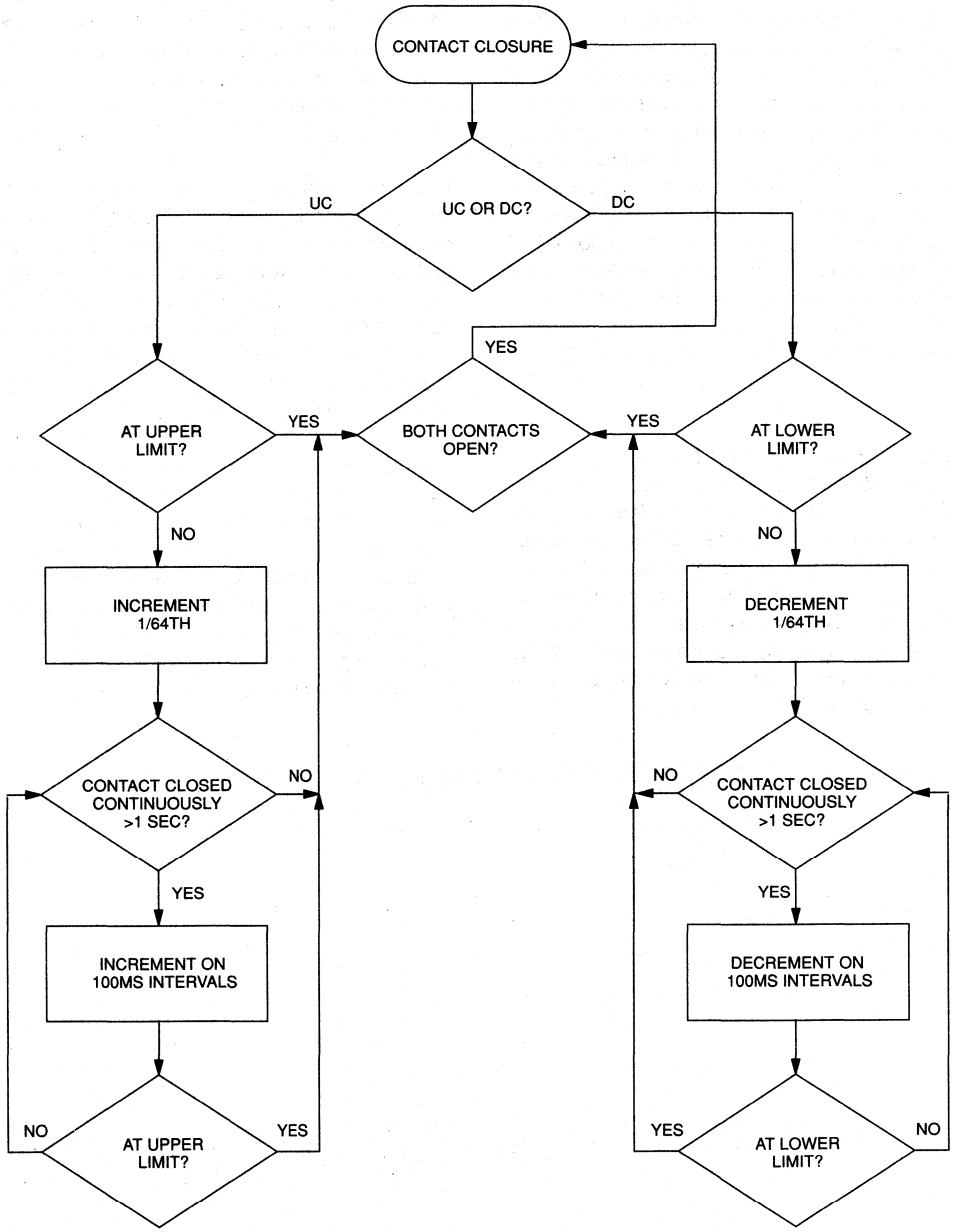
Changes or storage to the EEPROM memory cells must allow for a 2 second delay to guarantee that updates will occur. The EEPROM memory cells are specified to accept greater that 50,000 writes before a wear–out condition. If the EEPROM memory cells do reach a wear–out condition, the Dallastat will still function properly while power is applied. However, on power–up the device's wiper position will be that of the position last recorded before memory cell wear out.

FLOWCHART: ONE BUTTON OPERATION AND ELECTRICAL CONTROL Figure 3



CONTACT OPEN AND CONTACT CLOSURE TIMING IS 1 second ± 10%

FLOWCHART: TWO BUTTON OPERATION Figure 4



CONTACT OPEN AND CONTACT CLOSURE TIMING IS 1 second ± 10%

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to -V	-V –0.5V + 8.0V
Operating Temperature	0°C to 70°C commercial
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
+ Supply Voltage	+V	-V + 2.7		-V + 8.0	V	
- Supply Voltage	-V	+V - 8.0		+V - 2.7	V	
Rheostat Inputs	R_H,R_W,R_L	-V - 0.5		+V + 0.5	V	
Logic Input 1	V_{IH}	+2.4			V	1, 2, 10
Logic Input 0	V_{IL}			+0.8	V	1, 2, 10

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; -V to +V = 2.7V to 8.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
+, - Supply Current	I_{CC1}		1	2	mA	3
Supply Current, Idle State At 3.3V At 8.0V	I_{CC2}			 2 10	µA	9
Wiper Resistance	R_W		400	1000	Ω	
Wiper Current	I_W			1	mA	5
Rheostat Current	I_H, I_L			1	mA	5

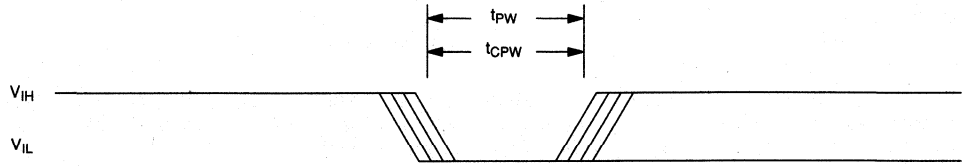
AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; -V to+V = 2.7V to 8.0V)

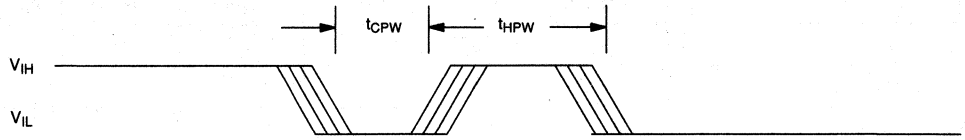
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width (D–input)	t_{PW}	1		DC	µs	1, 7, 8
Contact Pulse Width (UC, DC inputs)	t_{CPW}	1		DC	ms	1, 7, 8
Capacitance	C_{IN}		5	10	pF	6
Repetitive Input Pulse High Time	t_{HPW}	1		DC	ms	1, 7, 8
Continuous Input Pulse	t_{CCP}	1		DC	s	1, 7, 8

TIMING DIAGRAMS Figure 5

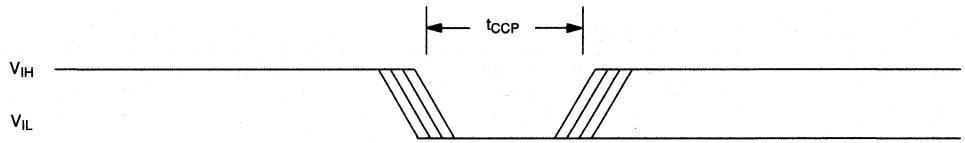
(A) SINGLE PULSE INPUTS



(B) REPETITIVE PULSE INPUTS



(C) CONTINUOUS PULSE INPUTS



NOTES:

1. All inputs; UC, DC, and D are internally pulled up with a resistance of 100KΩ.
2. Input logic levels are referenced to -V.
3. I_{CC} is the internal current that flows between -V and +V.
4. Input leakage applies to contact inputs UC and DC and digital input (D).
5. Wiper current and rheostat currents are the maximum current which can flow in the resistive elements.
6. Capacitance values apply at 25°C.
7. Input pulse width is the minimum time required for an input to cause an increment or decrement. If the UC, DC or D input is held active for longer than 1 second, subsequent increments or decrements will occur on 100 ms intervals until the inputs UC, DC, and/or D is released to V_{IH}.
8. Repetitive pulsed inputs on UC, DC, or D will be recognized as long as the pulse repetition occurs within 1 second of each other. Pulses occurring faster than 1 ms apart may not be recognized as individual inputs but can be interpreted a constant input. Tolerances for pulse timing ±10% on minimum inputs.
9. Idle state supply current is measured with no pushbutton pressed and with the wiper R_W tied to a CMOS load.
10. For +V referenced to –V=5V.

LINE INTERFACE

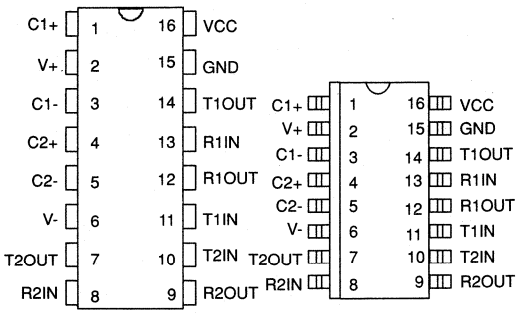
DALLAS SEMICONDUCTOR

DS1228
+5V Powered Dual RS-232 Transmitter/Receiver

FEATURES

- Operates from a single 5V power supply
- Two drivers and two receivers
- Meets all EIA RS-232-C specifications
- On-board voltage doubler
- On-board voltage inverter
- ± 30V input levels
- ± 9V output levels with + 5V supply
- Low-power CMOS
- Pin-compatible with the MAX 232
- Optional 16-pin SOIC surface mount package

PIN ASSIGNMENT



16–Pin DIP (300 MIL)
See Mech. Drawing
Pg. 480

16–Pin SOIC (300 MIL)
See Mech. Drawing
Pg. 484

PIN DESCRIPTION

C1+, C1	–	Capacitor 1 Connections
C2+, C2	–	Capacitor 2 Connections
V+, V-	–	± 10 Volts
T1IN, T2IN	–	Transmitter In
T1OUT, T2OUT	–	Transmitter Out
R1IN, R2IN	–	Receiver In
R1OUT, R2OUT	–	Receiver Out
V_{CC}	–	+5 Volts
GND	–	Ground

DESCRIPTION

The DS1228 is a dual RS-232-C Receiver/Transmitter that meets all EIA specifications while operating from a single, +5 volt supply. The DS1228 has two internal charge pumps. One of the charge pumps is used to generate +10 volts. The other is used to generate -10 volts. The DS1228 also contains four level translators. Two of the level translators are RS-232 transmitters which convert TTL/CMOS inputs into ±9V RS-232 outputs. The other two level translators are capable of operating with up to ±30V inputs. The DS1228 is suitable for all RS-232 communications and is particularly valuable where higher voltage power supplies for RS-232 drivers are not available. The power supply section of the DS1228 supplies ±10 volts from the V_{CC} input.

See the DS1229 data sheet for electrical specifications and operation.

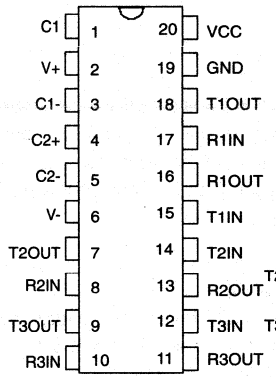
DALLAS SEMICONDUCTOR

DS1229
+5V Powered Triple RS-232 Transmitter/Receiver

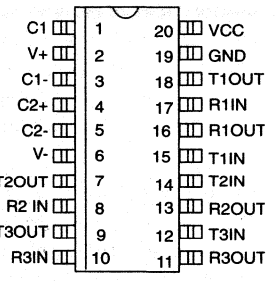
FEATURES

- Operates from a single 5V power supply
- Three drivers and three receivers
- Meets all EIA RS–232–C specifications
- Onboard voltage doubler
- Onboard voltage inverter
- ±30V input levels
- ±9V output levels with ±5V supply
- Low-power CMOS
- Optional 20-Pin SOIC surface mount package

PIN ASSIGNMENT



20-Pin DIP (300 MIL)
See Mech. Drawing
Pg. 480



20-Pin SOIC (300 MIL)
See Mech. Drawing
Pg. 484

PIN DESCRIPTION

C1+, C1-	Capacitor 1 Connections
C2+, C2-	Capacitor 2 Connections
V+, V-	±10 Volts
T1IN, T2IN, T3IN	Transmitter In
T1OUT, T2OUT, T3OUT	Transmitter Out
R1IN, R2IN, R3IN	Receiver In
R1OUT, R2OUT, R3OUT	Receiver Out
V_{CC}	+5 Volts
GND	Ground

DESCRIPTION

The DS1229 is a triple RS–232–C receiver/transmitter that meets all EIA specifications while operating from a single +5V supply. The DS1229 has two internal charge pumps which are used to generate ±10V. The DS1229 also contains six level translators, three of which are RS–232 transmitters that convert TTL/CMOS inputs into +9V RS-232 outputs. The other three level translators are RS–232 receivers that convert RS–232 inputs to 5V TTL/CMOS outputs. These receivers are capable of operating with up to ±30V inputs. The DS1229 is suitable for all RS–232–C communications and is particularly valuable where higher voltage power supplies for RS–232 drivers are not available. The power supply section of the DS1229 supplies ±10V from the V_{CC} input.

OPERATION

The DS1229 consists of three major sections: a triple transmitter, a triple receiver and a dual charge pump which generates ±10V from the 5V supply.

CHARGE PUMP SECTION

The dual charge pumps within the DS1229 are used to generate the voltages necessary for level conversion from TTL/CMOS to RS-232. One charge pump uses external capacitor C1 to double the V_{CC} input to +10V. The second charge pump uses external capacitor C2 to invert the +10V to -10V. Capacitors C3 and C4 are used to filter the +10V and -10V power supply. The recommended size of capacitors C1-C4 is 22 µF but the value is not critical. Increasing the value of C3 and C4 will lower the 16 KHz ripple on the +10V supplies and the RS-232 outputs. The value of C1 and C4 can be lowered to 1 µF where size is critical.

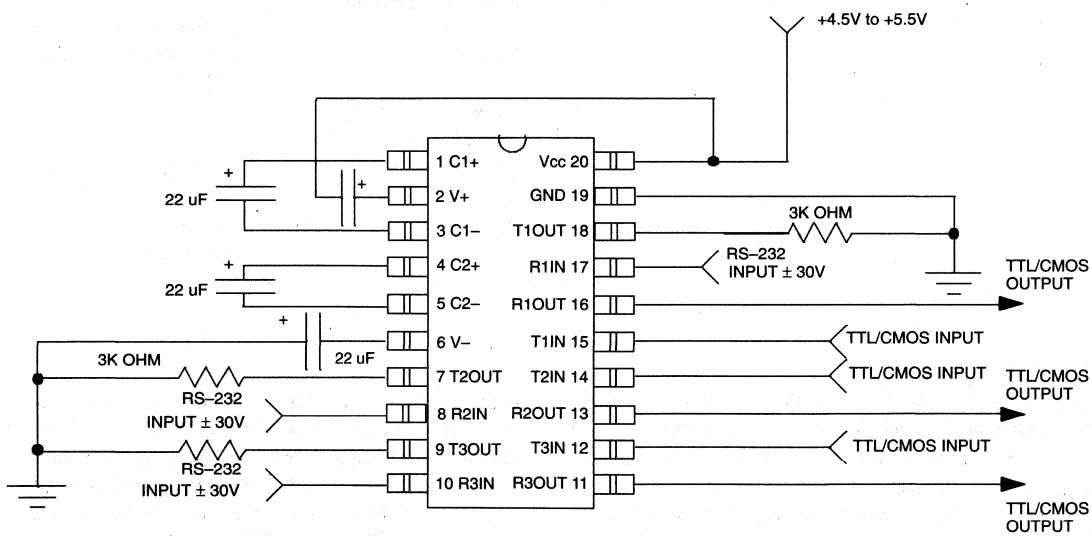
TRANSMITTER SECTION

The three transmitters are CMOS inverters powered by the internal +10V supply. The input is TTL/CMOS-compatible. Each input has an internal 750K pull-up resistor so that unused transmitter inputs can be left unconnected. Unused transmitter inputs will force the outputs low. The open circuit output voltage swing is from +10V to -10V. Worst-case conditions for RS-232-C of ±5V driving a 3K load are met at maximum allowable ambient temperature and a V_{CC} level of 5.0V. Typical voltage swings of ±9V occur with outputs of 5K and V_{CC} equal to 5V. The slew rate at the output is limited to less than 30V/us and the power-down output impedance will be a minimum of 300 ohms with ±2V applied to the outputs and V_{CC} at zero volts. The outputs are also short-circuit-protected and can be short-circuited to ground indefinitely.

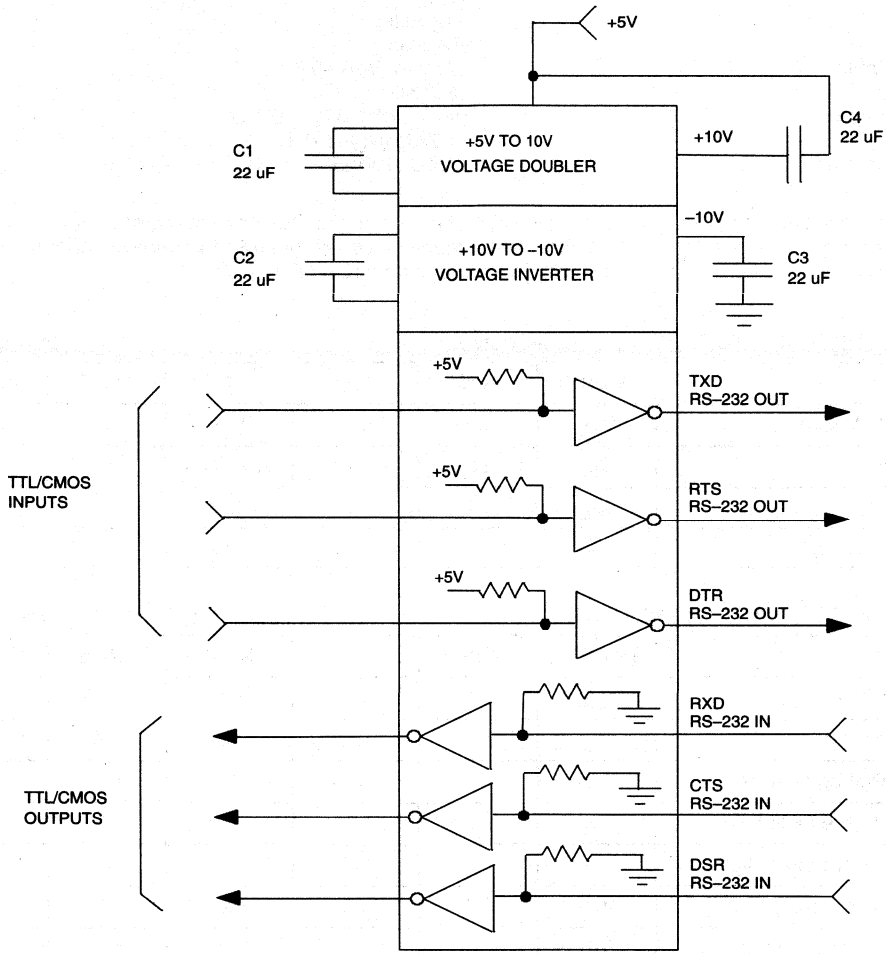
RECEIVER SECTION

The three receivers conform fully to the RS-232-C specifications. The input impedance is between 3K ohms and 7K ohms and can withstand up to ±30V with or without V_{CC} applied. The input switching thresholds are within the ±3V limit of RS-232-C specification with a V_{IL} of 0.7V and a V_{IH} of 2.4V. The receivers have 0.5 volts of hysteresis to improve noise rejection. The TTL/CMOS compatible output of the receiver will be low whenever the RS-232 input is greater than 2.4 volts. The receiver output will be high when the input is floating or driven between +0.8V and -30 V.

DS1229 RS-232 TRANSMITTER/RECEIVER Figure 1



TYPICAL APPLICATIONS Figure 2



ABSOLUTE MAXIMUM RATINGS*

V_{CC}	7.0V
V+	+12 volts
V-	-12 volts
Transmitter Inputs	-0.3V to (V_{CC} +0.3V)
Receiver Inputs	±30 volts
Transmitter Outputs	(V+ + 0.3V) to (V - -0.3V)
Receiver Outputs	-0.3V to (V_{CC} + 0.3V)
Storage Temperature	–55°C to +125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.2		V_{CC} +0.3	V	1
Logic 0 Input	V_{IL}	-0.3		+0.8	V	1
RS-232 Input Voltage	V_{RS}	-30		+30	V	1,2,11

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RS-232 Output Voltage	V_{ORS}	±4	±9	±10	V	3,12
Power Supply Current	I_{DD}		5	10	mA	4
Transmitter Pull-up Current	I_{TP}		5	200	µA	5
RS-232 Input Threshold Low	V_{TL}	0.7	1.2		V	6
RS-232 Input Threshold High	V_{TH}		1.7	2.4	V	6
RS-232 Input Hysteresis	V_{HY}	0.2	0.5	1.0	V	
Receiver Output Current @ 2.4V	I_{OH}	-1.0			mA	
Receiver Output Current @ 0.4V	I_{OL}			3.2	mA	
Output Resistance	R_{OUT}	300			ohms	7
RS-232 Output Current @ 0.4 V	I_{SC}			±25	mA	
Propagation Delay	t_{PD}		3		µs	8
Transmitter Output Instantaneous Slew Rate	t_{SR}			30	V/µs	9
Transmitter Output Transition Slew Rate	t_{TSR}		3		V/µs	10

NOTES:

1. All voltages are referenced to ground.
2. Applies to Receiver Inputs only.
3. T1, T2, and T3 loaded with 3K ohms to ground.
4. All outputs are unloaded.
5. T1, T2, and T3 Inputs = 0 volts.
6. V_{CC} = +5 volts.
7. V_{OUT} = ±2 volts.
8. RS-232 to TTL or TTL to RS-232.
9. C_L = 10 pF, R_L = 3K, t_A = 0°C. This parameter is sample tested only.
10. R_L = 3K, C_L = 2500 pF measured from +3 volts to -3 volts or -3 volts to +3 volts.
11. This parameter is sample tested only.
12. Negative output level of -5V is increased to -4.0 for the DS1229 only. Positive output level remains at +5V. Use of a +10%, -5% power supply will restore the negative level to -5V.

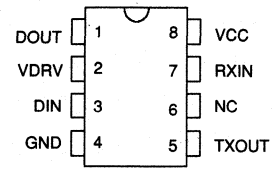
DALLAS SEMICONDUCTOR

DS1275
Line-Powered RS-232 Transceiver Chip

FEATURES

- Low-power serial transmitter/receiver for battery-backed systems
- Transmitter steals power from receive signal line to save power
- Ultra-low static current, even when connected to RS-232-C port
- Variable transmitter level from +5 to +12 volts
- Compatible with RS-232-C signals
- Available in 8-pin, 150-mil wide SOIC package (DS1275S)
- Low-power CMOS

PIN ASSIGNMENT



DS1275 8-Pin DIP (300 Mil.)
See Mech. Drawing – Pg. 480

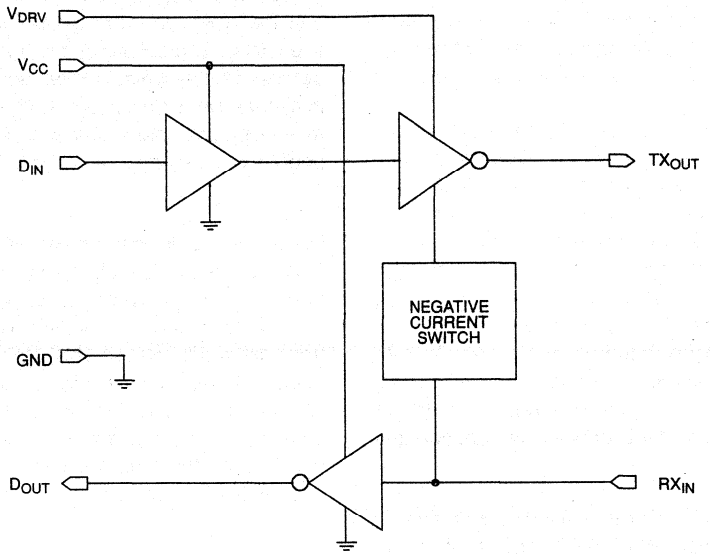
PIN DESCRIPTION

D_{OUT}	–	Digital data out
V_{DRV}	–	Transmit driver +V
D_{IN}	–	Digital data in
GND	–	System ground (0V)
TX_{OUT}	–	Transmit RS-232 out
NC	–	No connection
RX_{IN}	–	Receive RS-232 in
V_{CC}	–	System logic supply (+5V)

DESCRIPTION

The DS1275 Line-Powered RS-232 Transceiver Chip is a CMOS device that provides a low-cost, very low-power interface to RS-232 serial ports. The receiver input translates RS-232 signal levels to common CMOS/TTL levels. The transmitter employs a unique circuit which steals current from the receive RS-232 signal when that signal is in a negative state (marking). Since most serial communication ports remain in a negative state statically, using the receive signal for negative power greatly reduces the DS1275's static power consumption. This feature is especially important for battery-powered systems such as laptop computers, remote sensors, and portable medical instruments. During an actual communication session, the DS1275's transmitter will use system power (5-12 volts) for positive transitions while still employing the receive signal for negative transitions.

DS1275 BLOCK DIAGRAM Figure 1



OPERATION

Designed for the unique requirements of battery-backed systems, the DS1275 provides a low-power half-duplex interface to an RS-232 serial port. Typically, a designer must use an RS-232 device which uses system power during both negative and positive transitions of the transmit signal to the RS-232 port. If the connector to the RS-232 port is left connected for an appreciable time after the communication session has ended, power will statically flow into that port, draining the battery capacity. The DS1275 eliminates this static current drain by stealing current from the receive line (RX_{IN}) of the RS-232 port when that line is at a negative level (marking). Since most asynchronous communication over an RS-232 connection typically remains in a marking state when data is not being sent, the DS1275 will not consume system power in this condition. System power would only be used when positive-going transitions are needed on the transmit RS-232 output (TX_{OUT}) when data is sent. However, since synchronous communication sessions typically exhibit a very low duty-cycle, overall system power consumption remains low.

RECEIVER SECTION

The RX_{IN} pin is the receive input for an RS-232 signal whose levels can range from ±3 to ±15 volts. A negative data signal is called a mark while a positive data signal is called a space. These signals are inverted and then level-shifted to normal +5 volt CMOS/TTL logic levels. The logic output associated with RX_{IN} is D_{OUT} which swings from $+V_{CC}$ to ground. Therefore, a mark on RX_{IN} produces a logic 1 at D_{OUT}; a space produces a logic 0.

The input threshold of RX_{IN} is typically around 1.8 volts with 500 millivolts of hysteresis to improve noise rejection. Therefore, an input positive-going signal must exceed 1.8 volts to cause D_{OUT} to switch states. A negative-going signal must now be lower than 1.3 volts (typically) to cause D_{OUT} to switch again. An open on RX_{IN} is interpreted as a mark, producing a logic 1 at D_{OUT}.

TRANSMITTER SECTION

D_{IN} is the CMOS/TTL-compatible input for digital data from the user system. A logic 1 at D_{IN} produces a mark (negative data signal) at TX_{OUT} while a logic 0 produces a space (positive data signal). As mentioned earlier, the transmitter section employs a unique driver design that uses the RX_{IN} line for swinging to negative levels. The RX_{IN} line must be in a marking or idle state to take advantage of this design; if RX_{IN} is in a spacing state, TX_{OUT} will only swing to ground. When TX_{OUT} needs to

transition to a positive level, it uses the V_{DRV} power pin for this level. V_{DRV} can be a voltage supply between 5 to 12 volts, and in many situations it can be tied directly to the +5 volt V_{CC} supply. *It is important to note that V_{DRV} must be greater than or equal to V_{CC} at all times.*

The voltage range on V_{DRV} permits the use of a 9-volt battery in order to provide a higher voltage level when TX_{OUT} is in a space state. When V_{CC} is shut off to the DS1275 and V_{DRV} is still powered (as might happen in a battery-backed condition) , only a small leakage current (about 50-100 nA) will be drawn. If TX_{OUT} is loaded during such a condition, V_{DRV} will draw current only if RX_{IN} is not in a negative state. During normal operation (V_{CC}=5 volts), V_{DRV} will draw less than 2 uA when TX_{OUT} is marking. Of course, when TX_{OUT} is spacing, V_{DRV} will draw substantially more current – about 3 mA depending upon its voltage and the impedance that TX_{OUT} sees.

The TX_{OUT} output is slew-rate limited to less than 30 volts/us in accordance with RS-232 specifications. In the event TX_{OUT} should be inadvertently shorted to ground, internal current-limiting circuitry prevents damage, even if continuously shorted.

RS-232 COMPATIBILITY

The intent of the DS1275 is not so much to meet all the requirements of the RS-232 specification as to offer a low-power solution that will work with most RS-232 ports with a connector length of less than 10 feet. As a prime example, the DS1275 will not meet the RS-232 requirement that the signal levels be at least ±5 volts minimum when terminated by a 3K ohm load and V_{DRV}= +5 volts. Typically a voltage of 4 volts will be present at TX_{OUT} when spacing. However, since most RS-232 receivers will correctly interpret any voltage over 2 volts as a space, there will be no problem transmitting data.

APPLICATIONS INFORMATION

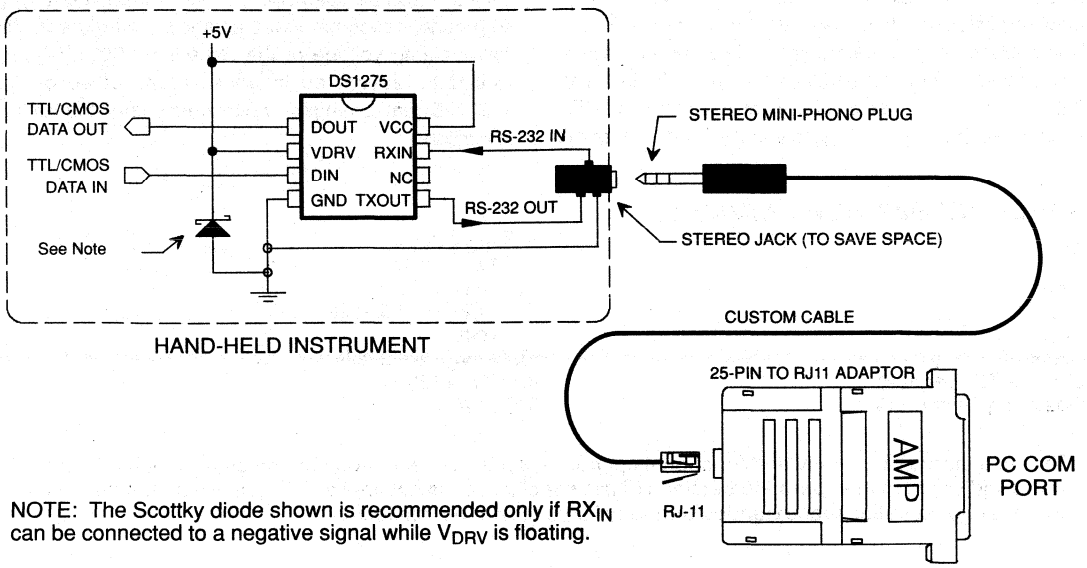
The DS1275 is designed as a low-cost, RS-232-C interface expressly tailored for the unique requirements of battery-operated handheld products. As shown in the electrical specifications, the DS1275 draws exceptionally low operating and static current. During normal operation when data from the handheld system is sent from the TX_{OUT} output, the DS1275 only draws significant V_{DRV} current when TX_{OUT} transitions positively (spacing). This current flows primarily into the RS-232 receiver's 3-7K ohm load at the other end of the attaching cable. When TX_{OUT} is marking (a negative data signal), the V_{DRV} current falls dramatically since the negative voltage is provided by the transmit signal from the other end of the cable. This represents a large reduction in overall operating current, since typical RS-232 interface chips use charge-pump circuits to establish both positive and negative levels at the transmit driver output.

To obtain the lowest power consumption from the DS1275, observe the following guidelines. First, to minimize V_{DRV} current when connected to an RS-232 port, always maintain D_{IN} at a logic 1 when data is not being transmitted (idle state). This will force TX_{OUT} into the marking state, minimizing V_{DRV} current. Second, V_{DRV} current will drop to less than 100 nA when V_{CC} is grounded. Therefore, if V_{DRV} is tied directly to the system battery, the logic +5 volts can be turned off to achieve the lowest possible power state.

FULL-DUPLEX OPERATION

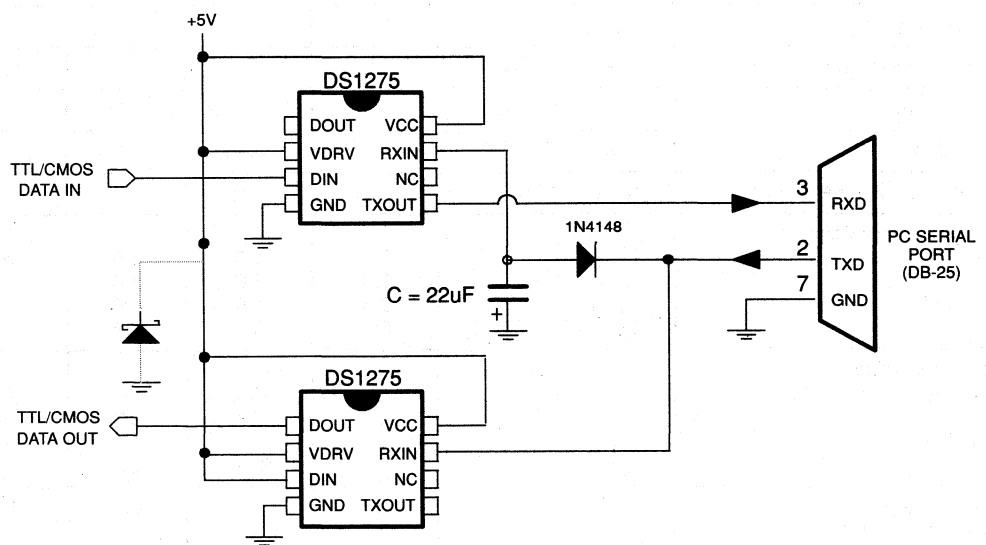
The DS1275 is intended primarily for half-duplex operation; that is, RX_{IN} should remain idle in the marking state when transmitting data out TX_{OUT} and visa versa. However, the part can be operated full-duplex with most RS-232-C serial ports since signals swinging between 0 and +5V will usually be correctly interpreted by an RS-232-C receiver device. The 5-volt swing occurs when TX_{OUT} attempts to swing negative while RX_{IN} is at a positive voltage, which turns on an internal weak pull-down to ground for the TX_{OUT} driver's negative reference. So, transmit mark signals at TX_{OUT} may have voltage jumps from some negative value (corresponding to RX_{IN} marking) to approximately ground. One possible problem that may occur in this case is if the receiver at the other end requires a negative voltage for recognizing a mark. In this situation, the full- duplex circuit shown in Figure 3 can be used as an alternative. The 22 µF capacitor forms a negative-charge reservoir; consequently, when the TXD line is spacing (positive), TX_{OUT} still has a negative source available for a time period determined by the capacitor and the load resistance at the other end (3-7K ohms). This circuit was tested from 150-19,200 bps with error-free operation using a SN75154 Quad Line Receiver as the receiver for the TX_{OUT} signal. Note that the SN75154 can have a marking input threshold below ground; hence there is the need for TX_{OUT} to swing both positive and negative in full-duplex operation with this device.

HANDHELD RS-232-C APPLICATION USING A STEREO MINI-JACK Figure 2



NOTE: The Scottky diode shown is recommended only if RX_{IN} can be connected to a negative signal while V_{DRV} is floating.

FULL-DUPLEX CIRCUIT USING NEGATIVE-CHARGE STORAGE Figure 3



NOTE:

The capacitor stores negative charge whenever the TXD signal from the PC serial port is in a marking data state (a negative voltage that is typically -10 volts). The top DS1275's TX_{OUT} uses this negative charge reservoir when it is in a marking state. The capacitor will discharge to 0 volts when the TXD line is spacing (and TX_{OUT} is still marking) at a time constant determined by its value and the value of the load resistance reflected back to TX_{OUT}. However, when TXD is marking, the capacitor will quickly charge back to -10 volts. Note that TXD remains in a marking state when idle, which improves the performance of this circuit.

LATCHUP PROTECTION

In most cases the DS1275 offers a high level of ESD and latchup protection. However, latchup can occur if V_{DRV} is left floating (high impedance) while a negative signal is attached to RX_{IN}. One possible scenario for this is as follows: if the handheld device is powered off with a FET switch, floating V_{DRV}, and at the same time the user still has the the RS-232-C port connected. In order to eliminate this latchup potential, a Schottky diode from V_{DRV} to ground is recommended as shown in Figure 2. The lower clamp voltage of the Schottky (300 mV) is required to prevent an internal silicon diode on the DS1275 from turning on, which precipitates the latchup condition.

ABSOLUTE MAXIMUM RATINGS*

V_{CC}	-0.3 to +7 volts
V_{DRV}	-0.3 to +13 volts
RX_{IN}	±15 volts
D_{IN}	-0.3 to V_{CC} + 0.3 volts
TX_{OUT}	±15 volts
D_{OUT}	-0.3 to V_{CC} + 0.3 volts
Storage Temperature	-55°C to +125°C
Operating Temperature	0°C to 70°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic Supply	V_{CC}	4.5	5.0	5.5	V	1
Transmit Driver Supply	V_{DRV}	4.5	5-12	13.0	V	1
Logic 1 Input	V_{IH}	2.0		V_{CC}+0.3	V	2
Logic 0 Input	V_{IL}	-0.3		+ 0.8	V	
RS-232 Input Range (RX_{IN})	V_{RS}	-15		+15	V	
Dynamic Supply Current $D_{IN} = V_{CC}$ D_{IN} = GND	 I_{DRV1} I_{CC1} I_{DRV1} I_{CC1}		 0.1 0.5 3.8 0.5	 5.0 5.0 5.0 5.0	 mA mA mA mA	3
Static Supply Current $D_{IN} = V_{CC}$ D_{IN} = GND	 I_{DRV2} I_{CC2} I_{DRV2} I_{CC2}		 1.5 10.0 3.8 10.0	 15.0 15.0 5.0 30.0	 µA µA mA µA	4
Driver Leakage Current (V_{CC}= 0V)	I_{DRV3}		0.05	1.0	µA	5

DC ELECTRICAL CHARACTERISTICS

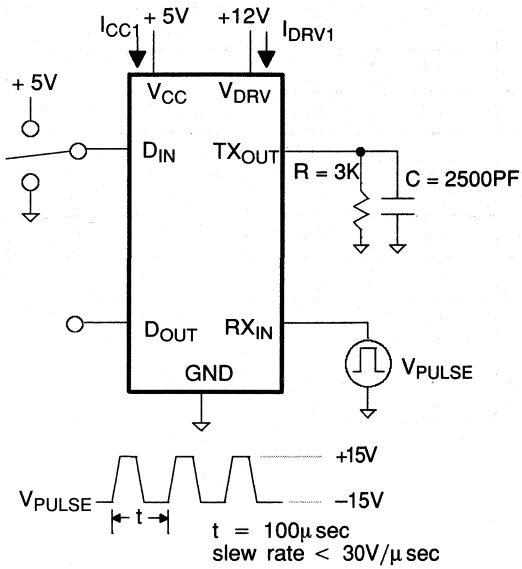
(0°C to 70°C; V_{CC} = V_{DRV} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TX_{OUT} Level High	V_{OTXH}	3.5	4.0	4.5	V	6
TX_{OUT} Level Low	V_{OTXL}	-8.5	-9.0		V	7
TX_{OUT} Short Circuit Current	I_{SC}		+60	+85	mA	
TX_{OUT} Output Slew Rate	t_{SR}			30	V/µs	
Propagation Delay	t_{PD}		5		µs	8
RX_{IN} Input Threshold Low	V_{TL}	0.8	1.2	1.6	V	
RX_{IN} Input Threshold High	V_{TH}	1.6	2.0	2.4	V	
RX_{IN} Threshold Hysteresis	V_{HYS}	0.5	0.8		V	9
D_{OUT} Output Current @ 2.4 V	I_{OH}	-1.0			mA	
D_{OUT} Output Current @ 0.4 V	I_{OL}			3.2	mA	

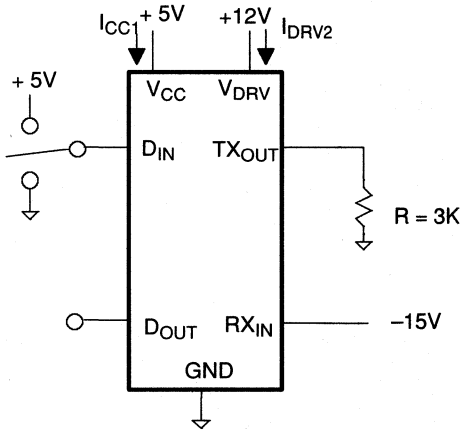
NOTES:

1. V_{DRV} must be greater than or equal to V_{CC}.
2. V_{CC} = V_{DRV} = 5V ± 10%.
3. See test circuit in Figure 4.
4. See test circuit in Figure 5.
5. See test circuit in Figure 6.
6. D_{IN} = V_{IL} and TX_{OUT} loaded by 3K ohms to ground.
7. D_{IN} = V_{IH} , RX_{IN} = -10 volts and TX_{OUT} loaded by 3K ohms to ground.
8. D_{IN} to TX_{OUT} - see Figure 7.
9. V_{HYS} = V_{TH} - V_{TL}.

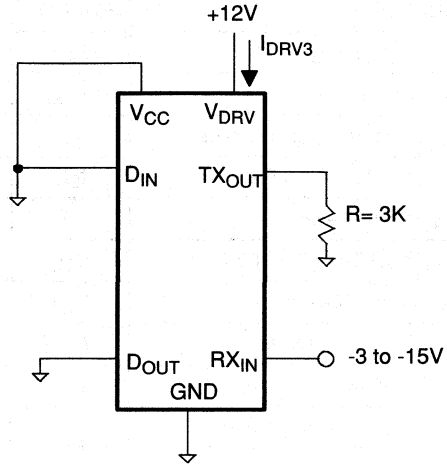
DYNAMIC OPERATING CURRENT TEST CIRCUIT Figure 4



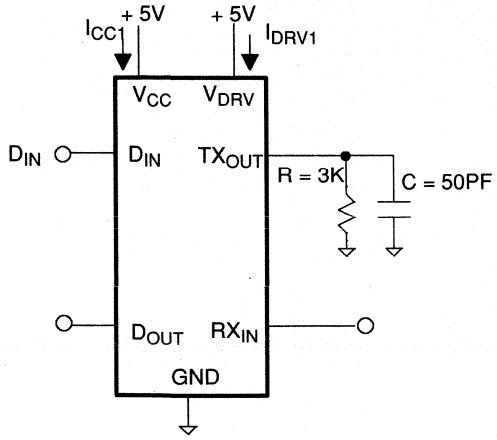
STATIC OPERATING CURRENT TEST CIRCUIT Figure 5

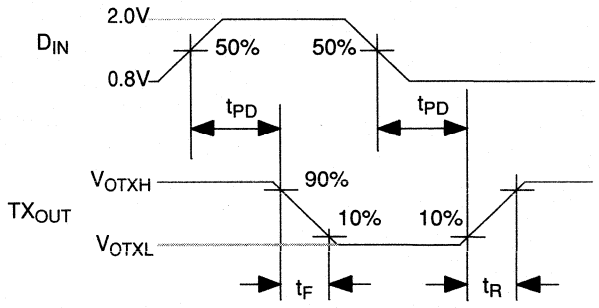


DRIVER LEAKAGE TEST CIRCUIT Figure 6



PROPAGATION DELAY TEST CIRCUIT Figure 7





$$t_{SR} = \frac{0.8(V_{OTXH} - V_{OTXL})}{t_F \text{ or } t_R}$$

SILICON TIMED CIRCUITS

SILICON TIMED CIRCUITS

DELAY LINES (HYBRID REPLACEMENTS)

Multiple-Tap Delays

# Taps	Part #	Packages	Features
5	DS1000	DIP, Gull, SO, Clip	4 to 500ns delays Pin-compatible with standard hybrids
	DS1004	DIP, Gull, SO	2 to 5ns tap-to-tap increments Temperature and voltage compensation
	DS1005	DIP, Gull, SO, Clip	12 to 500ns delays Temperature and voltage compensation
10	DS1010	DIP, Gull, SO	5 to 500ns delays Pin-compatible with standard hybrids

Multiple Independent Delays

# Delays	Part #	Packages	Features
3	DS1013	DIP, Gull, SO	10 to 200ns delays Pin-compatible with standard hybrids
	DS1033	DIP, SO TSSOP	8 to 30ns delays 3 to 5V operation
	DS1035	DIP, SO TSSOP	6 to 30ns delays High-speed, low-power
4	DS1044	DIP,Gull, SO	6 to 30ns delays Pin-compatible with standard hybrids
7	DS1007	DIP,Gull, SO	3 to 40ns delays

DELAY LINES (SYSTEM ENHANCEMENT)

# Delays	Part #	Packages	Features
1	DS1003	DIP, Gull	4-tap delay for RISC processors ±0.75ns tap-to-tap tolerance
1	DS1020	DIP,SO	8-bit programmable 0.15 to 2ns steps
2	DS1012	DIP,Gull, SO	3 to 50ns delays On-chip logic, can be used as frequency doubler
2	DS1045	DIP, SO	4-bit programmable 9 to 84ns delays

SYSTEM TIMING FUNCTIONS

Description	Part #	Packages	Key Features
Programmable one-shot	DS1040	DIP, Gull, SO	5 to 500ns pulse width No external components
Crystalless Oscillator Available 3Q94	DS1055	DIP, SO, TSSOP	5 to 66 MHz operation No external components

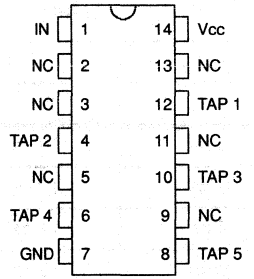
DALLAS SEMICONDUCTOR

DS1000
5-Tap Silicon Delay Line

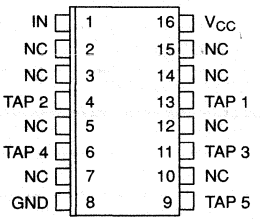
FEATURES

- All-silicon time delay
- 5 taps equally spaced
- Delays are stable and precise
- Both leading and trailing edge accuracy
- Delay tolerance ±5% or ±2 ns, whichever is greater
- Economical
- Auto-insertable, low profile
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom delays available
- Fast turn prototypes
- Extended temperature range available

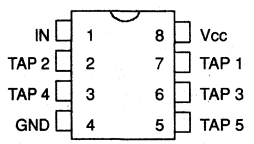
PIN ASSIGNMENT



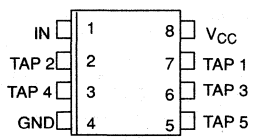
DS1000 14-PIN DIP (300 MIL)
DS1000G 14-PIN GULLWING (300 MIL)
DS1000K 14-PIN SHEARED NC
See Mech. Drawings
Pgs. 480 & 491



DS1000S 16-PIN SOIC
(300 MIL)
See Mech. Drawing
Pg. 484



DS1000M 8-PIN DIP (300 MIL)
DS1000H 8-PIN GULLWING (300 MIL)
See Mech. Drawings
Pgs. 480 & 491



DS1000Z 8-PIN SOIC
(150 MIL)
See Mech. Drawing
Pg. 483

PIN DESCRIPTION

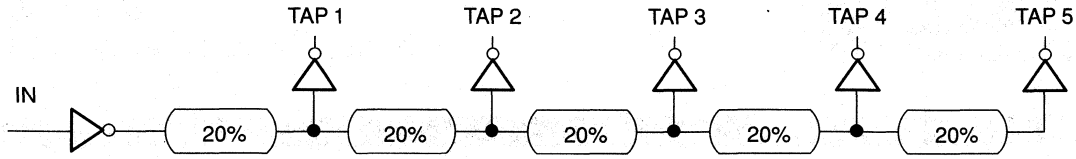
TAP 1-TAP 5	- TAP Output Number
V_{CC}	- +5 Volts
GND	- Ground
NC	- No Connection
IN	- Input

DESCRIPTION

The DS1000 series delay lines have five equally spaced taps providing delays from 4 ns to 500 ns. These devices are offered in a standard 14-pin DIP that is pin-compatible with hybrid delay lines. Alternatively, 8-pin DIPs and surface mount packages are available to save PC board area. Low cost and superior reliability over hybrid technology is achieved by the combination of a 100% silicon delay line and industry standard DIP and SOIC packaging. In order to maintain complete pin compatibility, DIP packages are available with hybrid lead configurations. The DS1000 series delay lines provide a nominal accuracy of ±5% or ±2 ns, whichever is greater. The DS1000 5-Tap Silicon Delay Line reproduces the input logic state at the output after a fixed delay as specified by the extension of the part number after the dash. The DS1000 is designed to reproduce both leading and trailing edges with equal precision. Each tap is capable of driving up to ten 74LS loads.

Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450-5348.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PHL}, t_{PLH}) Table 1

PART NO.	TAP 1	TAP 2	TAP 3	TAP 4	TAP 5
DS1000-20	4 ns	8 ns	12 ns	16 ns	20 ns
DS1000-25	5 ns	10 ns	15 ns	20 ns	25 ns
DS1000-30	6 ns	12 ns	18 ns	24 ns	30 ns
DS1000-35	7 ns	14 ns	21 ns	28 ns	35 ns
DS1000-40	8 ns	16 ns	24 ns	32 ns	40 ns
DS1000-45	9 ns	18 ns	27 ns	36 ns	45 ns
DS1000-50	10 ns	20 ns	30 ns	40 ns	50 ns
DS1000-60	12 ns	24 ns	36 ns	48 ns	60 ns
DS1000-75	15 ns	30 ns	45 ns	60 ns	75 ns
DS1000-100	20 ns	40 ns	60 ns	80 ns	100 ns
DS1000-125	25 ns	50 ns	75 ns	100 ns	125 ns
DS1000-150	30 ns	60 ns	90 ns	120 ns	150 ns
DS1000-175	35 ns	70 ns	105 ns	140 ns	175 ns
DS1000-200	40 ns	80 ns	120 ns	160 ns	200 ns
DS1000-250	50 ns	100 ns	150 ns	200 ns	250 ns
DS1000-350	70 ns	140 ns	210 ns	280 ns	350 ns
DS1000-450	90 ns	180 ns	270 ns	360 ns	450 ns
DS1000-500	100 ns	200 ns	300 ns	400 ns	500 ns

Custom delays available.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC} + 0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	uA	
Active Current	I_{CC}	V_{CC}= Max; Period= Min.		35	75	mA	2,8
High Level Output Current	I_{OH}	V_{CC}=Min. V_{OH}=4			-1	mA	
Low Level Output Current	I_{OL}	V_{CC}=Min. V_{OL}=0.5	12			mA	

AC ELECTRICAL CHARACTERISTICS

(T_A = 25°C; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}	40% of Tap 5 t_{PLH}			ns	7
Input to Tap Delay (leading edge)	t_{PLH}		Table 1		ns	3, 4, 5, 6, 9
Input to Tap Delay (trailing edge)	t_{PHL}		Table 1		ns	3, 4, 5, 6, 9
Power-up Time	t_{PU}			100	ms	
	Period	4 (t_{WI})			ns	7

CAPACITANCE

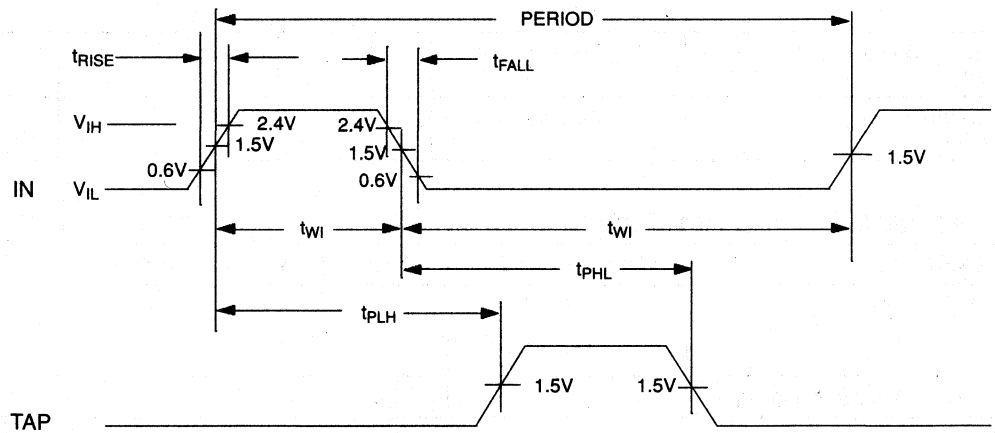
(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

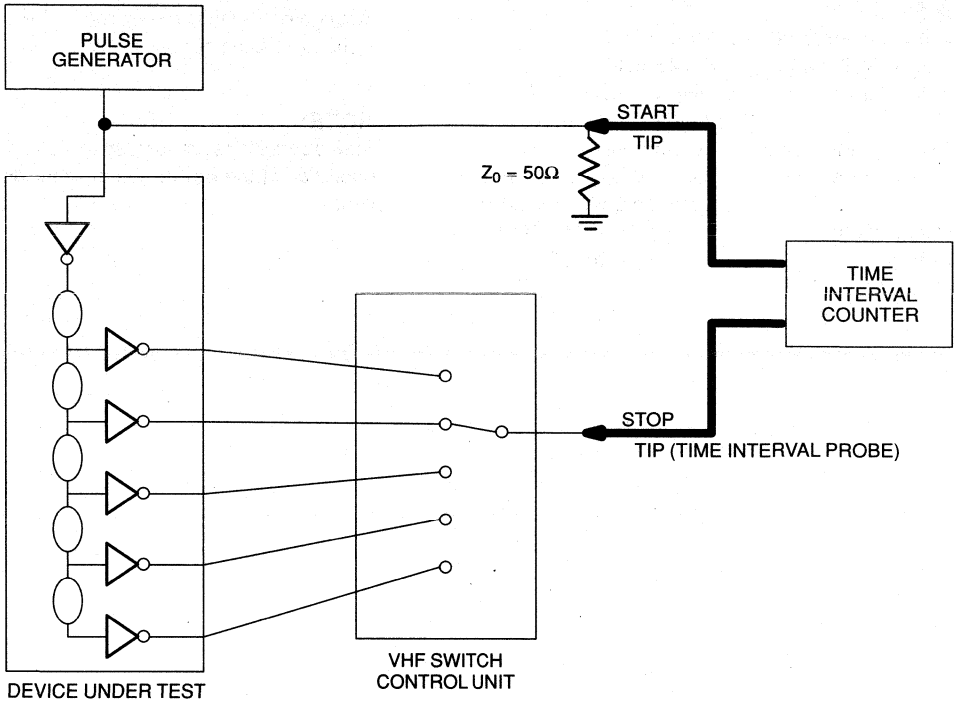
NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. V_{CC}= 5V @25°C. Delays accurate on both rising and falling edges within ±2 ns or 5%, whichever is greater.
4. For DS1000 delay lines with a TAP 5 delay of 50 ns or greater, temperature variations from 25°C to 0°C or 70°C may produce an additional input to tap delay shift of ± 1 ns or ± 3%, whichever is greater.
5. For DS1000 delay lines with a TAP 5 delay less than 50 ns, temperature variations from 25°C to 0°C or 70°C may produce an additional input to tap delay shift of ± 1 ns or ± 10%, whichever is greater.
6. All tap delays tend to vary unidirectionally with temperature or voltage changes. For example, if TAP 1 slows down, all other taps also slow down; TAP3 can never be faster than TAP2.
7. Pulse width and period specifications may be exceeded; however, accuracy will be application-sensitive (decoupling, layout, etc.).
8. I_{CC} is a function of frequency and TAP 5 delay. Only a -25 operating with a 40 ns period and V_{CC} = 5.25V will have an I_{CC} = 75 mA. For example a -100 will never exceed 30 mA, etc.
9. See "Test Conditions" section at the end of this data sheet.

TIMING DIAGRAM-SILICON DELAY LINE Figure 2



TEST CIRCUIT Figure 3



TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any tap output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any tap output pulse.

TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1000. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each tap. Each tap is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT :

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50 ohm Max.
Rise and Fall Time:	3.0 ns Max. (measured between 0.6V and 2.4V)
Pulse Width:	500 ns (1 µs for -500)
Period:	1 µs (2 µs for -500)

OUTPUT:

Each output is loaded with the equivalent of one 74F04 input gate. Delay is measured at the 1.5V level on the rising and falling edge.

NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

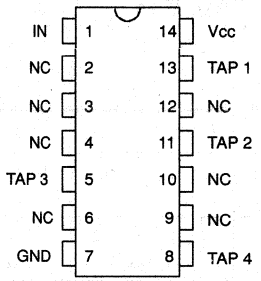
DALLAS SEMICONDUCTOR

DS1003
4-Tap Silicon Delay Line for RISC Applications

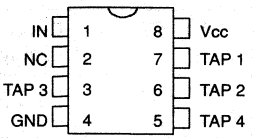
FEATURES

- All-silicon time delay
- Four delayed clock phases from input
- Input frequency independent
- Precise tap-to-tap delays
- Leading and trailing edge precision
- Preserves input symmetry
- Output rise time minimizes ringing
- Economical
- 8- and 14-pin packages available in DIP and surface mount
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom delays and pinouts available
- Fast turn prototypes

PIN ASSIGNMENT



DS1003 14-PIN DIP
(300 MIL)
DS1003G 14-PIN GULLWING
(300 MIL)
See Mech. Drawings
Pgs. 480 & 491



DS1003M 8-PIN DIP
(300 MIL)
DS1003H 8-PIN GULLWING
(300 MIL)
See Mech. Drawings
Pgs. 480 & 491

PIN DESCRIPTION

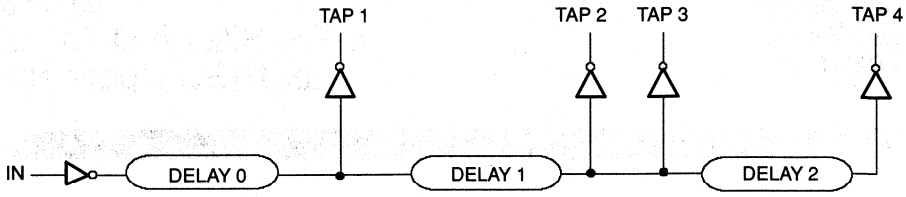
TAP 1 – TAP 4	–	TAP Output Number
V_{CC}	–	+5 Volts
GND	–	Ground
NC	–	No Connection
IN	–	Input

DESCRIPTION

The DS1003 Delay Line has been specifically designed to supply the four independent clock timing phases required by some RISC microprocessors and their related coprocessors. For optimum compatibility, the DS1003 accepts TTL input levels and supplies CMOS and TTL compatible output levels. The DS1003 is offered in 8- and 14-pin DIP and gullwing packages for surface mounting. Low cost and superior reliability is achieved by the combination of a 100% silicon delay line and industry standard packaging. The DS1003 series of delay lines provides precise tap-to-tap delays while preserving input waveform symmetry. Since the DS1003 is not based on Phase Locked Loop (PLL) technology, timing is input frequency-independent. Each tap is capable of driving a minimum of four LSTTL or CMOS loads. Tap-to-tap timing accuracy is not affected by the addition of equal capacitive loads (e.g. coprocessors).

Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450–5348.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PLH}) Table 1

PART NO.		DS1003-16	DS1003-20	DS1003-25	DS1003-33	DS1003-40
INPUT - TAP 1	Delay 0	8 ns ± 2 ns	8 ns ± 2 ns	8 ns ± 2 ns	6 ns ± 2 ns	6 ns ± 2 ns
TAP 1 - TAP 2	Delay 1	6 ns ± .75 ns	6 ns ± .75 ns	6 ns ± .5 ns	4.5 ns ± .5 ns	4.0 ns ± .5 ns
TAP 1 - TAP 4	Delay 1+ Delay 2	16 ns ± 1 ns	14 ns ± 1 ns	12 ns ± .75 ns	9 ns ± .75 ns	8 ns ± .75 ns
TAP 2 - TAP 3 (Note 10)	——	0.2 ns ± .2 ns	0.2 ns ± .2 ns	0.2 ns ± .2 ns	0.2 ns ± .2 ns	0.2 ns ± .2 ns
TAP 3 - TAP 4	Delay 2	10 ns ± .75 ns	8 ns ± .75 ns	6 ns ± .5 ns	4.5 ns ± .5 ns	4.0 ns ± .5 ns

PERIOD AND WIDTH TABLE Table 2

PART NO.	PERIOD			t_{WI}		
	MIN	NOM	MAX	MIN	NOM	MAX
DS1003-16	29 ns	30 ns	∞	12 ns	15 ns	∞
DS1003-20	24 ns	25 ns	∞	10 ns	12.5 ns	∞
DS1003-25	19 ns	20 ns	∞	8 ns	10 ns	∞
DS1003-33	14 ns	15 ns	∞	6 ns	7.5 ns	∞
DS1003-40	12 ns	12.5 ns	∞	5 ns	6.25 ns	∞

I_{CC} TABLE Table 3

PART NO.	I_{CC}	
	TYP	MAX
DS1003-16	65 mA	75 mA
DS1003-20	75 mA	85 mA
DS1003-25	85 mA	95 mA
DS1003-33	100 mA	110 mA
DS1003-40	115 mA	125 mA

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC} + 0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	µA	
Active Current	I_{CC}	V_{CC} = Max; Period = Min.		Table 3	Table 3	mA	2
High Level Output Current	I_{OH}	V_{CC} = Min. V_{OH} = 4			-1	mA	
Low Level Output Current	I_{OL}	V_{CC} = Min V_{OH} = 0.5	12			mA	

AC ELECTRICAL CHARACTERISTICS

(T_A = 25°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}	Table 2	Table 2	Table 2	ns	6
TAP to TAP Delay (leading edge)	t_{PLH}	Table 1	Table 1	Table 1	ns	3,4,5,6,7
TAP to TAP Delay (trailing edge)	t_{PHL}		Note 9		ns	9
Output Symmetry (Input: 50%±5%)		40	50	60	%	3,5
Output Rise Time	t_{OR}		2.0	2.5	ns	8,10
Output Fall Time	t_{OF}		2.0	2.5	ns	8,10
Power-up Time	t_{PU}			100	ms	
Period	Period	Table 2	Table 2	Table 2	ns	

CAPACITANCE

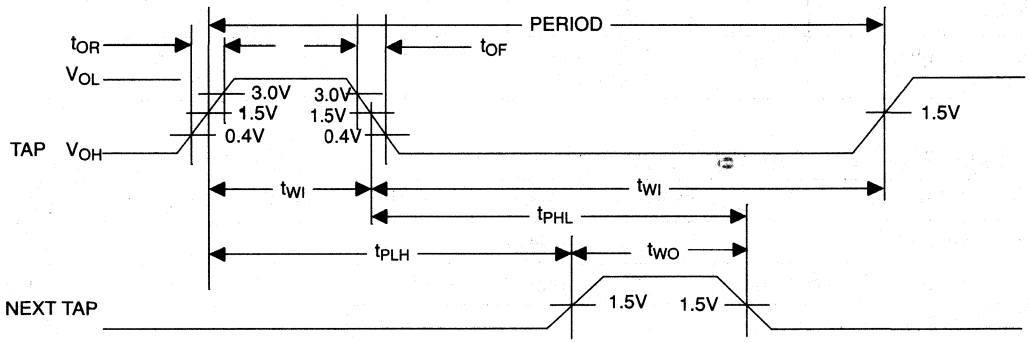
(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	10

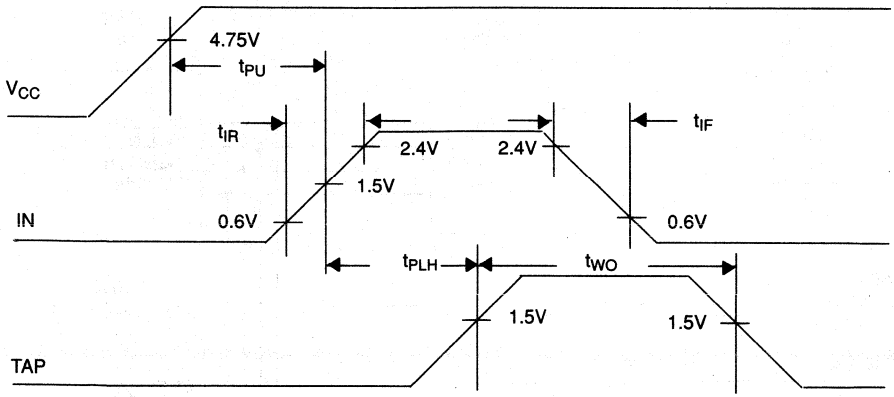
NOTES:

1. All voltages are reference to ground.
2. Measured with outputs open, minimum period.
3. V_{CC} = 5V @ 25°C.
4. Temperature variations from 25°C to 0°C or 70°C may produce an additional tap-to-tap delay shift of ±0.5 ns. Voltage variations from 5.0V to 4.75V or 5.25V produce a worst case tap-to-tap delay shift of 5%.
5. All tap-to-tap delays vary unidirectionally over temperature or voltage range. For example, if the TAP 1 - TAP 2 delay, t_{PLH}, slows down, the TAP2 - TAP 4 delay, t_{PLH}, will also slow down. Since t_{PHL} tracks t_{PLH}, symmetry is preserved.
6. See "Test Conditions" section at the end of this data sheet.
7. Since all four taps have identical output stages, tap-to-tap delays and waveform symmetry will exhibit minimal variation when capacitive loading is increased identically on all taps at the same time (e.g., the addition of one or more RISC coprocessors).
8. V_{CC} = Min; C_L = 30 pF
9. Trailing edge delays, t_{PHL}, are adjusted to maintain waveform symmetry.
10. Guaranteed by design. Periodically tested.

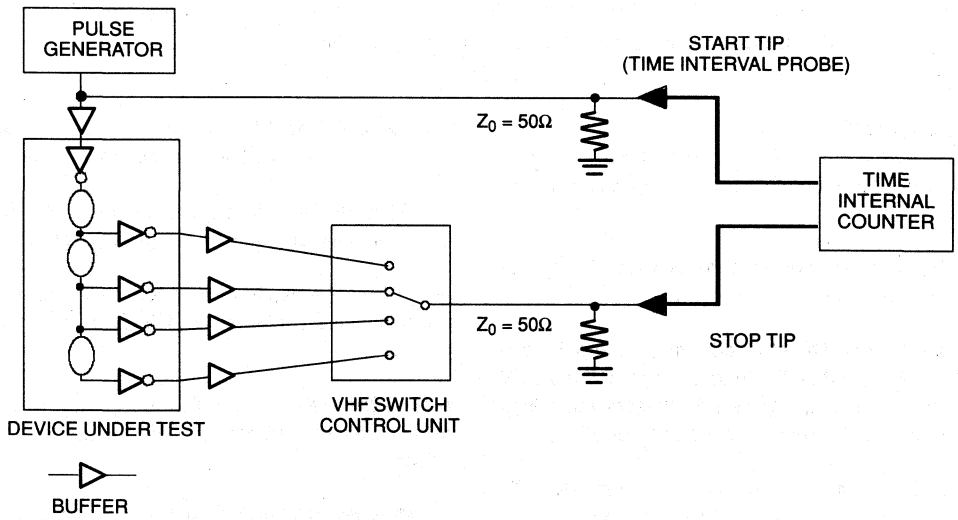
TIMING DIAGRAM - SILICON DELAY LINE Figure 2



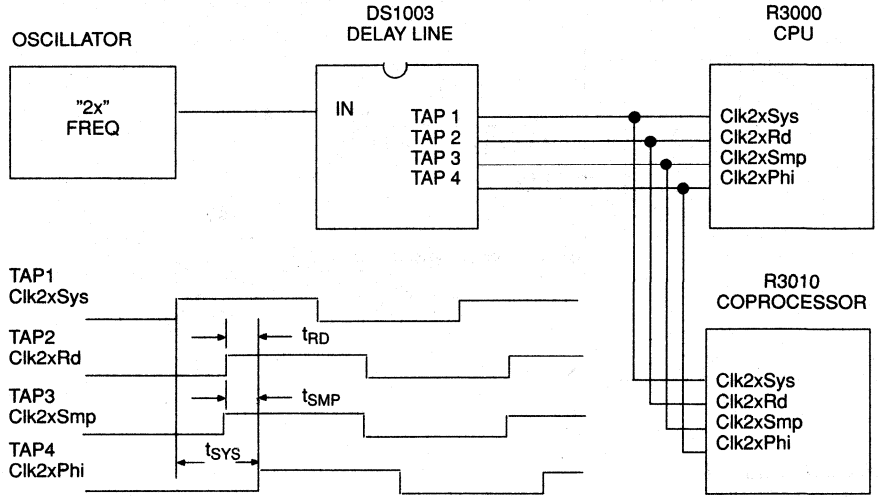
POWER-UP TIMING DIAGRAM Figure 3



TEST CIRCUIT Figure 4



TYPICAL APPLICATION Figure 5



NOTE: TAP 2 can be used for Clk2xSmp with TAP 3 as Clk2xRd.

TERMINOLOGY

Period: The time elapsed between the leading edge of the first trigger pulse and the leading edge of the following pulse.

Symmetry: That percent of the Period when the input or output is above 1.5V.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{IR} (Input Rise Time): The elapsed time between 0.6V and 2.4V on the leading edge of the input pulse.

t_{IF} (Input Fall Time): The elapsed time between 2.4V and 0.6V on the trailing edge of the input pulse.

t_{OR} (Output Rise Rime): The elapsed time between 0.4V and 3.0V on the leading edge of the output pulse.

t_{OF} (Output Fall Time): The elapsed time between 3.0V and 0.4V of the trailing edge output pulse.

t_{PLH} (Time Delay, Rising): Input-to-tap or tap-to-tap delay measured between the 1.5V points on the leading edges.

t_{PHL} (Time Delay, Falling): Input-to-tap or tap-to-tap delay measured between the 1.5V points on the trailing edges.

t_{PU} (Power-up Time): After V_{CC} is valid, the time required before timing specifications are within tolerance.

TEST SETUP DESCRIPTION

Figure 4 illustrates the hardware configuration used for measuring the timing parameters on the DS1003. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution connected between the input and each tap). Each tap is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

Input:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V Low = 0.0V ± 0.1
Source Impedance:	50 ohm max.
Rise and Fall Time:	3.0 ns max. (measured between 0.6V and 2.4)
Pulse Width:	500 ns
Period:	1000 ns

Output:

Each output is loaded with the equivalent of one 74F04 input. Delays are measured at the 1.5V level.

Note:

Above conditions are for test only. The adjusted test limits and guardbands used assure operation to data sheet timing specifications.

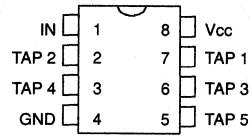
DALLAS SEMICONDUCTOR

DS1004
5-Tap High–Speed Silicon Delay Line

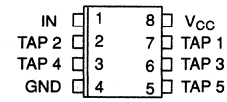
FEATURES

- All–silicon timing circuit
- Five equally delayed clock phases per input
- Precise tap–to–tap delay tolerances of ±0.5, ±0.75, or ±1 ns
- Input–to–tap 1 delay of 5 ns
- Delay tolerances of ±1.5 ns over temperature and voltage
- Leading and trailing edge precision preserves the input symmetry
- CMOS design with TTL compatibility
- Standard 8–pin DIP and 150 mil 8–pin SOIC
- Vapor phasing, IR and wave solderable
- Available in Tape and Reel

PIN ASSIGNMENT



DS1004M 8-PIN DIP
(300 MIL)
See Mech. Drawing
Pg. 480



DS1004Z 8-PIN SOIC
(150 MIL)
See Mech. Drawing
Pg. 483

PIN DESCRIPTION

TAP 1–5	–	TAP Output Number
V_{CC}	–	+5 Volt Supply
GND	–	Ground
IN	–	Input

DESCRIPTION

The DS1004 is a 5–tap all silicon delay line which can provide 2, 3, 4, or 5 ns tap–to–tap delays within a standard part family. The device is Dallas Semiconductor's fastest 5–tap delay line. It is available in a standard 8–pin DIP and 150 mil 8–pin mini–SOIC. The device features precise leading and trailing edge accuracies and has the inherent reliability of an all–silicon delay line solution.

The DS1004 is specified for tap–to–tap tolerances as shown in Table 1. Each device has a minimum input–to–tap 1 delay of 5 ns. Subsequent taps (taps 2 through 5) are precisely delayed by 2, 3, 4, or 5 ns. See Table 1 for details. Tolerance over temperature and voltage is ±1.5 ns. Nominal tap–to–tap tolerances range from ±0.5 ns to ±1.0 ns. Each output is capable of driving up to 10 LS loads.

For customers needing non–standard delay values, the Late Package Program (LPP) is available. Customers may contact Dallas Semiconductor at 214–450–5348 for further details.

PART NUMBER TOLERANCE TABLE Table 1

PART NUMBER	INPUT–TO–TAP		TAP–TO–TAP		
	TOLERANCE NOMINAL	VARIATION OVER TEMP & VOLTAGE	INCREMENT	TOLERANCE NOMINAL	VARIATION OVER TEMP & VOLTAGE
DS1004M–002	5 ± 1.5 ns	±1.5 ns	2 ns	±0.5 ns	±0.75 ns
DS1004M–003	5 ± 1.5 ns	±1.5 ns	3 ns	±0.75 ns	±0.75 ns
DS1004M–004	5 ± 1.5 ns	±1.5 ns	4 ns	±1.0 ns	±0.75 ns
DS1004M–005	5 ± 1.5 ns	±1.5 ns	5 ns	±1.0 ns	±0.75 ns
DS1004Z–002	5 ± 1.5 ns	±1.5 ns	2 ns	±0.5 ns	±0.75 ns
DS1004Z–003	5 ± 1.5 ns	±1.5 ns	3 ns	±0.75 ns	±0.75 ns
DS1004Z–004	5 ± 1.5 ns	±1.5 ns	4 ns	±1.0 ns	±0.75 ns
DS1004Z–005	5 ± 1.5 ns	±1.5 ns	5 ns	±1.0 ns	±0.75 ns

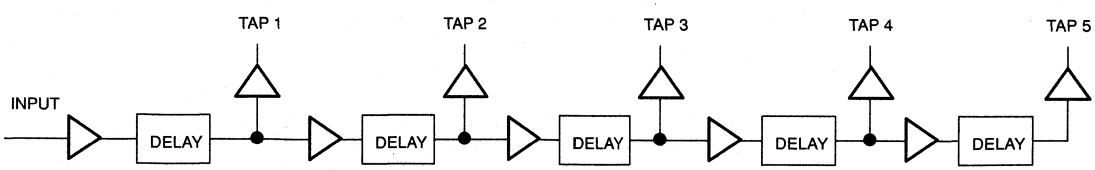
NOTES:

1. Nominal conditions are +25°C and V_{CC}=+5.0 volts.
2. Temperature and voltage variations cover the range from V_{CC}=5.0 volts ± 5% and temperature range from 0°C to +70°C.
3. Delay accuracy for both leading and trailing edges.

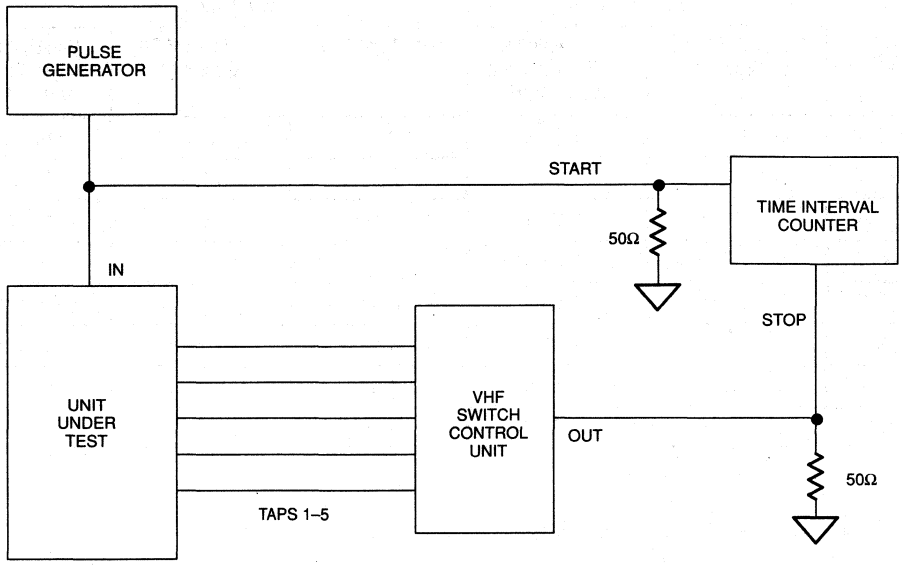
PART NUMBER DELAY TABLE Table 2

PART NUMBER	NOMINAL VALUES (FOR REFERENCE ONLY)				
	INPUT–TO–TAP1	INPUT–TO–TAP2	INPUT–TO–TAP3	INPUT–TO–TAP 4	INPUT–TO–TAP 5
DS1004M–002	5 ns	7 ns	9 ns	11 ns	13 ns
DS1004M–003	5 ns	8 ns	11 ns	14 ns	17 ns
DS1004M–004	5 ns	9 ns	13 ns	17 ns	21 ns
DS1004M–005	5 ns	10 ns	15 ns	20 ns	25 ns
DS1004Z–002	5 ns	7 ns	9 ns	11 ns	13 ns
DS1004Z–003	5 ns	8 ns	11 ns	14 ns	17 ns
DS1004Z–004	5 ns	9 ns	13 ns	17 ns	21 ns
DS1004Z–005	5 ns	10 ns	15 ns	20 ns	25 ns

LOGIC DIAGRAM



DS1004 TEST CIRCUIT Figure 1



TEST SETUP DESCRIPTION

Figure 1 illustrates the hardware configuration used for measuring the timing parameters of the DS1004. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected to the output. The DS1004 output taps are selected and connected to the interval counter by a VHF switch control unit. All measurements are fully automated with each instrument controlled by the computer over an IEEE 488 bus.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
Active Current	I_{CC}	V_{CC}=5.25V PERIOD=1 µs		35	75	mA	
High Level Input Voltage	V_{IH}		2.2		V_{CC} + 0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage	I_I	0.0V ≤ V_I ≤ V_{CC}	-1.0		1.0	µA	
High Level Output Current	I_{OH}	V_{CC}=4.75V V_{OH} = 4V			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC}=4.75V V_{OL} = 0.5V	12			mA	

AC ELECTRICAL CHARACTERISTICS

(T_A = 25°C; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Period	t_{PERIOD}	4 (t_{WI})			ns	3
Input Pulse Width	t_{WI}	40% of tap 5 t_{PLH}			ns	3
Input to Tap 1 Output Delay	t_{PLH}, t_{PHL}		Table 1		ns	2
Tap–to–Tap Delays	t_{PLH}		Table 1		ns	2
Output Rise or Fall Time	t_{OR}, t_{OF}		2.0	2.5	ns	
Power-up Time	t_{PU}			100	ms	

CAPACITANCE

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	

NOTES:

1. All voltages are referenced to ground.
2. V_{CC}=5 volts and 25°C. Delay accuracy on both the rising and falling edges within tolerances given in Table 1.
3. Pulse width and duty cycle specifications may be exceeded, however, accuracy will be application sensitive with respect to decoupling, layout, etc.

TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50 ohm max.
Rise and Fall Time:	3.0 ns max. (measured between 0.6V and 2.4V)
Pulse Width:	500 ns
Pulse Period:	1 µs
Output Load Capacitance:	15 pF

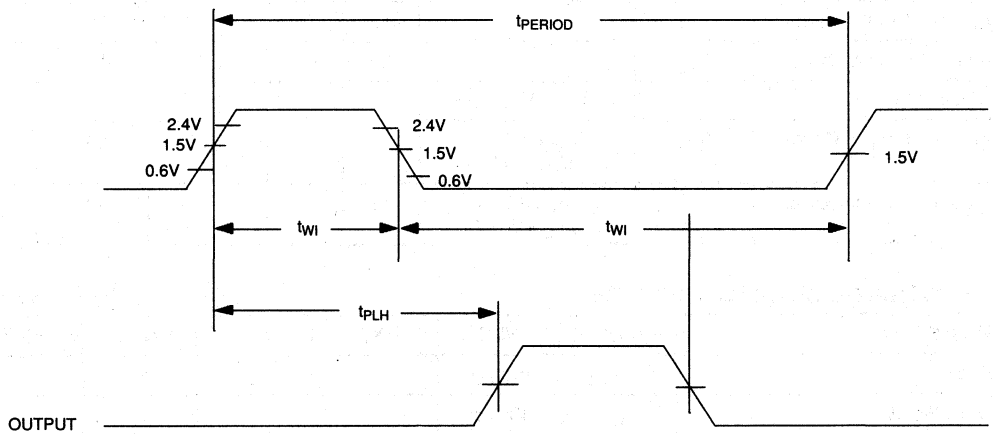
OUTPUT:

Each output is loaded with the equivalent of one 74F04 input gate. Data is measured at the 1.5V level on the rising and falling edge.

NOTE:

Above conditions are for test only and do not restrict the devices under other data sheet conditions.

TIMING DIAGRAM: DS1004 INPUT TO OUTPUTS



TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of the output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the falling edge of the input pulse and the 1.5V point on the falling edge of the output pulse.

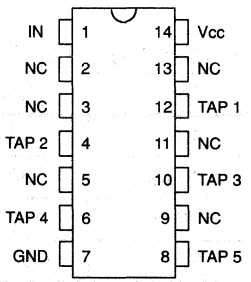
DALLAS SEMICONDUCTOR

DS1005
5-Tap Silicon Delay Line

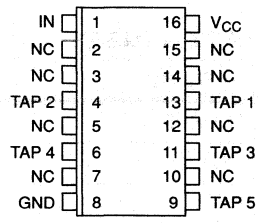
FEATURES

- All-silicon time delay
- 5 taps equally spaced
- Delay tolerance ±2 ns or ±3%, whichever is greater
- Stable and precise over temperature and voltage range
- Leading and trailing edge accuracy
- Economical
- Auto-insertable, low profile
- Standard 14-pin DIP, 8-pin DIP, or 16-pin SOIC
- Tape and reel available for surface-mount
- Low-power CMOS
- TTL/CMOS compatible
- Vapor phase, IR and wave solderability
- Custom delays available
- Quick turn prototypes
- Extended temperature range available

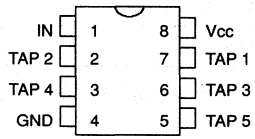
PIN ASSIGNMENT



DS1005 14-PIN DIP (300 MIL)
DS1005G 14-PIN GULLWING (300 MIL)
DS1005K 14-PIN SHEARED NC
See Mech. Drawings
Pgs. 480 & 491



DS1005S 16-PIN SOIC
(300 MIL)
See Mech. Drawing
Pg. 484



DS1005M 8-PIN DIP (300 MIL)
DS1005H 8-PIN GULLWING (300 MIL)
See Mech. Drawings
Pgs. 480 & 491

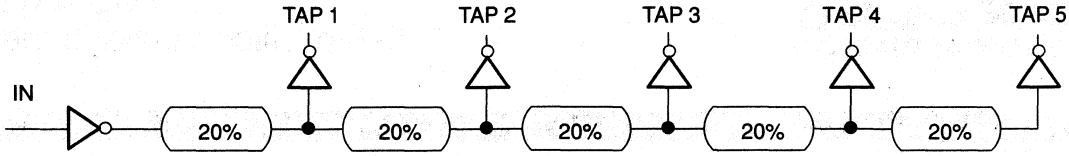
PIN DESCRIPTION

TAP 1 – TAP 5	–	TAP Output Number
V_{CC}	–	+5 Volts
GND	–	Ground
NC	–	No Connection
IN	–	Input

DESCRIPTION

The DS1005 5-Tap Silicon Delay Line provides five equally spaced taps with delays ranging from 12 ns to 250 ns, with an accuracy of ±2 ns or ±3%, whichever is greater. This device is offered in a standard 14-pin DIP making it compatible with existing delay line products. Space-saving 8-pin DIPs and 16-pin SOICs are also available. The 14-pin DIP and 8-pin DIP are available in a surface mountable gullwing construction. Both enhanced performance and superior reliability over hybrid technology is achieved by the combination of a 100% silicon delay line and industry standard DIP and SOIC packaging. In order to maintain complete pin compatibility, DIP packages are available with hybrid lead configurations. The DS1005 reproduces the input logic level at each tap after the fixed delay specified by the dash number in Table 1. The device is designed with both leading and trailing edge accuracy. Each tap is capable of driving up to ten 74LS loads. Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450-5348.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PHL}, t_{PLH}) Table 1

PART NO.	TAP 1	TAP 2	TAP 3	TAP 4	TAP 5
DS1005-60	12 ns	24 ns	36 ns	48 ns	60 ns
DS1005-75	15 ns	30 ns	45 ns	60 ns	75 ns
DS1005-100	20 ns	40 ns	60 ns	80 ns	100 ns
DS1005-125	25 ns	50 ns	75 ns	100 ns	125 ns
DS1005-150	30 ns	60 ns	90 ns	120 ns	150 ns
DS1005-175	35 ns	70 ns	105 ns	140 ns	175 ns
DS1005-200	40 ns	80 ns	120 ns	160 ns	200 ns
DS1005-250	50 ns	100 ns	150 ns	200 ns	250 ns

Custom delays available

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	TEST COND.	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC}+0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	u A	
Active Current	I_{CC}	V_{CC} = Max; Period = Min.		40	70	mA	2
High Level Output Current	I_{OH}	V_{CC} = Min. V_{OH} = 4			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC} = Min. V_{OL} = 0.5	12			mA	

AC ELECTRICAL CHARACTERISTICS

(T_A = 25°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}	40% of TAP 5 t_{PLH}			ns	7
Input to Tap Delay (leading edge)	t_{PLH}		Table 1		ns	3,4,5,6
Input to Tap Delay (trailing edge)	t_{PHL}		Table 1		ns	3,4,5,6
Power-up Time	t_{PU}			100	ms	
	Period	4 (t_{WI})			ns	7

CAPACITANCE

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. V_{CC} = 5V @ 25°C. Delays accurate on both rising and falling edges within ±2 ns or ±3%, whichever is greater.
4. See Test Conditions.
5. The combination of temperature variations from 25°C to 0°C or 25°C to 70°C and voltage variations from 5.0V to 4.75V or 5.0V to 5.25V may produce an additional input-to-tap delay shift of ±1.5 ns or ±4%, whichever is greater.
6. All tap delays tend to vary unidirectionally with temperature or voltage. For example, if TAP 1 slows down, all other taps will also slow down; TAP 3 can never be faster than TAP 2.
7. Pulse width and duty cycle specifications may be exceeded; however, accuracy will be application-sensitive (decoupling, layout, etc.).

TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any tap output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any tap output pulse.

TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1005. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each tap. Each tap is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature	25°C ± 3°C
Supply Voltage (V_{CC})	5.0V ± 0.1V
Input Pulse	High = 3.0V ± 0.1V Low = 0.0V ± 0.1V
Source Impedance	50 ohm maximum
Rise and Fall Time	3.0 ns maximum
Pulse Width	500 ns
Period	1 µs

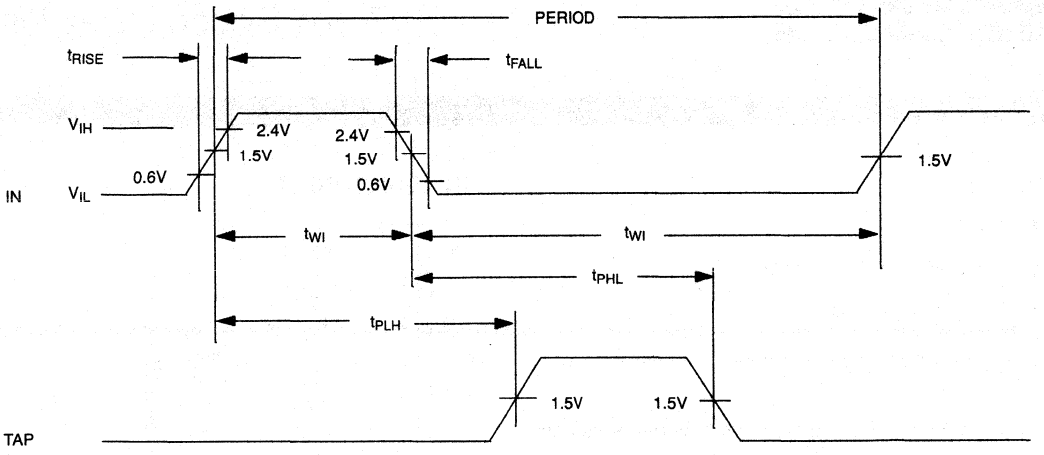
OUTPUT:

Each output is loaded with the equivalent of a 74F04 input gate. Delay is measured at the 1.5V level on the rising and falling edge.

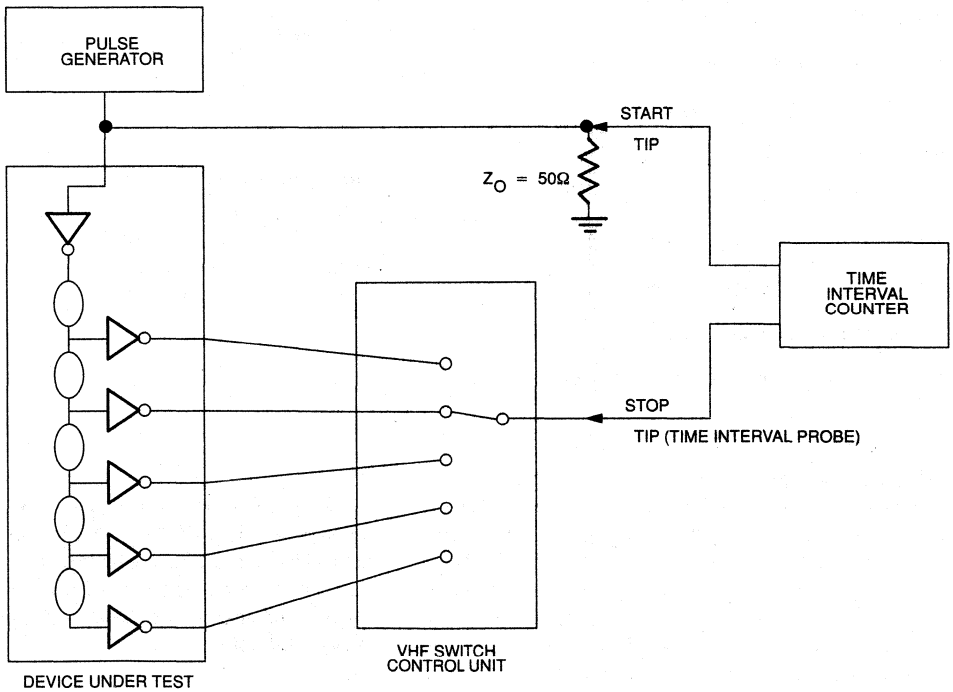
NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

TIMING DIAGRAM-SILICON DELAY LINE Figure 2



DALLAS SEMICONDUCTOR TEST CIRCUIT Figure 3



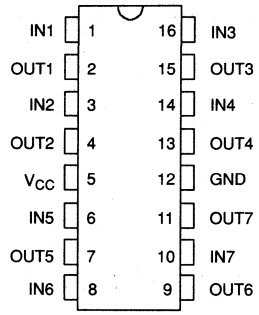
DALLAS SEMICONDUCTOR

DS1007
7-in-1 Silicon Delay Line

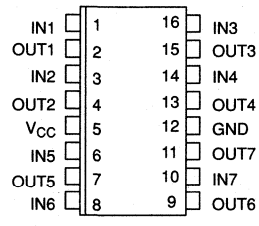
FEATURES

- All-silicon time delay
- 7 independent buffered delays
- Delay tolerance ±2 ns
- Four delays can be custom set between 3 ns and 10 ns
- Three delays can be custom set between 9 ns and 40 ns
- Delays are stable and precise
- Economical
- Auto-insertable, low profile
- Surface mount 16-pin SOIC
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom specifications available
- Quick turn prototypes
- Extended temperature range available

PIN ASSIGNMENT



DS1007 16-PIN DIP (300 MIL)
See Mech. Drawing
Pg. 480



DS1007S 16-PIN SOIC
(300 MIL)
See Mech. Drawing
Pg. 484

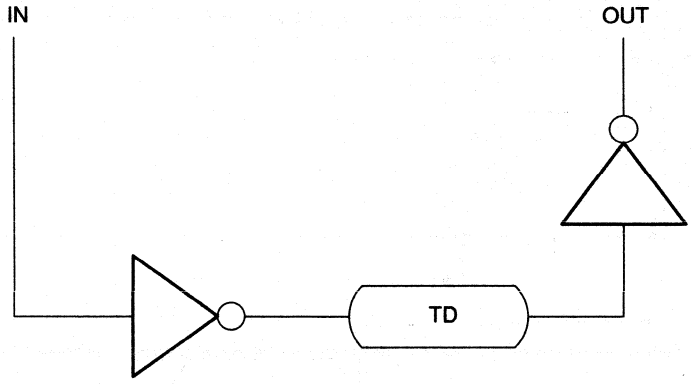
PIN DESCRIPTION

IN1 - IN7	–	Inputs
Out1 - Out7	–	Outputs
GND	–	Ground
V_{CC}	–	+5 Volts

DESCRIPTION

The DS1007 7-in-1 Silicon Delay Line provides seven independent delay times which are set by Dallas Semiconductor to the customer's specification. The delay times can be set from 3 ns to 40 ns with an accuracy of ±2 ns at room temperature. The device is offered in both a 16-pin DIP and a 16-pin SOIC. Since the DS1007 is an all-silicon solution, better economy and reliability are achieved when compared to older methods using hybrid technology. The DS1007 reproduces the input logic state at the output after the fixed delay. Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450-5348.

LOGIC DIAGRAM Figure 1



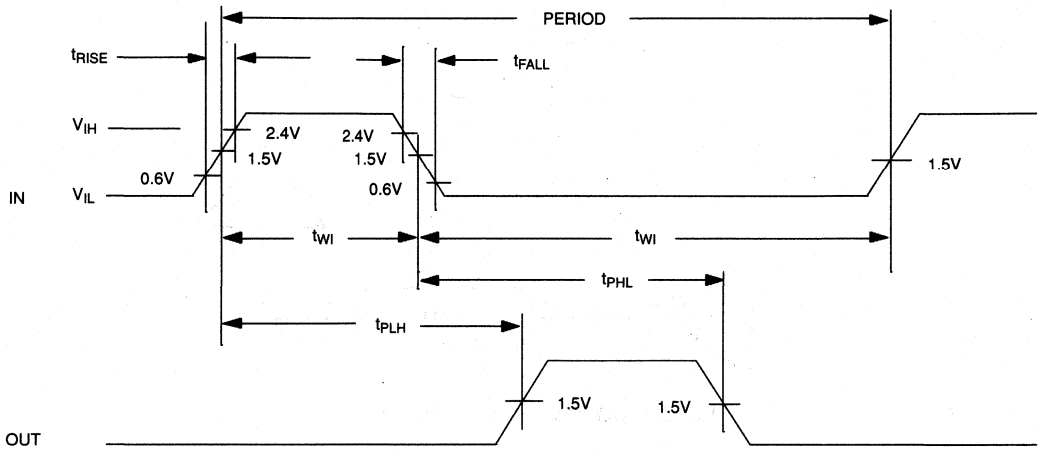
PULSE WIDTH > 100% OF DELAY

PART NUMBER DELAY TABLE (t_{PLH}) Table 1

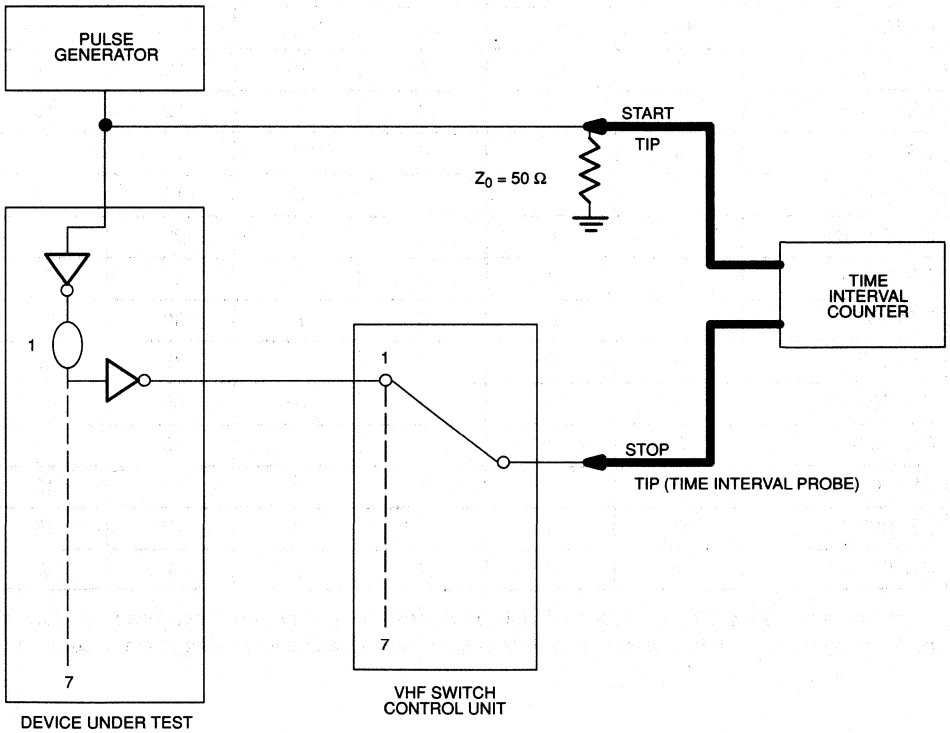
PART #	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	OUT7
DS1007-1	3ns	4ns	5ns	6ns	9ns	13ns	18ns
DS1007-2	4	6	8	10	12	14	16
DS1007-3	3	3	3	3	10	10	10
DS1007-4	4	4	4	4	12	12	12
DS1007-5	5	5	5	5	15	15	15
DS1007-6	6	6	6	6	20	20	20
DS1007-7	7	7	7	7	25	25	25
DS1007-8	8	8	8	8	30	30	30
DS1007-9	9	9	9	9	35	35	35
DS1007-10	10	10	10	10	40	40	40
DS1007-11	3	4	6	8	10	12	14
DS1007-12	3	4	6	8	10	15	20
DS1007-13	3	4	6	8	12	15	20
DS1007-14	7	7	7	7	9	9	9

Custom delays available. Out 1 through Out 4 can be custom set from 3 to 10ns. (Leading edge only accuracy.) Out 5 through Out 7 can be custom set from 9 to 40ns. (Both leading and trailing edge accuracy.)

TIMING DIAGRAM SILICON DELAY LINE Figure 2



TEST CIRCUIT Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC}+0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	uA	
Active Current	I_{CC}	V_{CC}= Max; Period= Min.		40.0	70.0	mA	2
High Level Output Current	I_{OH}	V_{CC}= Min. V_{OH}= 2.4V			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC}= Min. V_{OL}= 0.5V	12.0			mA	

AC ELECTRICAL CHARACTERISTICS

(T_A= 25°C; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}	100% of t_{PLH}			ns	
Input to Output (leading edge)	t_{PLH}		Table 1		ns	3, 4, 5
Power-up Time	t_{PU}			100	ms	7
	Period	3 (t_{WI})			ns	6

CAPACITANCE

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. V_{CC} = 5V @25°C. Delays accurate on rising edges within ±2 ns.
4. See Test Conditions below.
5. All output delays in the same speed output tend to vary unidirectionally with temperature or voltage range (i.e., if OUT 2 slows down, all other outputs also slow down).
6. Period specifications may be exceeded; however, accuracy will be application-sensitive (decoupling, layout, etc.).
7. t_{PU} = 0 ms for OUT 1 through OUT 4.

TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge, and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of the corresponding output pulse.

TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1007. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each output. Each output is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50 ohm Max.
Rise and Fall Time:	3.0 ns Max.
Pulse Width:	500 ns
Period:	1 µs

OUTPUT:

Each output is loaded with the equivalent of one 74F04 input gate. Delay is measured at the 1.5V level on the rising edge.

NOTE:

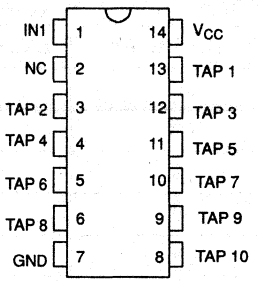
Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

DALLAS SEMICONDUCTOR

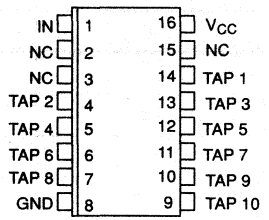
DS1010
10-Tap Silicon Delay Line

FEATURES
- All-silicon time delay
- 10 taps equally spaced
- Delays are stable and precise
- Leading and trailing edge accuracy
- Delay tolerance ±5% or ±2 ns, whichever is greater
- Economical
- Auto-insertable, low profile
- Standard 14-pin DIP or 16-pin SOIC
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom delays available
- Fast turn prototypes
- Extended temperature range available

PIN ASSIGNMENT



DS1010 14-PIN DIP
(300 MIL)
DS1010G 14-PIN GULLWING
(300 MIL)
See Mech. Drawings
Pgs. 480 & 491



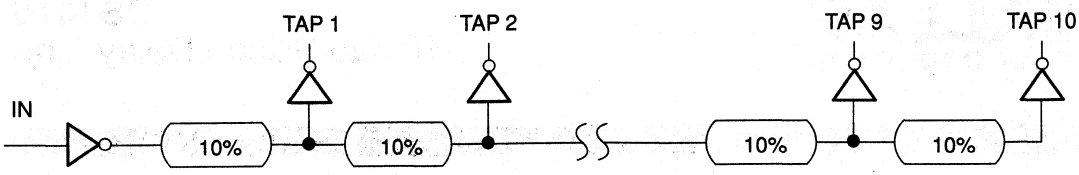
DS1010S 16-PIN SOIC
(300 MIL)
See Mech. Drawing
Pg. 484

PIN DESCRIPTION

TAP 1-TAP 10	–	TAP Output Number
V_{CC}	–	5 Volts
GND	–	Ground
NC	–	No Connection
IN	–	Input

DESCRIPTION
The DS1010 series delay line has ten equally spaced taps providing delays from 5 ns to 500 ns. The devices are offered in a standard 14-pin DIP which is pin-compatible with hybrid delay lines. Alternatively, a 16-pin SOIC is available for surface mount technology which reduces PC board area. Since the DS1010 is an all-silicon solution, better economy is achieved when compared to older methods using hybrid techniques. The DS1010 series delay lines provide a nominal accuracy of ±5% or ±2 ns, whichever is greater. The DS1010 reproduces the input logic state at the TAP 10 output after a fixed delay as specified by the dash number extension of the part number. The DS1010 is designed to produce both leading and trailing edge with equal precision. Each tap is capable of driving up to ten 74LS type loads. Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450-5348.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PHL}, t_{PLH}) Table 1

CATALOG P/N	TOTAL DELAY	DELAY/TAP (ns)
DS1010-50	50	5
DS1010-60	60	6
DS1010-75	75	7.5
DS1010-80	80	8
DS1010-100	100	10
DS1010-125	125	12.5
DS1010-150	150	15
DS1010-175	175	17.5
DS1010-200	200	20
DS1010-250	250	25
DS1010-300	300	30
DS1010-350	350	35
DS1010-400	400	40
DS1010-450	450	45
DS1010-500	500	50

Custom delays available.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	TEST COND.	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC}+0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	µA	
Active Current	I_{CC}	V_{CC}=Max: Period=Min.		40	150	mA	2
High Level Output Current	I_{OH}	V_{CC}=Min. V_{OH}=4			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC}=Min. V_{OL}=0.5	12			mA	

AC ELECTRICAL CHARACTERISTICS

(T_A = 25°C; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}	40% of TAP 10 t_{PLH}			ns	8
Input to Tap Delay (leading edge)	t_{PLH}		Table 1		ns	3,4,5,6,7,9
Input to Tap Delay (trailing edge)	t_{PHL}		Table 1		ns	3,4,5,6,7,9
Power-up Time	t_{PU}			100	ms	
	Period	$4(t_{WI})$			ns	8

CAPACITANCE

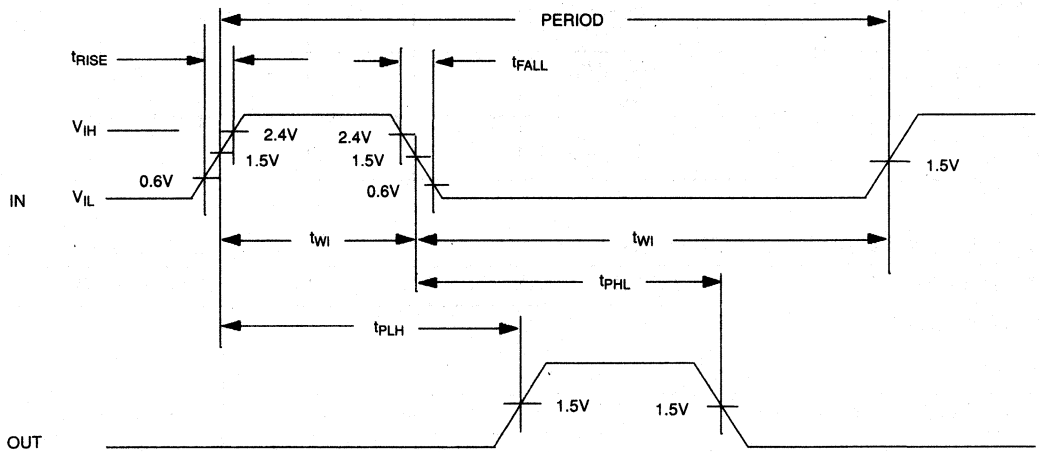
(T_A= 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

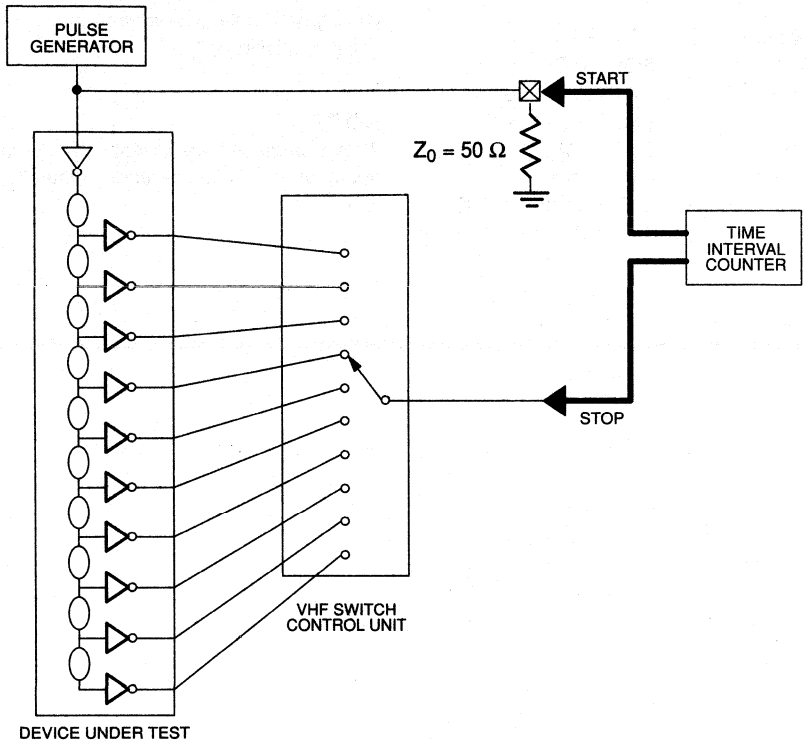
NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. V_{CC}= 5V @ 25°C. Input-to-tap delays accurate on both rising and falling edges within ±2 ns or ±5% whichever is greater.
4. See "Test Conditions" section.
5. For DS1010 delay lines with a TAP 10 delay of 100 ns or greater, temperature variations from 25°C to 0°C or 70°C may produce an additional input-to-tap delay shift of ±2ns or ±3%, whichever is greater.
6. For DS1010 delay lines with a TAP 10 delay less than 100 ns, temperature variations from 25°C to 0°C or 70°C may produce an additional input-to-tap delay shift of ±1 ns or ±9%, whichever is greater.
7. All tap delays tend to vary unidirectionally with temperature or voltage changes. For example, if TAP 1 slows down, all other taps will also slow dow; TAP 3 can never be faster than TAP 2.
8. Pulse width and period specifications may be exceeded; however, accuracy will be application-sensitive (de-coupling, layout, etc.).
9. Certain high-frequency applications not recommended for -50 in 16-pin package. Consult factory.

TIMING DIAGRAM-SILICON DELAY LINE Figure 2



TEST CIRCUIT Figure 3



TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any tap output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any tap output pulse.

TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1010. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each tap. Each tap is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50 ohm Max.
Rise and Fall Time:	3.0 ns Max.
Pulse Width:	500 ns (1 µs for -500)
Period:	1 µs (2 µs for -500)

OUTPUT:

Each output is loaded with the equivalent of one 74FO4 input gate. Delay is measured at the 1.5V level on the rising and falling edge.

NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

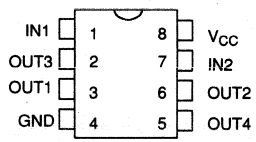
DALLAS SEMICONDUCTOR

DS1012
2-in-1 Sub-Miniature Silicon Delay Line with Logic

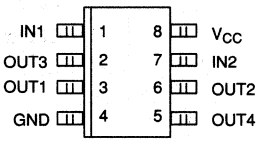
FEATURES

- All-silicon time delay
- 53 µW max. CMOS quiescent mode
- Surface mount 8-pin mini-SOIC and standard 8-pin DIP
- 2 independent buffered delays per input
- Option of complemented output(s)
- Option of timed AND, NAND, OR, NOR, XOR, XNOR, HALF-XOR and HALF-XNOR logic outputs
- Delay tolerance: ±1.5 ns (delays: 3-10 ns), ±2.0 ns (delays: 11-40 ns)
- Vapor phase, IR and wave solderability
- Economical
- TTL/CMOS-compatible
- Quick turn prototypes
- Custom delays and logic options available

PIN ASSIGNMENT



DS1012M 8-PIN DIP (300 MIL)
DS1012H 8-PIN GULLWING
See Mech. Drawing – Pgs. 480 & 491



DS1012Z 8-PIN SOIC (150 MIL)
See Mech. Drawing – Pg. 483

PIN DESCRIPTION

IN1, IN2	–	Inputs
OUT1, OUT2	–	Outputs (delays)
OUT3, OUT4	–	Outputs (delays, logic)
GND	–	Ground
V_{CC}	–	+5 Volts

DESCRIPTION

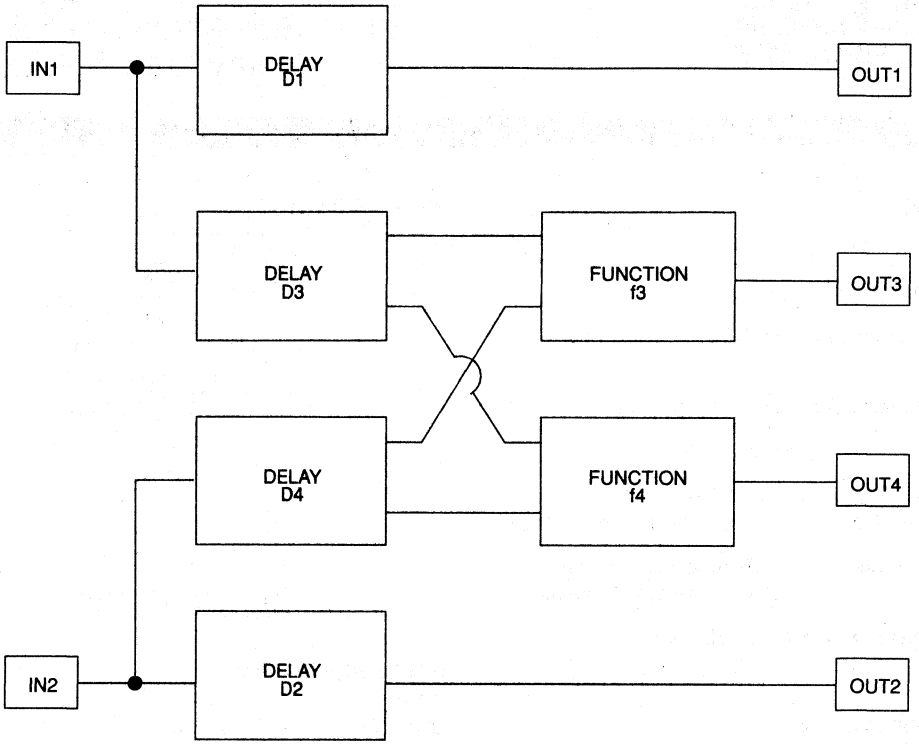
In its most simple configuration, the DS1012 2-in-1 Sub-Miniature Silicon Delay Line Chip provides two inputs, each of which in turn provides independent delays to a pair of outputs. Any of the four outputs can be inverted at the time of manufacture. The DS1012-1 and DS1012-3 are examples of catalog parts having this basic configuration.

For applications requiring two-input timed logic functions, at the time of manufacture the simple delay on OUT4 can be replaced by one of the following: OR, NOR, XOR, or XNOR. Similarly, a timed AND, NAND, HALF-XOR (D3 AND $\overline{D4}$), or NOT HALF-XOR ($\overline{D3}$ OR D4) can be substituted for the simple delay on OUT3. DS1012-2, DS1012-4, and DS1012-5 are examples of catalog parts configured with logic functions on OUT3 and OUT4. Note that DS1012-2 also utilizes an output inversion on OUT2.

In any configuration, delays D1 (t_{D1}) and D2 (t_{D2}) can be specified within the range of ~3 ns to 10 ns. Delays D3 (t_{D3}) and D4 (t_{D4}) can be specified to have values between ~3 ns and 40 ns. The worst case leading edge delay accuracy at nominal voltage and room temperature is ±2 ns. The DS1012 is offered in two packages: an 8-pin DIP and an 8-pin 150 mil wide mini-SOIC.

Dallas Semiconductor offers the DS1012 in a wide variety of custom delay and logic configurations. For special requests and quick turn delivery, call (214) 450-5348.

LOGIC DIAGRAM Figure 1



Function f3 can be one of the following:

D3	$\overline{D3}$
D3 AND D4	D3 NAND D4
D3 HALF-XOR D4	D3 HALF-XNOR D4

Function f4 can be one of the following:

D4	$\overline{D4}$
D3 OR D4	D3 NOR D4
D3 XOR D4	D3 XNOR D4

NOTE: Any output(s) can be inverted at time of manufacture.
If D1 > 10 ns, D1 = D3.
If D2 > 10 ns, D2 = D4.

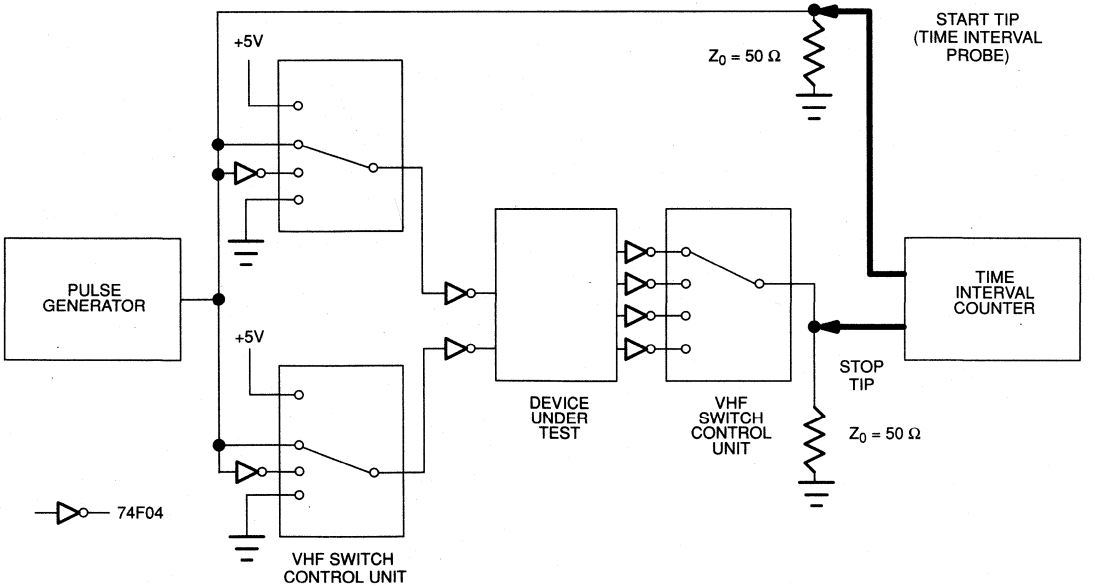
PART NUMBER DELAY AND CONFIGURATION Table 1

CATALOG P/N	t_{D1} (ns)	t_{D2} (ns)	t_{D3} (ns)	t_{D4} (ns)	OUT1	OUT2	OUT3	OUT4
DS1012-1	5	5	10	10	D1	D2	D3	D4
DS1012-2	5	5	10	10	D1	$\overline{D2}$	D3.D4	D3+D4
DS1012-3	3	7	10	40	D1	D2	D3	D4
DS1012-4	5	5	25	25	D1	D2	D3HXD4	D3XD4
DS1012-5	10	10	5	5	D1	D2	D3.D4	D3+D4
DS1012-7	15	4	4	14	D1	$\overline{D2}$	D3	D3XD4
DS1012–9	5	25	5	25	D1	D2	$\overline{D3HXD4}$	D3XD4
DS1012-D16	4	19.6	4	19.6	D1	D2	$\overline{D3.D4}$	D3XD4
DS1012-D20	4	16.5	4	16.5	D1	D2	$\overline{D3.D4}$	D3XD4
DS1012-D25	4	14	4	14	D1	D2	$\overline{D3.D4}$	D3XD4
DS1012-D33	4	11.5	4	11.5	D1	D2	$\overline{D3.D4}$	D3XD4
DS1012-D50	4	9	4	9	D1	D2	$\overline{D3.D4}$	D3XD4
DS1012-V20	25	50	25	50	D1	D2	$\overline{D3.D4}$	$\overline{D3+D4}$
DS1012-V40	12.5	25	12.5	25	D1	D2	$\overline{D3.D4}$	D3XD4
DS1012-V50	10	20	10	20	D1	D2	$\overline{D3.D4}$	D3XD4
DS1012-V60	8.3	8.3	8.3	8.3	D1	D2	$\overline{D3.D4}$	$\overline{D3+D4}$

NOTE: . = AND, + = OR, X = XOR, HX = HALF–XOR

Contact Dallas Semiconductor for information on custom configurations and timing delays.

TEST CIRCUIT Figure 2



TEST SETUP DESCRIPTION

Figure 2 illustrates the hardware configuration used for measuring the timing parameters on the DS1012. The input waveform is produced by a precision pulse generator under software control connected to the inputs by VHF switch control units. Time delays are measured by a time interval counter (20 ps resolution) connected between the inputs and the outputs. Outputs are connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50 ohms max.
Rise and Fall Time:	3.0 ns max.
Pulse Width:	50 ns
Period:	100 ns

OUTPUT:
Each output is loaded with a 74F04. Delay is measured between the 1.5V level of the rising edge of the input signal and the 1.5V level of the corresponding edge of the output.

NOTE: These conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	TEST	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC}+0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	µA	
Active Current	I_{CC1}	V_{CC} = MAX; PERIOD = MIN		40.0	70.0	mA	2
Quiescent Current	I_{CC2}	V_{CC} = MAX.			10	µA	5
High Level Output Current	I_{OH}	V_{CC} = MIN V_{OH} = 2.4V			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC} = MIN. V_{OL} = 0.5V	8.0			mA	

AC ELECTRICAL CHARACTERISTICS

(T_A = 25°C; V_{CC} = 5V ± 5%)

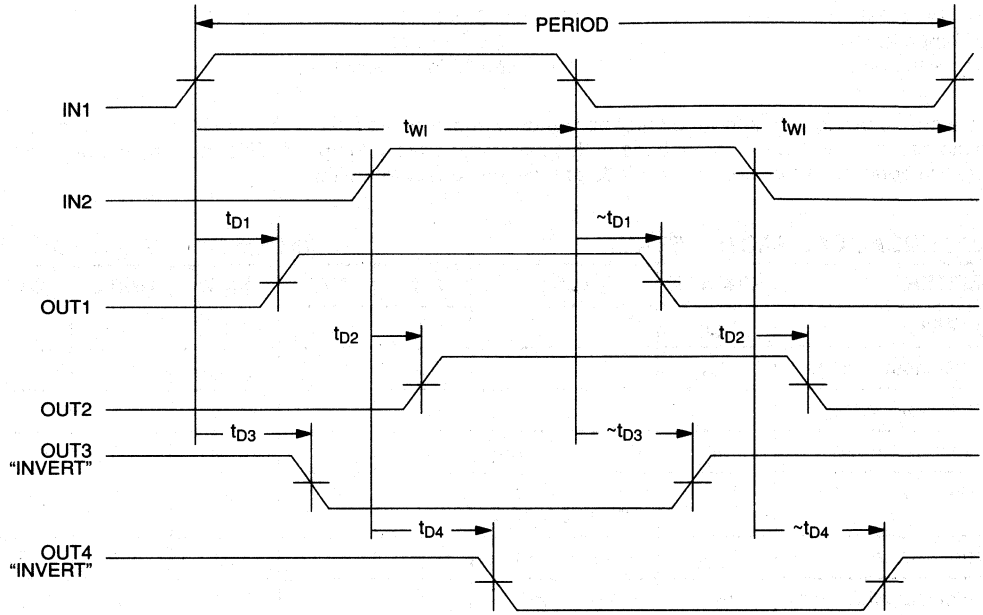
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}				ns	6
Input to Output (leading edge)	t_{D1}, t_{D2}, t_{D3}, t_{D4}				ns	3, 4
Power-up Time	t_{PU}			0	ns	7
	Period	2(t_{WI})			ns	

CAPACITANCE

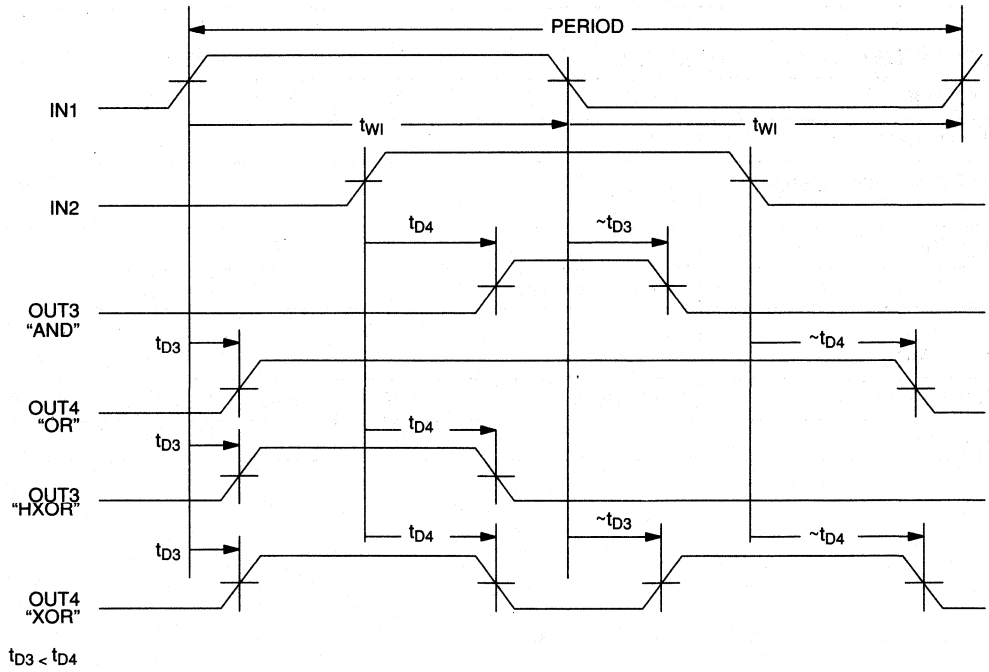
(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

DELAY FUNCTION Figure 3



LOGIC FUNCTIONS Figure 4



$t_{D3} < t_{D4}$

NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open, minimum period. I_{CC1} (max.) for any value of Period can be calculated using the formula:

   I_{CC1} (max.) in mA = 840 mA-ns/Period (in ns) + I_{CC2} in mA

   Example: If Period = 50 ns then

   ICC1 (Max) in mA = 840 mA-ns/50 ns + 0.01 mA = 16.81 mA
3. V_{CC} = 5V @ 25°C. Delays referenced to leading (input rising) edges are accurate within ±1.5 ns for values between 3 to 10 ns and ±2 ns for values between 11 to 40 ns. Delays referenced to trailing (input falling) edges will typically equal the corresponding leading edge delay within ±1 ns.
4. See the section entitled "Test Conditions."
5. For the quiescent mode, both inputs must meet the conditions
   $0.3V > V_I$ or $VI > V_{CC} - 0.3$
6. For specified accuracy, t_{WI} (min) is the longer of $3(t_{D1})$, $3(t_{D2})$, $3(t_{D3})$, or $3(t_{D4})$. Pulse doublers designed for single frequency use will meet specified accuracies at 50% duty cycle; i.e., $2(t_{WI})$ = 1/FREQ = PERIOD. Customs will be adjusted to be accurate at customer input width specifications when t_{WI} is longer than t_{D1}, t_{D2}, t_{D3}, and t_{D4}.
7. On power-up, the DS1012 will supply timing and logic functions with specified accuracy as soon as V_{CC} achieves nominal value.

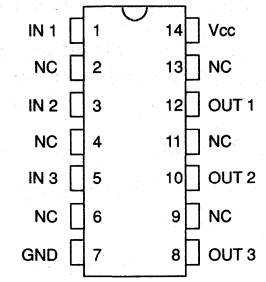
DALLAS SEMICONDUCTOR

DS1013
3-in-1 Silicon Delay Line

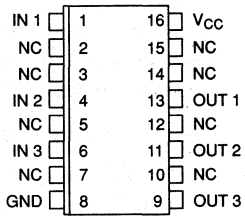
FEATURES

- All-silicon time delay
- 3 independent buffered delays
- Delay tolerance ±2ns for -10 through -65
- Stable and precise over temperature and voltage range
- Leading and trailing edge accuracy
- Economical
- Auto-insertable, low profile
- Standard 14-pin DIP, 8-pin DIP, or 16-pin SOIC
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom delays available
- Quick turn prototypes
- Extended temperature ranges available

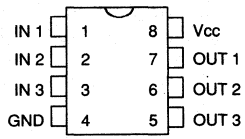
PIN ASSIGNMENT



DS1013 14-PIN DIP (300 MIL)
DS1013G 14-PIN GULLWING (300 MIL)
DS1013K 14-PIN SHEARED NC
See Mech. Drawings
Pgs. 480 & 491



DS1013S 16-PIN SOIC
(300 MIL)
See Mech. Drawing
Pg. 484



DS1013M 8-PIN DIP (300 MIL)
DS1013H 8-PIN GULLWING (300 MIL)
See Mech. Drawings
Pgs. 480 & 491

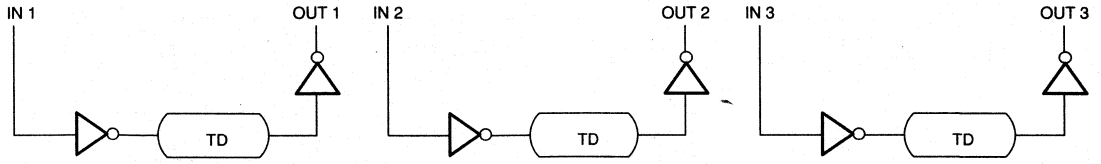
PIN DESCRIPTION

IN 1, IN 2, IN 3	– Inputs
OUT 1, OUT 2, OUT 3	– Outputs
GND	– Ground
V_{CC}	– +5 Volts
NC	– No Connection

DESCRIPTION

The DS1013 series of delay lines has three independent logic buffered delays in a single package. The devices are offered in a standard 14-pin DIP which is pin-compatible with hybrid delay lines. Alternative 8-pin DIP and surface mount packages are available which save PC board area. Since the DS1013 products are an all silicon solution, better economy is achieved when compared to older methods using hybrid techniques. The DS1013 series delay lines provide a nominal accuracy of ±2ns for delay times ranging from 10 ns to 65 ns, increasing to 5% for delays of 150 ns. The DS1013 delay line reproduces the input logic state at the output after a fixed delay as specified by the dash number extension of the part number. The DS1013 is designed to reproduce both leading and trailing edges with equal precision. Each output is capable of driving up to ten 74LS loads. Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450-5348.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PHL}, t_{PLH},) Table 1

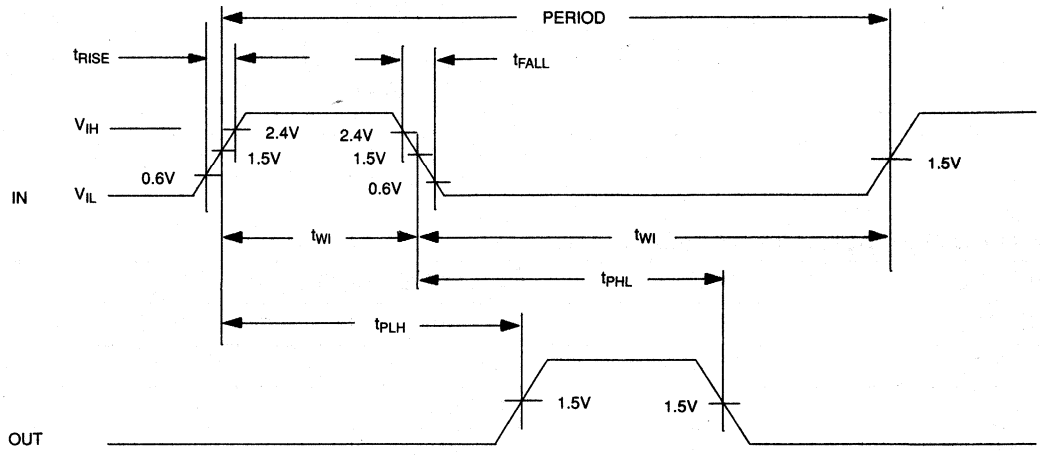
PART NO.	DELAY PER OUTPUT (ns)
DS1013-10	10/10/10
DS1013-12	12/12/12
DS1013-15	15/15/15
DS1013-20	20/20/20
DS1013-25	25/25/25
DS1013-30	30/30/30
DS1013-35	35/35/35
DS1013-40	40/40/40
DS1013-45	45/45/45
DS1013-50	50/50/50
DS1013-55	55/55/55
DS1013-60	60/60/60
DS1013-65	65/65/65
DS1013-70*	70/70/70
DS1013-75*	75/75/75
DS1013-80*	80/80/80
DS1013-90*	90/90/90
DS1013-100*	100/100/100
DS1013-150**	150/150/150
DS1013–200**	200/200/200

Custom delays available.

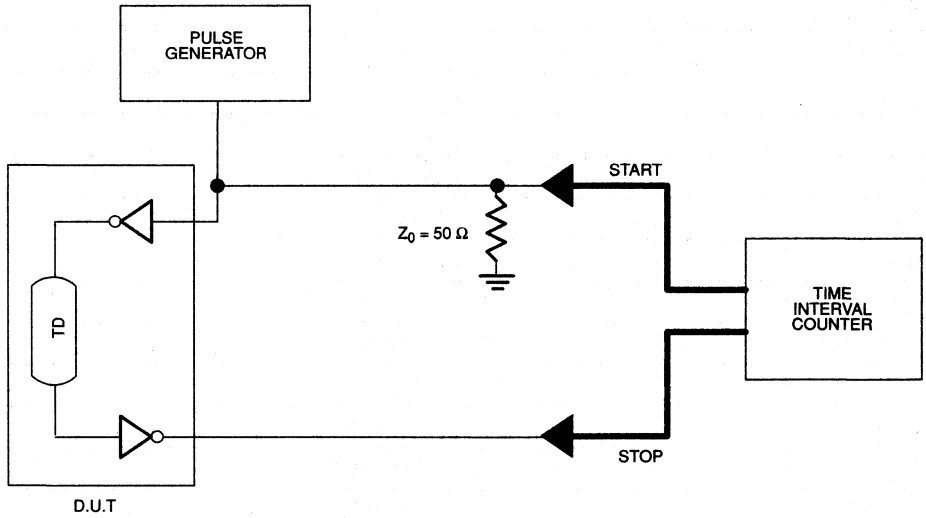
* ±3% tolerance.

** ±5% tolerance.

TIMING DIAGRAM-SILICON DELAY LINE Figure 2



TEST CIRCUIT Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C;V_{CC}= 5.0V ± 5%)

PARAMETER	SYMBOL	TEST COND.	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC}+0.5		
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	0.0V ≤ VI ≤ V_{CC}	-1.0		1.0	µA	
Active Current	I_{CC}	V_{CC}= Max Period= Min.		40	70	mA	2
High Level Output Current	I_{OH}	V_{CC}= Min. V_{OH}= 4.0V			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC}=Min V_{OL}=0.5V	12.0			mA	

AC ELECTRICAL CHARACTERISTICS

(T_A= 25°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}	100% of t_{PLH}			ns	
Input to Output Delay (leading edge)	t_{PLH}		Table 1		ns	3,4,5,6
Input to Output Delay (trailing edge)	t_{PHL}		Table 1		ns	3,4,5,6
Power-up Time	t_{PU}			100	ms	
	Period	3(t_{WI})			ns	7

CAPACITANCE

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. V_{CC}= 5V @ 25°C. Delays accurate on both rising and falling edges within ±2 ns for -10 to -65, ±3% for -70 to -100 and ±5% for -150 and longer delays.
4. See "Test Conditions" section.
5. The combination of temperature variations from 25°C to 0°C or 25°C to 70°C and voltage variations from 5.0V to 4.75V or 5.0V to 5.25V may produce an additional delay shift of ±1.5 ns or ±3%, whichever is greater.
6. All output delays tend to vary unidirectionally over temperature or voltage ranges (i.e., if OUT 1 slows down, all other outputs also slow down).
7. Period specifications may be exceeded; however, accuracy will be application-sensitive (decoupling, layout, etc.).

TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of the corresponding output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of the corresponding output pulse.

TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1013. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between each input and corresponding output. Each output is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50 ohms Max.
Rise and Fall Time:	3.0 ns Max.
Pulse Width:	500 ns
Period:	1 µs

OUTPUT:

Each output is loaded with the equivalent of one 74F04 input gate. Delay is measured at the 1.5V level on the rising and falling edge.

NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

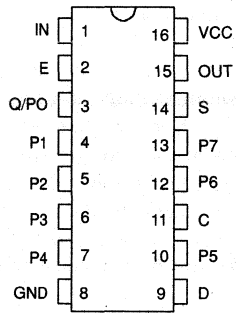
DALLAS SEMICONDUCTOR

DS1020
Programmable 8-Bit Silicon Delay Line

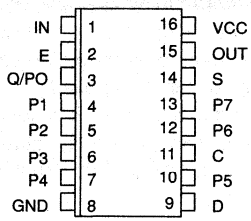
FEATURES

- All-silicon time delay
- Models with 0.15 ns, 0.25 ns, 0.5 ns, 1 ns, and 2 ns steps
- Programmable using 3-wire serial port or 8-bit parallel port
- Leading and trailing edge accuracy
- Standard 16-pin DIP or 16-pin SOIC
- Economical
- Auto-insertable, low profile
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable

PIN ASSIGNMENT



DS1020 16-PIN DIP
(300 MIL)
See Mech. Drawing
Pg. 480



DS1020S 16-PIN SOIC
(300 MIL)
See Mech. Drawing
Pg. 484

PIN DESCRIPTION

IN	–	Delay Input
P0-P7	–	Parallel Program Pins
GND	–	Ground
OUT	–	Delay Output
VCC	–	+5 Volts
S	–	Mode Select
E	–	Enable
C	–	Serial Port Clock
Q	–	Serial Data Output
D	–	Serial Data Input

DESCRIPTION

The DS1020 Programmable 8-Bit Silicon Delay Line consists of an 8-bit, user-programmable CMOS silicon integrated circuit. Delay values, programmed using either the 3-wire serial port or the 8-bit parallel port, can be varied over 256 equal steps. The fastest model (-015) offers a maximum delay of 48.25 ns with an incremental delay of 0.15 ns, while the slowest model (-200) has a maximum delay of 520 ns with an incremental delay of 2 ns. All models have an inherent (step zero) delay of 10 ns. After the user-determined delay, the input logic state is reproduced at the output without inversion. The DS1020 is TTL- and CMOS-compatible, capable of driving 10 74LS-type loads, and features both rising and falling edge accuracy.

The all-CMOS DS1020 integrated circuit has been designed as a reliable, economic alternative to hybrid programmable delay lines. It is offered in a standard 16-pin auto-insertable DIP and a space-saving surface mount 16-pin SOIC.

PARALLEL MODE (S = 1)

In the PARALLEL programming mode, the output of the DS1020 will reproduce the logic state of the input after a delay determined by the state of the eight program input pins P0 - P7. The parallel inputs can be programmed using DC levels or computer-generated data. For infrequent modification of the delay value, jumpers may be used to connect the input pins to V_{CC} and ground. For applications requiring frequent timing adjustment, DIP switches should be used. The enable pin (E) must be at a logic 1 in hardwired implementations.

Maximum flexibility is obtained when the eight parallel programming bits are set using computer-generated data. When the data setup (t_{DSE}) and data hold (t_{DHE}) requirements are observed, the enable pin can be used to latch data supplied on an 8-bit bus. Enable must be held at a logic 1 if it is not used to latch the data. After each change in delay value, a settling time (t_{EDV} or t_{PDV}) is required before input logic levels are accurately delayed.

Since the DS1020 is a CMOS design, unused input pins (D and C) must be connected to well-defined logic levels; they must not be allowed to float.

SERIAL MODE (S = 0)

In the SERIAL programming mode, the output of the DS1020 will reproduce the logic state of the input after a delay time determined by an 8-bit value clocked into serial port D. While observing data setup (t_{DSC}) and data hold (t_{DHC}) requirements, timing data is loaded in MSB-to-LSB order by the rising edge of the serial clock (C). The enable pin (E) must be at a logic 1 to load or read the internal 8-bit input register, during which time the delay is determined by the last value activated. Data transfer ends and the new delay value is activated when enable (E) returns to a logic 0. After each change, a settling time (t_{EDV}) is required before the delay is accurate.

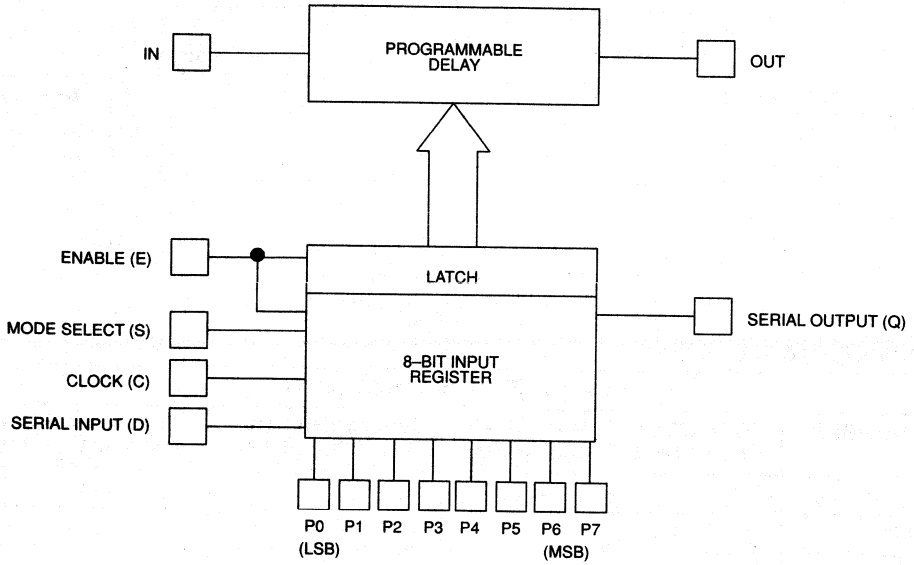
As timing values are shifted into the serial data input (D), the previous contents of the 8-bit input register are shifted out of the serial output pin (Q) in MSB-to-LSB order. By connecting the serial output of one DS1020 to the serial input of a second DS1020, multiple devices can be daisy-chained (cascaded) for programming purposes (Figure 3). The total number of serial bits must be eight times the number of units daisy-chained and each group of 8 bits must be sent in MSB-to-LSB order.

Applications can read the setting of the DS1020 delay line by connecting the serial output pin (Q) to the serial input (D) through a resistor with a value of 1K to 10K ohms (Figure 2). Since the read process is destructive, the resistor restores the value read and provides isolation when writing to the device. The resistor must connect the serial output (Q) of the last device to the serial input (D) of the first device of a daisy-chain (Figure 3). For serial readout with automatic restoration through a resistor, the device used to write serial data must go to a high impedance state.

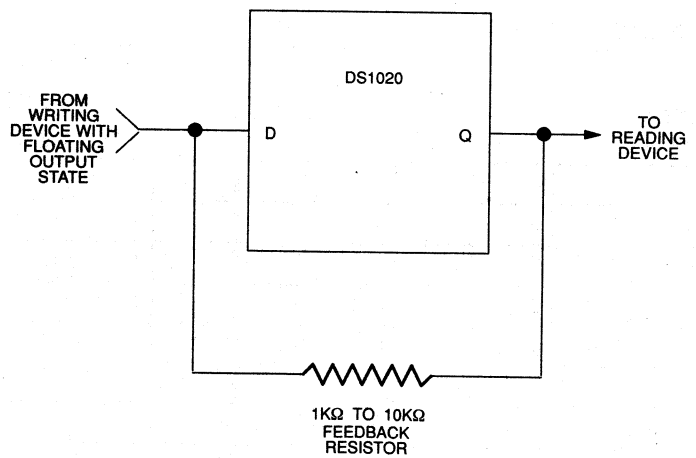
To initiate a serial read, enable (E) is taken to a logic 1 while serial clock (C) is at a logic 0. After a waiting time (t_{EQV}), bit 7 (MSB) appears on the serial output (Q). On the first rising (0 --> 1) transition of the serial clock (C), bit 7 (MSB) is rewritten and bit 6 appears on the output after a time t_{CQV}. To restore the input register to its original state, this clocking process must be repeated 8 times. In the case of a daisy-chain, the process must be repeated 8 times per package. If the value read is restored before enable (E) is returned to logic 0, no settling time (t_{EDV}) is required and the programmed delay remains unchanged.

Since the DS1020 is a CMOS design, unused input pins (P1 - P7) must be connected to well-defined logic levels; they must not be allowed to float. Serial output Q/P0 should be allowed to float if unused.

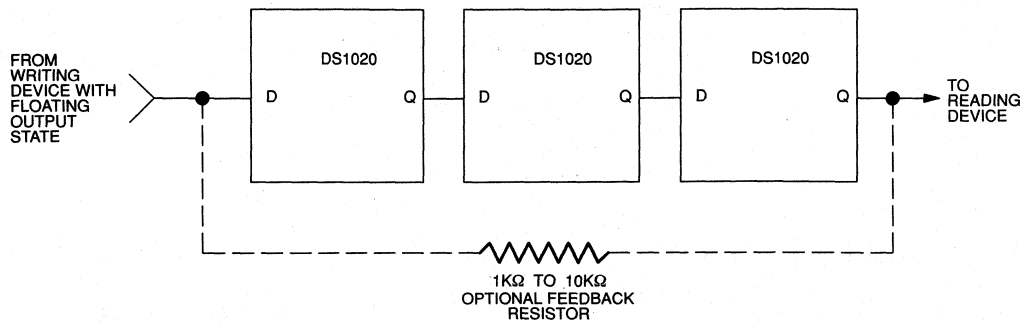
FUNCTION BLOCK DIAGRAM Figure 1



SERIAL READOUT Figure 2



CASCADING MULTIPLE DEVICES (DAISY CHAIN) Figure 3



PART NUMBER TABLE Table 1

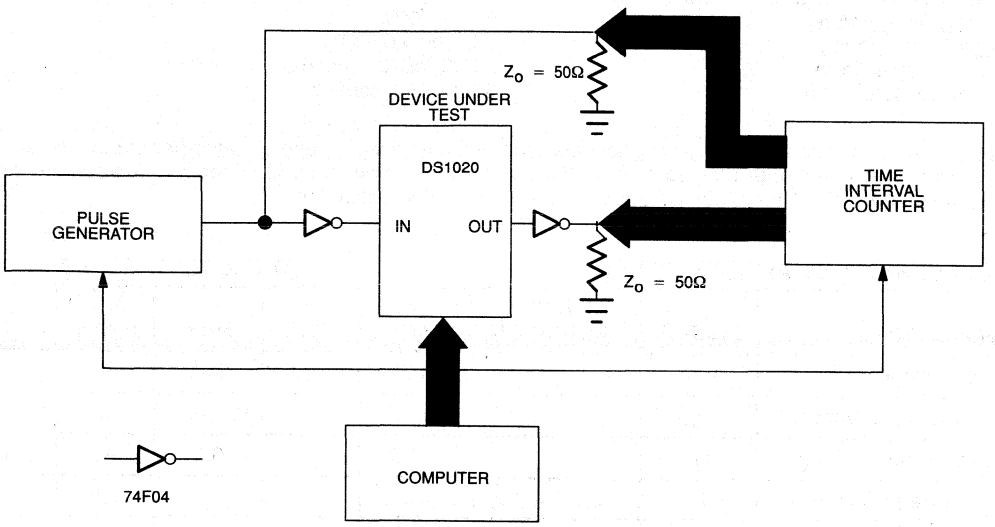
DELAYS AND TOLERANCES (IN ns)				
PART NUMBER	**STEP ZERO DELAY TIME**	**MAX DELAY TIME (NOM)**	**DELAY CHANGE PER STEP (NOM)**	**MAX DEVIATION FROM PROGRAMMED DELAY**
DS1020–015	10 ± 2	48.25	0.15	±4
DS1020-025	10 ± 2	73.75	0.25	±6
DS1020-050	10 ± 2	137.5	0.5	±8
DS1020-100	10 ± 2	265	1	±20
DS1020-200	10 ± 3	520	2	±40

DELAY VS. PROGRAMMED VALUE Table 2

	STEP ZERO								**MAX DELAY**	**PARALLEL PORT**	**SERIAL PORT**
BINARY PROGRAMMED VALUE	0	0	0	0	0	0	1	1	1	P7	MSB
	0	0	0	0	0	0	1	1	1	P6	
	0	0	0	0	0	0	1	1	1	P5	
	0	0	0	0	0	0	1	1	1	P4	
	0	0	0	0	0	0	1	1	1	P3	
	0	0	0	0	1	1	1	1	1	P2	
	0	0	1	1	0	0	0	1	1	P1	
PART NUMBER	0	1	0	1	0	1	1	0	1	P0	LSB
DS1020–015	10.00	10.15	10.30	10.45	10.60	10.75	47.95	48.10	48.25		
DS1020-025	10.00	10.25	10.50	10.75	11.00	11.25	73.25	73.50	73.75		
DS1020-050	10.0	10.5	11.0	11.5	12.0	12.5	136.5	137.0	137.5		
DS1020-100	10	11	12	13	14	15	263	264	265		
DS1020-200	10	12	14	16	18	20	516	518	520		

All delays in nanoseconds, referenced to input pin.

DALLAS SEMICONDUCTOR TEST CIRCUIT Figure 4



TEST SETUP DESCRIPTION

Figure 4 illustrates the hardware configuration used for measuring the timing parameters of the DS1020. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected to the output. The DS1020 serial and parallel ports are controlled by interfaces to a central computer. All measurements are fully automated with each instrument controlled by the computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50 ohms max.
Rise and Fall Time:	3.0 ns max. (measured between 0.6V and 2.4V)
Pulse Width:	500 ns (DS1020–015)
	500 ns (DS1020–025)
	2 µs (DS1020–050)
	4 µs (DS1020–100)
	4 µs (DS1020–200)
Period:	1 µs (DS1020–015)
	1 µs (DS1020–025)
	4 µs (DS1020–050)
	8 µs (DS1020–100)
	8 µs (DS1020–200)

NOTE: Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

OUTPUT:

Output is loaded with a 74F04. Delay is measured between the 1.5V level of the rising edge of the input signal and the 1.5V level of the corresponding edge of the output.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC}+0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0 \le V_I \le V_{CC}$	-1.0		1.0	µA	
Active Current	I_{CC}	V_{CC} = MAX; PERIOD = 1 µs			30.0	mA	3
High Level Output Current	I_{OH}	V_{CC} = MIN V_{OH} = 2.7V			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC} = MIN. V_{OL} = 0.5V	8			mA	5

AC ELECTRICAL CHARACATERISTICS

(0°C to 70°C; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	f_C			10	MHz	
Enable Width	t_{EW}	50			ns	
Clock Width	t_{CW}	50			ns	
Data Setup to Clock	t_{DSC}	30			ns	
Data Hold from Clock	t_{DHC}	10			ns	
Data Setup to Enable	t_{DSE}	30			ns	
Data Hold from Enable	t_{DHE}	20			ns	
Enable to Serial Output Valid	t_{EQV}			50	ns	
Enable to Serial Output High Z	t_{EQZ}	0		50	ns	
Clock to Serial Output Valid	t_{CQV}			50	ns	
Clock to Serial Output Invalid	t_{CQX}	10			ns	
Enable Setup to Clock	t_{ES}	50			ns	
Enable Hold from Clock	t_{EH}	50			ns	

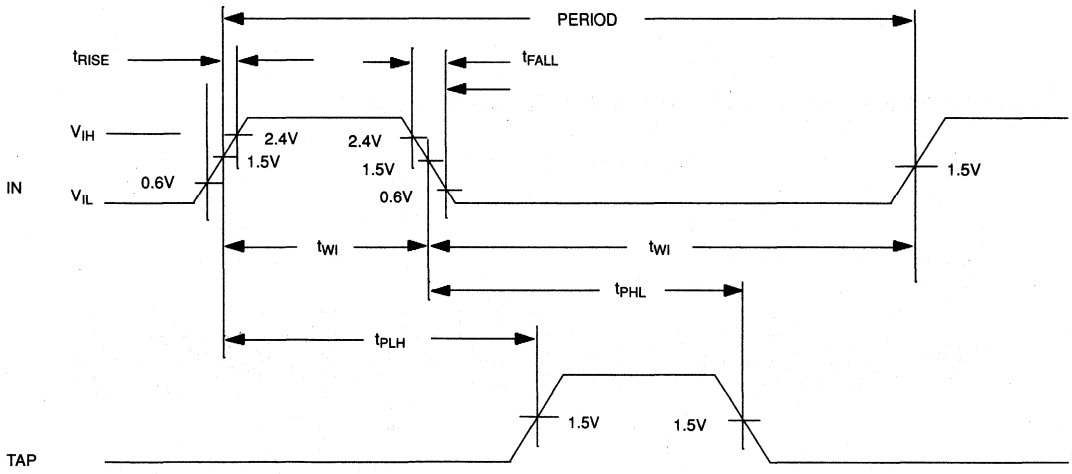
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Parallel Input Valid to Delay Valid	t_{PDV}			50	µs	
Parallel Input Change to Delay Invalid	t_{PDX}	0			ns	
Enable to Delay Valid	t_{EDV}			50	µs	
Enable to Delay Invalid	t_{EDX}	0			ns	
V_{CC} Valid to Device Functional	t_{PU}			100	ms	
Input Pulse Width	t_{WI}	100% of Output Delay			ns	
Input to Output Delay	t_{PLH}, t_{PHL}		Table 2		ns	2
Input Period	Period	$3(t_{WI})$			ns	4

CAPACITANCE

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	

TIMING DIAGRAM: SILICON DELAY LINE Figure 5



TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

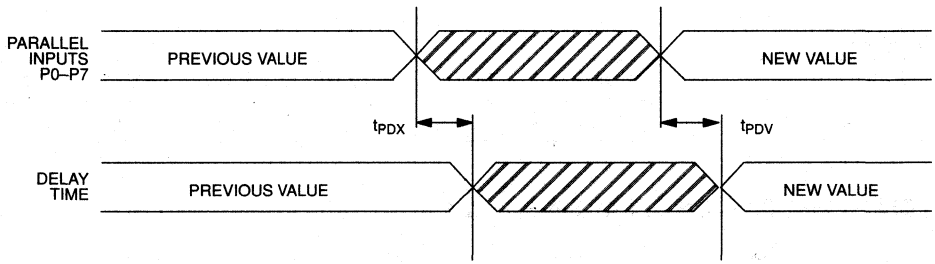
t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

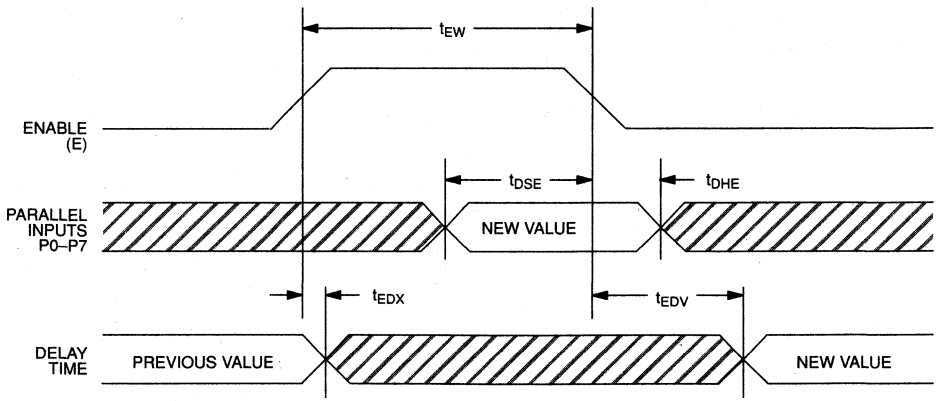
t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of the output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of the output pulse.

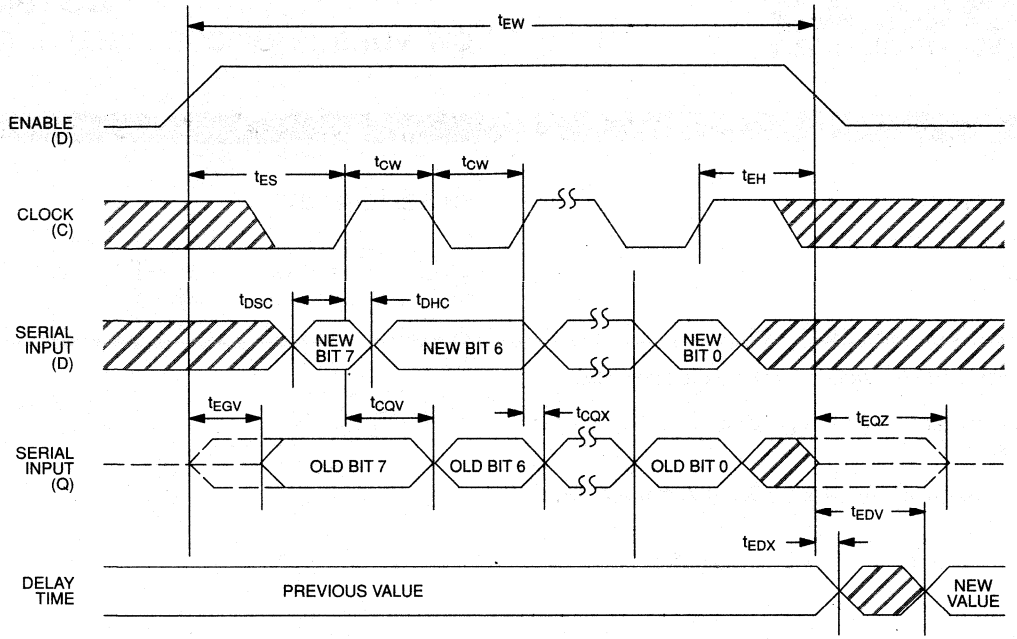
TIMING DIAGRAM: NON-LATCHED PARALLEL MODE (S = 1, E = 1) Figure 6



TIMING DIAGRAM: LATCHED PARALLEL MODE (S=1) Figure 7



TIMING DIAGRAM: SERIAL MODE (S = 0) Figure 8



NOTES:

1. All voltages are referenced to ground.
2. @V_{CC} = 5V and 25°C. Delay accurate on both rising and falling edges within tolerances given in Table 1.
3. Measured with output open.
4. Period specifications may be exceeded; however, accuracy will be application-sensitive (decoupling, layout, etc.).
5. The "Q" output will only source 4 mA. This pin is only intended to drive other DS1020s.

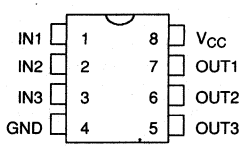
DALLAS SEMICONDUCTOR

DS1033
3–in–1 Low Voltage Silicon Delay Line

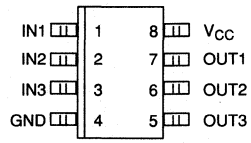
FEATURES

- All–silicon timing circuit
- Three independent buffered delays
- Initial delay tolerance ±1.5 ns
- Stable and precise over temperature and voltage
- Leading and trailing edge precision preserves the input symmetry
- Standard 8–pin DIP, 8–pin SOIC (150 mil) and 20–pin TSSOP
- Vapor phasing, IR and wave solderable
- Available in Tape and Reel

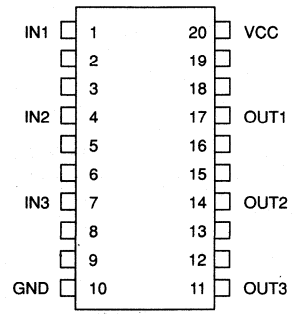
PIN ASSIGNMENT



DS1033M 8–PIN DIP
See Mech. Drawing
Pg. 480



DS1033Z 8–PIN SOIC (150 MIL)
See Mech. Drawing
Pg. 483



DS1033E 20–PIN TSSOP
(CONTACT FACTORY FOR AVAILABILITY)
See Mech. Drawing
Pg. 485

PIN DESCRIPTION

IN1–IN3	–	Input Signals
OUT1–OUT3	–	Output Signals
NC	–	No Connection
V_{CC}	–	Supply Voltage
GND	–	Ground

DESCRIPTION

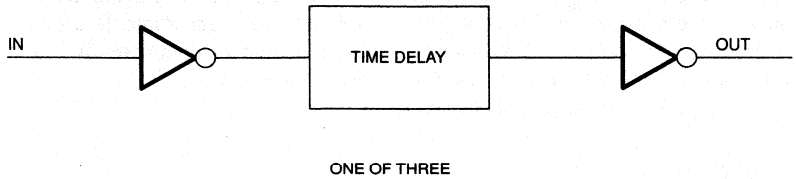
The DS1033 series is a low–power +3.3 Volt version of the DS1035. It is characterized for operation over the range of 2.7V to 3.6V.

The DS1033 series of delay lines have three independent logic buffered delays in a single package. It is available in a standard 8–pin DIP, 150 Mil 8–pin Mini–SOIC and 20–pin TSSOP.

The device features precise leading and trailing edge accuracies. It has the inherent reliability of an all–silicon delay line solution. The DS1033's nominal tolerance is ±1.5 ns and an additional tolerance over temperature and voltage of ±1.0 ns for the faster delays. Detailed specifications are shown in Table 1.

Standard delay values are indicated in Table 1. Customers may contact Dallas Semiconductor at 214–450–5348 for further information.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PLH}, t_{PHL}) Table 1

PART NUMBER	DELAY PER OUTPUT (ns) (note 1)	INITIAL TOLERANCE (note 1)	TOLERANCE OVER TEMPERATURE AND VOLTAGE (note 2)	
			V_{CC}=3.3V ± 0.3V	V_{CC}=2.7V
DS1033–08	8/8/8	±1.5 ns	±1.0 ns	±1.5 ns
DS1033–10	10/10/10	±1.5 ns	±1.0 ns	±1.5 ns
DS1033–12	12/12/12	±1.5 ns	±1.0 ns	±1.5 ns
DS1033–15	15/15/15	±1.5 ns	±1.5 ns	±2.0 ns
DS1033–20	20/20/20	±1.5 ns	±1.5 ns	±2.5 ns
DS1033–25	25/25/25	±2.0 ns	±2.0 ns	±3.5 ns
DS1033–30	30/30/30	±2.0 ns	±2.0 ns	±5.0 ns

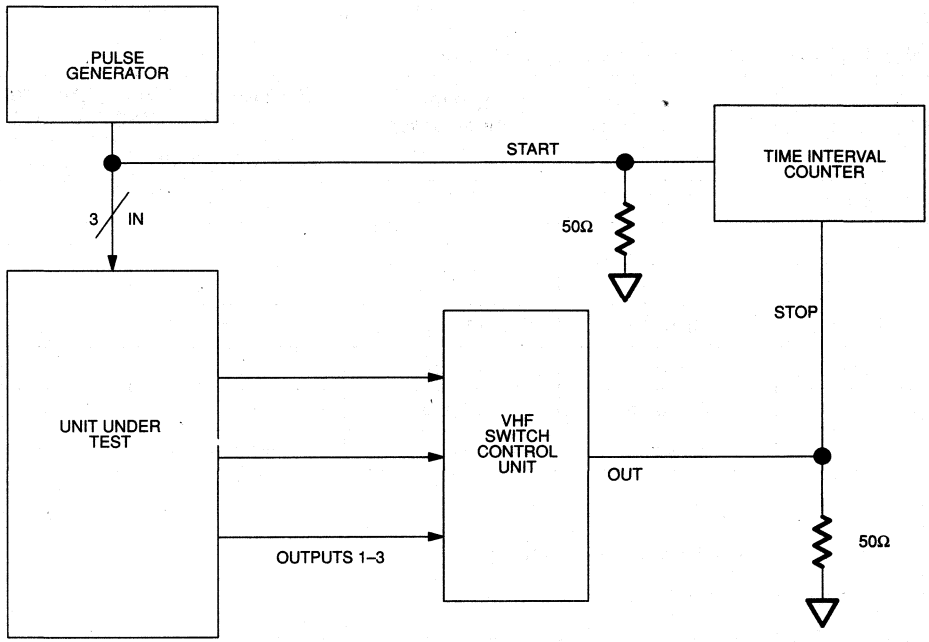
NOTES:

1. Nominal conditions are +25°C and V_{CC}=+3.3 volts.
2. Temperature range of 0°C to 70°C.
3. Delay accuracy is for both leading and trailing edges.

TEST SETUP DESCRIPTION

Figure 2 illustrates the hardware configuration used for measuring the timing parameters of the DS1033. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected to the output. The DS1033 output taps are selected and connected to the interval counter by a VHF switch control unit. All measurements are fully automated with each instrument controlled by the computer over an IEEE 488 bus.

DS1033 TEST CIRCUIT Figure 2



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–1.0V to +6.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(T_A=0°C to 70°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		2.7	3.3	3.6	V
Active Current	I_{CC}	V_{CC}=3.6V Period=1µs			25	mA
High Level Input Voltage	V_{IH}		2.0		V_{CC}+0.5	V
Low Level Input Voltage	V_{IL}		–0.5		0.8	V
Input Leakage	I_L	$0V \le V_I \le V_{CC}$	–1.0		1.0	µA
High Level Output Current	I_{OH}	V_{CC}=2.7V V_{OH}=2V			–1.0	mA
Low Level Output Current	I_{OL}	V_{CC}=2.7V V_{OL}=0.4V	8			mA

AC ELECTRICAL CHARACTERISTICS

(T_A=+25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Period	t_{PERIOD}	2 (t_{WI})			ns	2
Input Pulse Width	t_{WI}	100% of Tap Delay			ns	2
Input–to–Tap Output Delay	t_{PLH}, t_{PHL}		Table 1		ns	
Output Rise or Fall Time	t_{OR}, t_{OF}		2.0 3.0	2.5 3.5	ns ns	3 4
Power–up Time	t_{PU}			100	ms	

CAPACITANCE

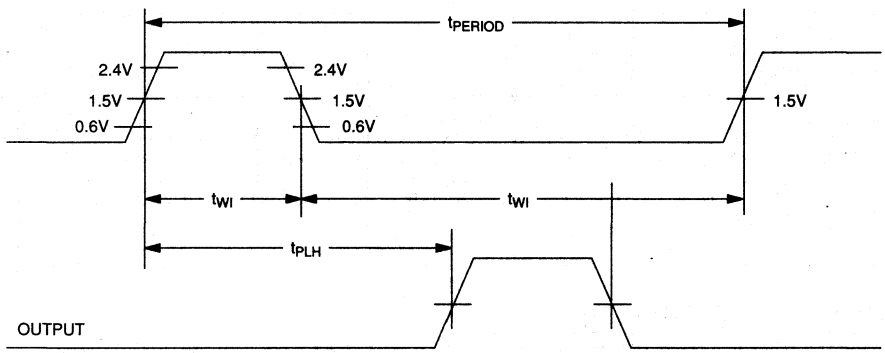
(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	

TEST CONDITIONS

Ambient Temperature: 25°C ± 3°C
Supply Voltage (V_{CC}): 3.3V ± 0.1V
Input Pulse:
High: 3.0V ± 0.1V
Low: 0.0V ± 0.1V
Source Impedance: 50Ω Max.
Rise and Fall Time: 3.0 ns Max. – Measured between 0.6V and 2.4V.
Pulse Width: 500 ns
Pulse Period: 1 µs
Output Load Capacitance: 15 pF
Output: Each output is loaded with the equivalent of one 74F04 input gate.
Data is measured at the 1.5V level on the rising and falling edges.
Note: The above conditions are for test only and do not restrict the devices under other data sheet conditions.

TIMING DIAGRAM: DS1033 INPUT TO OUTPUTS



NOTES:

1. All voltages are referenced to ground.
2. Pulse width and duty cycle specifications may be exceeded, however, accuracy will be application sensitive with respect to de–coupling, layout, etc.
3. V_{CC}=3.3V ± 10%
4. V_{CC}=2.7V

TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5 volt point on the leading edge and the 1.5 volt point on the trailing edge or the 1.5 volt point on the trailing edge and the 1.5 volt point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge on the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5 volt point on the leading edge of the input pulse and the 1.5 volt point on the leading edge of the output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5 volt point on the falling edge of the input pulse and the 1.5 volt point on the falling edge of the output pulse.

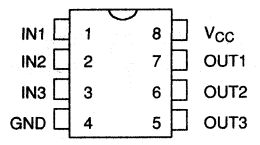
DALLAS SEMICONDUCTOR

DS1035
3–in–1 High–Speed Silicon Delay Line

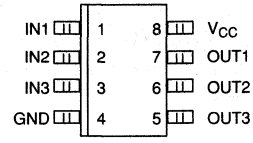
FEATURES

- All–silicon timing circuit
- Three independent buffered delays
- Initial delay tolerance ±1.5 ns
- Stable and precise over temperature and voltage
- Leading and trailing edge precision preserves the input symmetry
- Standard 8–pin DIP, 8–pin SOIC (150 mil) and 20–pin TSSOP
- Vapor phasing, IR and wave solderable
- Available in Tape and Reel

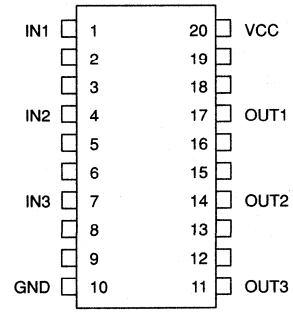
PIN ASSIGNMENT



DS1035M 8–PIN DIP
See Mech. Drawing
Pg. 480



DS1035Z 8–PIN SOIC (150 MIL)
See Mech. Drawing
Pg. 483



DS1035E 20–PIN TSSOP
(CONTACT FACTORY FOR AVAILABILITY)
See Mech. Drawing
Pg. 485

PIN DESCRIPTION

IN1–IN3	–	Input Signals
OUT1–OUT3	–	Output Signals
NC	–	No Connection
V_{CC}	–	+5 Volt Supply
GND	–	Ground

DESCRIPTION

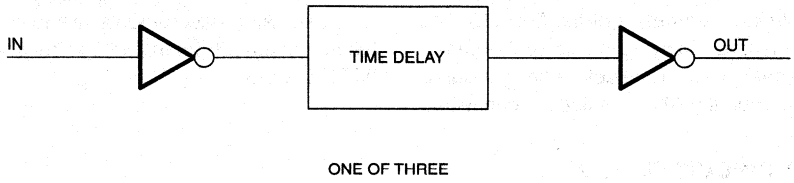
The DS1035 series is a low–power +5 Volt high speed version of the popular DS1013 and compliments the DS1033 +3.3 Volt version.

The DS1035 series of delay lines have three independent logic buffered delays in a single package. The device is Dallas Semiconductor's fastest 3–in–1 delay line. It is available in a standard 8–pin DIP, 150 Mil 8–pin Mini–SOIC and 20–pin TSSOP.

The device features precise leading and trailing edge accuracies. It has the inherent reliability of an all–silicon delay line solution. The DS1035's nominal tolerance is ±1.5 ns and an additional tolerance over temperature and voltage of ±1.0 ns for the faster delays. Each output is capable of driving up to 10 LS loads.

Standard delay values are indicated in Table 1. Customers may contact Dallas Semiconductor at 214–450–5348 for further information.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PLH}, t_{PHL}) Table 1

PART NUMBER	DELAY PER OUTPUT (ns)	INITIAL TOLERANCE	TOLERANCE OVER (temp and voltage)
DS1035–06	6/6/6	±1.5 ns	±1.0 ns
DS1035–08	8/8/8	±1.5 ns	±1.0 ns
DS1035–10	10/10/10	±1.5 ns	±1.0 ns
DS1035–12	12/12/12	±1.5 ns	±1.0 ns
DS1035–15	15/15/15	±1.5 ns	±1.5 ns
DS1035–20	20/20/20	±1.5 ns	±1.5 ns
DS1035–25	25/25/25	±2.0 ns	±1.5 ns
DS1035–30	30/30/30	±2.0 ns	±1.5 ns

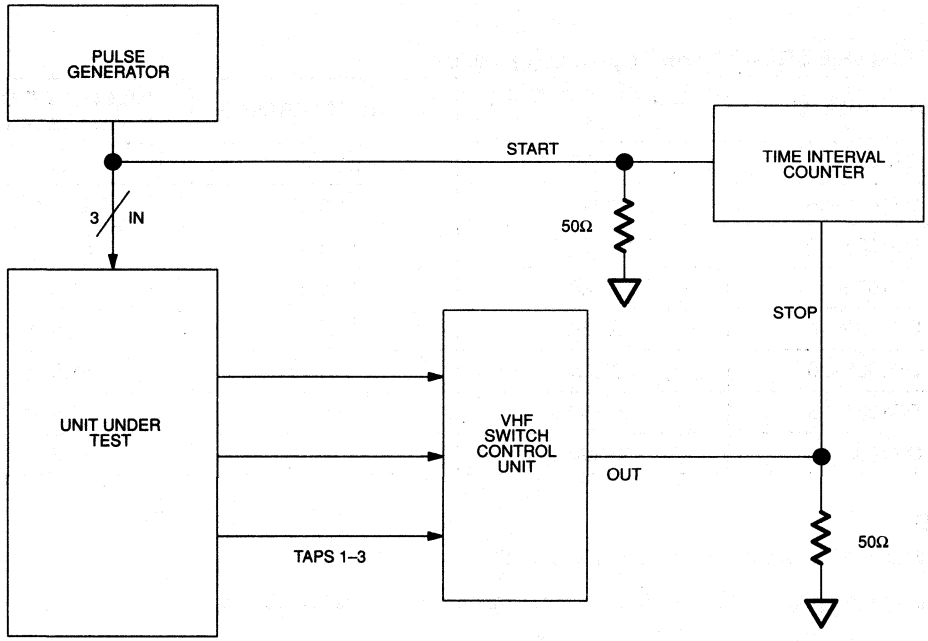
NOTES:

1. Nominal conditions are +25°C and V_{CC}=+5.0 volts.
2. Temperature range of 0°C to 70°C and voltage range of 4.75 volts to 5.25 volts.
3. Delay accuracy are for both leading and trailing edges.

TEST SETUP DESCRIPTION

Figure 2 illustrates the hardware configuration used for measuring the timing parameters of the DS1035. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected to the output. The DS1035 output taps are selected and connected to the interval counter by a VHF switch control unit. All measurements are fully automated with each instrument controlled by the computer over an IEEE 488 bus.

DS1035 TEST CIRCUIT Figure 2



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=+5V ± 5%)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75	5.00	5.25	V
Active Current	I_{CC}	V_{CC}=5.25V Period=1µs			35	mA
High Level Input Voltage	V_{IH}		2.2		V_{CC}+0.5	V
Low Level Input Voltage	V_{IL}		–0.5		0.8	V
Input Leakage	I_L	$0V \le V_I \le V_{CC}$	–1.0		1.0	µA
High Level Output Current	I_{OH}	V_{CC}=4.75V V_{OH}=4V			–1.0	mA
Low Level Output Current	I_{OL}	V_{CC}=4.75V V_{OL}=0.5V	12			mA

AC ELECTRICAL CHARACTERISTICS

(+25°C; V_{CC}=5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Period	t_{PERIOD}	2 (t_{WI})			ns	3
Input Pulse Width	t_{WI}	100% of Tap Delay			ns	3
Input–to–Tap Output Delay	t_{PLH}, t_{PHL}		Table 1		ns	
Output Rise or Fall Time	t_{OR}, t_{OF}		2.0	2.5	ns	
Power–up Time	t_{PU}			100	ms	

CAPACITANCE

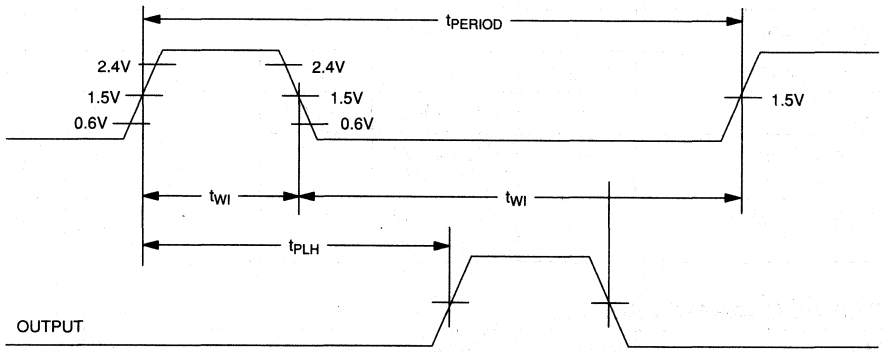
(T_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	

TEST CONDITIONS

Ambient Temperature: 25°C ± 3°C
Supply Voltage (V_{CC}): 5.0V ± 0.1V
Input Pulse:
High: 3.0V ± 0.1V
Low: 0.0V ± 0.1V
Source Impedance: 50Ω Max.
Rise and Fall Time: 3.0 ns Max. – Measured between 0.6V and 2.4V.
Pulse Width: 500 ns
Pulse Period: 1 µs
Output Load Capacitance: 15 pF
Output: Each output is loaded with the equivalent of one 74F04 input gate.
Data is measured at the 1.5V level on the rising and falling edges.
Note: The above conditions are for test only and do not restrict the devices under other data sheet conditions.

TIMING DIAGRAM: DS1035 INPUT TO OUTPUTS



NOTES:

1. All voltages are referenced to ground.
2. @ V_{CC}=5 volts and 25°C, delay accuracy on both the rising and falling edges within tolerances given in Table 1.
3. Pulse width and duty cycle specifications may be exceeded, however, accuracy will be application sensitive with respect to de–coupling, layout, etc.

TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5 volt point on the leading edge and the 1.5 volt point on the trailing edge or the 1.5 volt point on the trailing edge and the 1.5 volt point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge on the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5 volt point on the leading edge of the input pulse and the 1.5 volt point on the leading edge of the output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5 volt point on the falling edge of the input pulse and the 1.5 volt point on the falling edge of the output pulse.

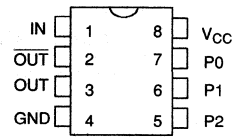
DALLAS SEMICONDUCTOR

DS1040
Programmable One-Shot Pulse Generator

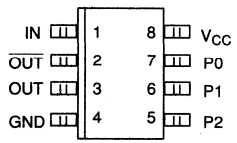
FEATURES

- All-silicon pulse width generator
- Five programmable widths
- Equal and unequal increments available
- Maximum pulse widths from 50 ns to 500 ns
- Widths are stable and precise
- Rising edge-triggered
- Inverted and non-inverted outputs
- Width tolerance ±5% or ±2 ns, whichever is greater
- Economical
- Auto-insertable, low profile
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom widths available
- Fast turn prototypes
- Extended temperature range available

PIN ASSIGNMENT



DS1040M 8-PIN DIP (300 MIL)
DS1040H 8-PIN GULLWING (300 MIL)
See Mech. Drawings – Pgs. 480 & 491



DS1040Z 8-PIN SOIC (150 MIL)
See Mech. Drawing – Pg. 483

Also Available In Die Form

PIN DESCRIPTION

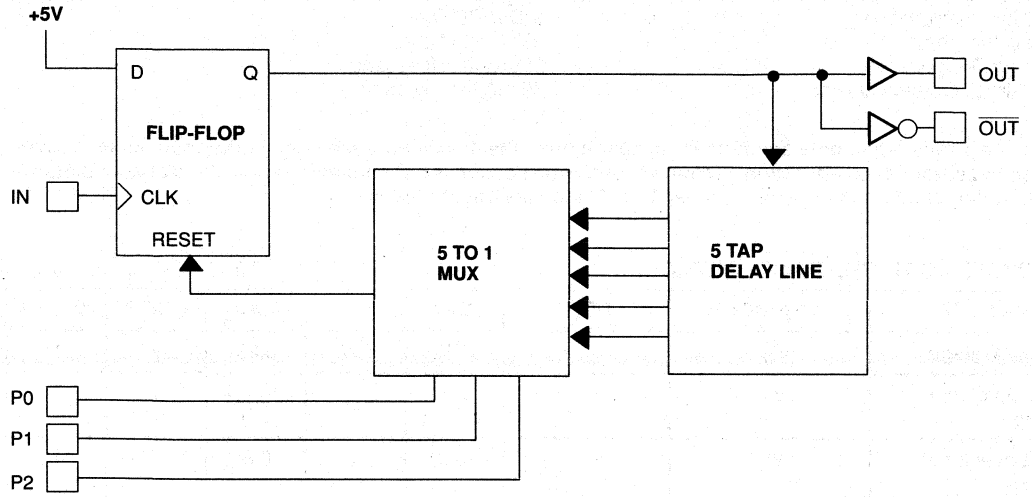
IN	–	Trigger Input
P0-P2	–	Programming Pins
GND	–	Ground
OUT	–	Pulse Output
$\overline{OUT}$	–	Inverted Pulse Output
V_{CC}	–	+5V

DESCRIPTION

The DS1040 Pulse Generator is a user-programmable one-shot with a choice of five precise pulse widths. Maximum widths range from 50 ns to 500 ns; increments range from 2.5 ns to 100 ns. For maximum flexibility in applications such as magneto-optical read/write disk laser power control, varieties are offered with equal and unequal increments. The DS1040 is offered in standard 8-pin DIPs and 8-pin mini-SOICs. Low cost and superior reliability over hybrid technology are achieved by the combination of a 100% CMOS silicon design and industry standard packaging. The DS1040 series of pulse generators provide a nominal width accuracy of ±5% or ±2 ns, whichever is greater. In response to the rising edge of the input (trigger) pulse, the DS1040 produces an output pulse with a width determined by the logic states of the three parallel programming pins. For convenience, both inverting and non-inverting outputs are supplied. The intrinsic delay between the trigger pulse and the output pulse is no more than 10 ns. Each output is capable of driving up to five 74LS loads.

Dallas Semiconductor can customize standard products to meet special needs. For special request and rapid delivery, call (214) 450-5348.

LOGIC DIAGRAM Figure 1



PULSE WIDTH VS. PROGRAMMED VALUE Table 1

	PROGRAMMING PINS	MAX WIDTH	MAX WIDTH →				MAX WIDTH	MAX WIDTH	MAX WIDTH
	MSB P2	0	0	0	0	1	1	1	1
	P1	0	0	1	1	0	0	1	1
	LSB P0	0	1	0	1	0	1	0	1
PART NUMBER									
DS1040-75		75	15	30	45	60	75	75	75
DS1040-100		100	20	40	60	80	100	100	100
DS1040-150		150	30	60	90	120	150	150	150
DS1040-200		200	40	80	120	160	200	200	200
DS1040-250		250	50	100	150	200	250	250	250
DS1040-500		500	100	200	300	400	500	500	500
DS1040-B50		50	30	35	40	45	50	50	50
DS1040-D60		60	20	30	40	50	60	60	60
DS1040-A15		15	5	7.5	10	12.5	15	15	15
DS1040-A20		20	10	12.5	15	17.5	20	20	20
DS1040-A32		32.5	22.5	25	27.5	30	32.5	32.5	32.5
DS1040-B40		40	20	25	30	35	40	40	40
DS1040-D70		70	30	40	50	60	70	70	70

All times in nanoseconds.
Custom pulse widths available.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

($0°C$ to $70°C$; $V_{CC} = 5.0V \pm 5\%$)

PARAMETER	SYMBOL	TEST	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC} + 0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0 \le V_I \le V_{CC}$	-1.0		1.0	mA	
Active Current	I_{CC}	V_{CC} = Max; Period = Min		35	75	mA	2,6
High Level Output Current	I_{OH}	V_{CC} = Min V_{OH} = 4			-1	mA	
Low Level Output Current	I_{OL}	V_{CC} = Min V_{OL} = 0.5	8			mA	

AC ELECTRICAL CHARACTERISTICS

($T_A = 25°C$; $V_{CC} = 5.0V \pm 5\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Programming Setup	t_{PS}	5			ns	
Programming Hold	t_{PH}	0			ns	
Input Pulse Width at Logic 1	t_{WIH}	5			ns	
Input Pulse Width at Logic 0	t_{WIL}	5			ns	
Intrinsic Delay	t_D	0	5	10	ns	
Output Pulse Width	t_{WO}		Table 1		ns	3,4,5,7
Power-up Time	t_{PU}			100	ms	
Period	Period	t_{WO} + 50			ns	

CAPACITANCE

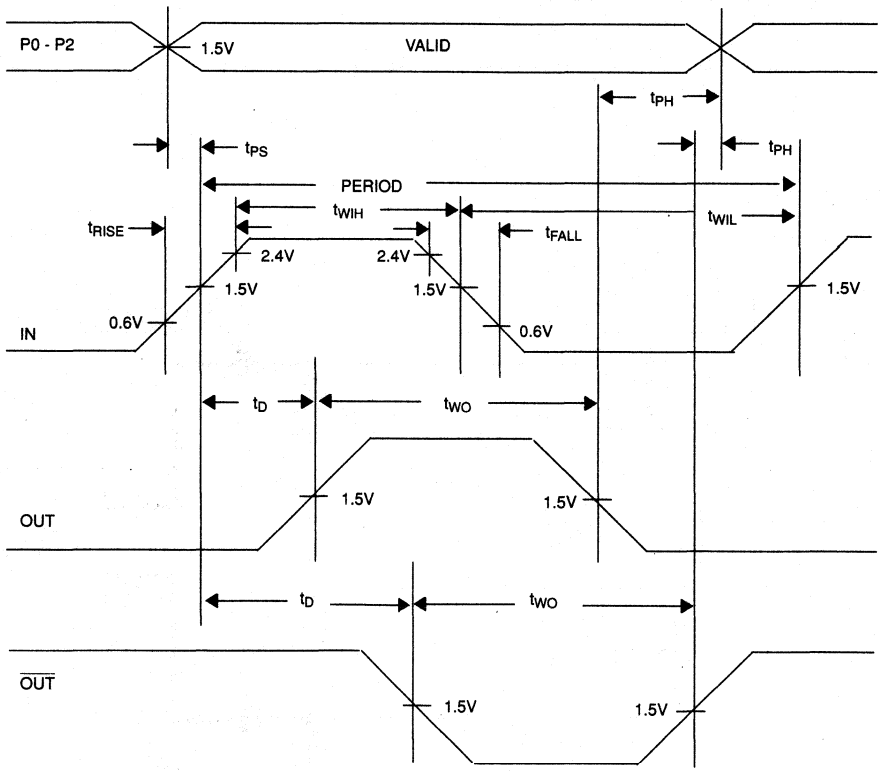
($T_A = 25°C$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

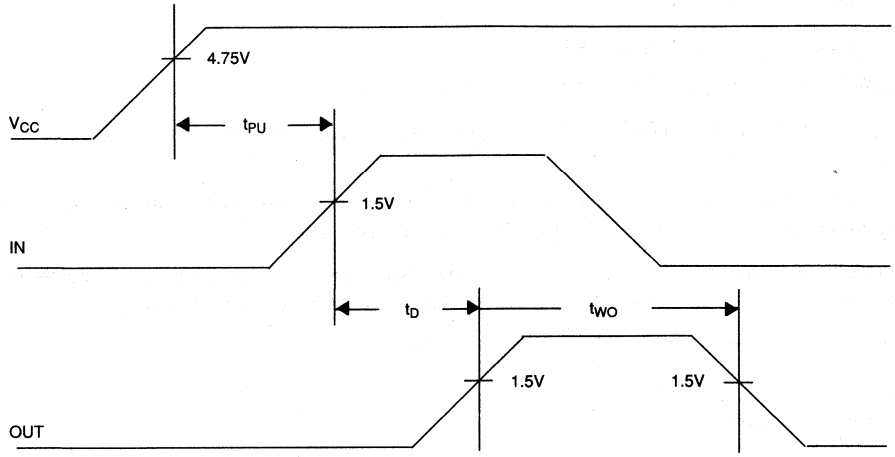
NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open, minimum period.
3. V_{CC} = 5V @ 25°C. Width accurate to within ±2 ns or 5%.
4. Temperature variations between 0°C and 70°C may increase or decrease width by an additional ±1 ns or ±3%, whichever is greater.
5. For DS1040 pulse generators with maximum widths less than 50ns, temperature variations between 0°C and 70°C may increase or decrease width by ±1 ns or ±9%, whichever is greater.
6. I_{CC} is a function of frequency and maximum width. Only a pulse generator operating with 40 ns period and V_{CC}=5.25V will have an I_{CC}=75 mA. For example, a -100 will never exceed 30 mA, etc.
7. See "Test Conditions" sections at the end of this data sheet.

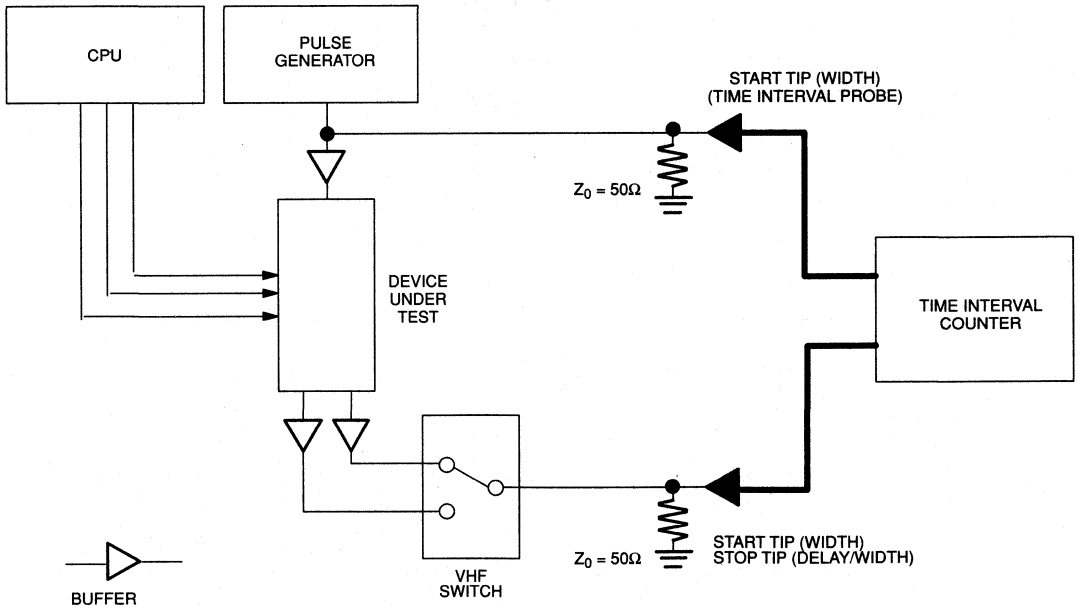
TIMING DIAGRAM Figure 2



POWER -UP TIMING DIAGRAM Figure 3



TEST CIRCUIT Figure 4



TERMINOLOGY

Period: The time elapsed between the leading edge of the first trigger pulse and the leading edge of the following trigger pulse.

$t_{WIH, WIL, WO}$ (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_D (Intrinsic Delay): The elapsed time between the 1.5 point on the leading edge of the input trigger pulse and the 1.5V point on the leading edge of output pulse.

t_{PU} (Power-up Time): After V_{CC} is valid, the time required before timing specifications is within tolerance.

TEST SETUP DESCRIPTION

Figure 4 illustrates the hardware configuration used for measuring the timing parameters on the DS1040. The input waveform is produced by a precision pulse generator under software control. The intrinsic delay is measured by a time interval counter (20 ps resolution) connected between the input and each output. Outputs are selected and connected to the counter by a VHF switch control unit. Width measurements are made by directing both the start and stop functions of the counter to the same output. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

Input:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1
Source Impedance:	50 ohm max.
Rise and Fall Time:	3.0 ns max. (measured between 0.6V and 2.4)
Pulse Width:	500 ns (1 µs for -500)
Period:	1 µs (2 µs for -500)

Output:

The output is loaded with a 74F04. Delay is measured at the 1.5V level on the rising and falling edge.

Note:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

PRELIMINARY

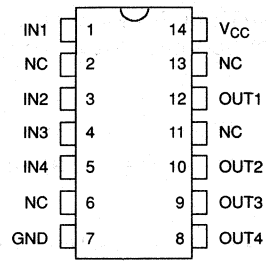
DALLAS SEMICONDUCTOR

DS1044
4–in–1 High–Speed Silicon Delay Line

FEATURES

- All–silicon timing circuit
- Four independent buffered delays
- Initial delay tolerance ±1.5 ns
- Stable and precise over temperature and voltage
- Leading and trailing edge precision preserves the input symmetry
- Standard 14–pin DIP, 14–pin SOIC (150 mil) and 14–pin DIP Gullwing
- Vapor phasing, IR and wave solderable
- Available in Tape and Reel

PIN ASSIGNMENT



DS1044 14–PIN DIP
DS1044G 14–PIN GULLWING
DS1044R 14–PIN SOIC (150 MIL)
See Mech. Drawing
Pgs. 480, 484 & 491

PIN DESCRIPTION

IN1–IN4	–	Input Signals
OUT1–OUT4	–	Output Signals
NC	–	No Connection
V_{CC}	–	+5 Volt Supply
GND	–	Ground

DESCRIPTION

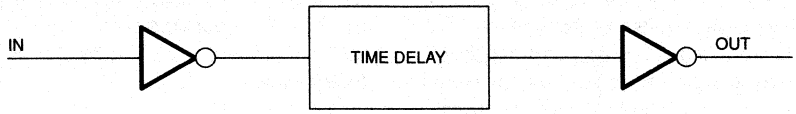
The DS1044 series is a 4–in–1 version of the low–power, +5 Volt, high speed, DS1035.

The DS1044 series of delay lines have four independent logic buffered delays in a single package. The device is Dallas Semiconductor's fastest 4–in–1 delay line. It is available in a standard 14–pin DIP, 14–pin SOIC and 14–pin DIP Gullwing.

The device features precise leading and trailing edge accuracies. It has the inherent reliability of an all–silicon delay line solution. The DS1044's nominal tolerance is ±1.5 ns and an additional tolerance over temperature and voltage of ±1.0 ns for the faster delays. Each output is capable of driving up to 10 LS loads.

Standard delay values are indicated in Table 1. Customers may contact Dallas Semiconductor at 214–450–5348 for further information.

LOGIC DIAGRAM Figure 1



ONE OF FOUR

PART NUMBER DELAY TABLE (t_{PLH}, t_{PHL}) Table 1

PART NUMBER	DELAY PER OUTPUT (ns)	INITIAL TOLERANCE	TOLERANCE OVER (temp and voltage)
DS1044–05	5	±1.5 ns	±1.0 ns
DS1044–06	6	±1.5 ns	±1.0 ns
DS1044–07	7	±1.5 ns	±1.0 ns
DS1044–08	8	±1.5 ns	±1.0 ns
DS1044–10	10	±1.5 ns	±1.0 ns
DS1044–12	12	±1.5 ns	±1.0 ns
DS1044–14	14	±1.5 ns	±1.5 ns
DS1044–18	18	±1.5 ns	±1.5 ns
DS1044–20	20	±1.5 ns	±1.5 ns
DS1044–25	25	±2.0 ns	±1.5 ns

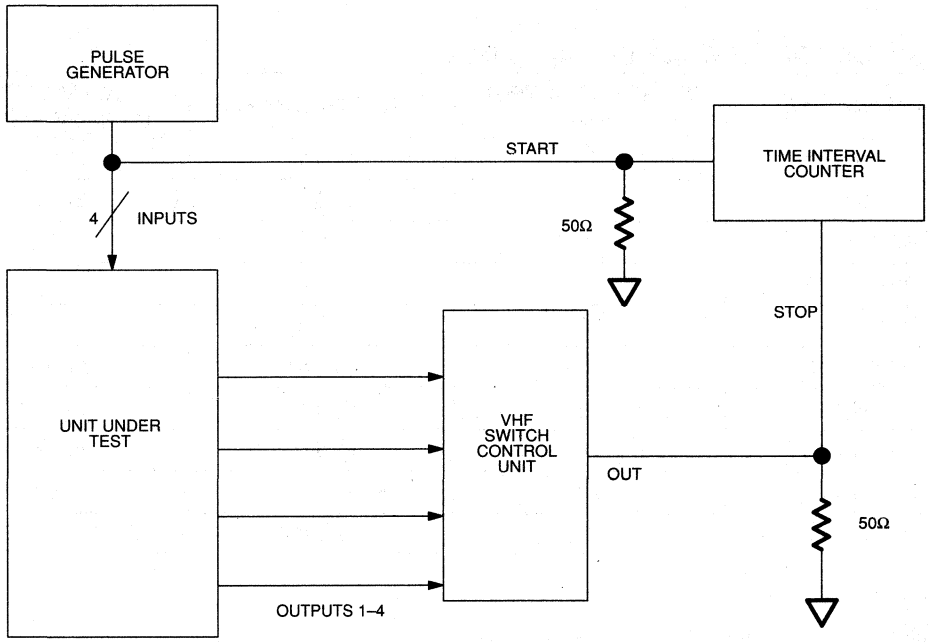
NOTES:

1. Nominal conditions are +25°C and V_{CC}=+5.0 volts.
2. Temperature range of 0°C to 70°C and voltage range of 4.75 volts to 5.25 volts.
3. Delay accuracy are for both leading and trailing edges.

TEST SETUP DESCRIPTION

Figure 2 illustrates the hardware configuration used for measuring the timing parameters of the DS1044. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected to the output. The DS1044 output taps are selected and connected to the interval counter by a VHF switch control unit. All measurements are fully automated with each instrument controlled by the computer over an IEEE 488 bus.

DS1044 TEST CIRCUIT Figure 2



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=+5V ± 5%)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75	5.00	5.25	V
Active Current	I_{CC}	V_{CC}=5.25V Period=1µs			45	mA
High Level Input Voltage	V_{IH}		2.2		V_{CC}+0.5	V
Low Level Input Voltage	V_{IL}		–0.5		0.8	V
Input Leakage	I_L	$0V \le V_I \le V_{CC}$	–1.0		1.0	µA
High Level Output Current	I_{OH}	V_{CC}=4.75V V_{OH}=4V			–1.0	mA
Low Level Output Current	I_{OL}	V_{CC}=4.75V V_{OL}=0.5V	12			mA

AC ELECTRICAL CHARACTERISTICS

(+25°C; V_{CC}=5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Period	t_{PERIOD}	2 (t_{WI})			ns	3
Input Pulse Width	t_{WI}	100% of Tap Delay			ns	3
Input–to–Tap Output Delay	t_{PLH}, t_{PHL}		Table 1		ns	
Output Rise or Fall Time	t_{OR}, t_{OF}		2.0	2.5	ns	
Power–up Time	t_{PU}			100	ms	

CAPACITANCE

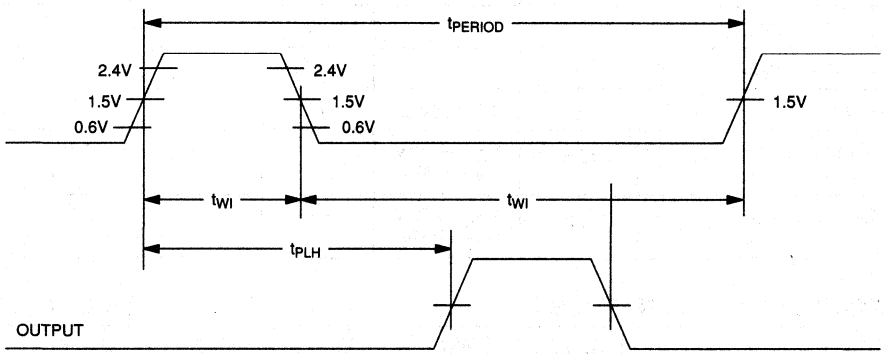
(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	

TEST CONDITIONS

Ambient Temperature: 25°C ± 3°C
Supply Voltage (V_{CC}): 5.0V ± 0.1V
Input Pulse:
High: 3.0V ± 0.1V
Low: 0.0V ± 0.1V
Source Impedance: 50Ω Max.
Rise and Fall Time: 3.0 ns Max. – Measured between 0.6V and 2.4V.
Pulse Width: 500 ns
Pulse Period: 1 µs
Output Load Capacitance: 15 pF
Output: Each output is loaded with the equivalent of one 74F04 input gate.
Data is measured at the 1.5V level on the rising and falling edges.
Note: The above conditions are for test only and do not restrict the devices under other data sheet conditions.

TIMING DIAGRAM: DS1044 INPUT TO OUTPUTS



NOTES:

1. All voltages are referenced to ground.
2. @ V_{CC}=5 volts and 25°C, delay accuracy on both the rising and falling edges within tolerances given in Table 1.
3. Pulse width and duty cycle specifications may be exceeded, however, accuracy will be application sensitive with respect to de–coupling, layout, etc.

TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5 volt point on the leading edge and the 1.5 volt point on the trailing edge or the 1.5 volt point on the trailing edge and the 1.5 volt point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge on the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5 volt point on the leading edge of the input pulse and the 1.5 volt point on the leading edge of the output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5 volt point on the falling edge of the input pulse and the 1.5 volt point on the falling edge of the output pulse.

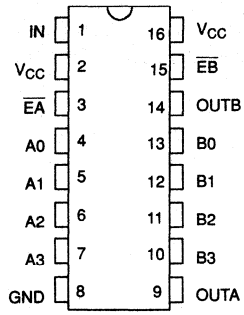
DALLAS SEMICONDUCTOR

DS1045
4-Bit Dual Programmable Delay Line

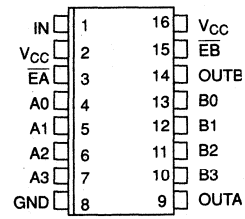
FEATURES

- All–silicon time delay
- Two programmable outputs from a single input produce output–to–output delays between 9 and 84 ns depending on device type
- Programmable via four input pins
- Programmable increments of 3 to 5 ns with a minimum of 9 ns and a maximum of 84 ns
- Output pulse is a reproduction of input pulse after delay with both leading and trailing edge accuracy
- Standard 16–pin DIP or surface mount 16–pin SOIC
- Auto-insertable
- Low–power CMOS design is TTL–compatible

PIN ASSIGNMENT



DS1045 16-PIN DIP (300 MIL)
See Mech. Drawing
Pg. 480



DS1045S 16-PIN SOIC (300 MIL)
See Mech. Drawing
Pg. 484

PIN DESCRIPTION

IN	-	Delay Line Input
OUTA, OUTB	-	Delay Line Outputs
A0-A3	-	Parallel Program Inputs for OUT1
B0-B3	-	Parallel Program Inputs for OUT2
$\overline{EA}$, $\overline{EB}$	-	Enable A and B Inputs
V_{CC}	-	+5 Volt Input
GND	-	Ground

DESCRIPTION

The DS1045 is a programmable silicon delay line having one input and two 4-bit programmable delay outputs. Each 4-bit programmable output offers the user 16 possible delay values to select from, starting with a minimum inherent DS1045 delay of 9 ns and a maximum achievable delay in the standard DS1045 family of 84 ns. The standard DS1045 product line provides the user with three devices having uniform delay increments of 3, 4, and 5 ns depending on the device. Table 2 presents standard device family and delay capability. Additionally, custom delay increments are available for special order through Dallas Semiconductor.

The DS1045 is TTL and CMOS-compatible and capable of driving ten 74LS-type loads. The output produced by the DS1045 is both rising and falling edge precise. The DS1045 programmable silicon delay line has been designed as a reliable, economic alternative to hybrid programmable delay lines. It is offered in a standard 16-pin auto-insertable DIP and a space-saving surface mount 16-pin SOIC package.

PARALLEL PROGRAMMING

Parallel programming of the DS1045 is accomplished via the set of parallel inputs A0–A3 and B0–B3 as shown in Figure 1. Parallel input A0–A3 and B0–B3 accept TTL levels and are used to set the delay values of outputs OUTA and OUTB, respectively. Sixteen possible delay values between the minimum 9 ns delay and the maximum delay of the DS1045-x device version can be selected using the parallel programming inputs A0–A3 or B0–B3 (see Table 2, "Delay vs. Programmed Input"). For example, the DS1045-3 outputs OUTA or OUTB and can be programmed to produce 16 possible delays between the 9 ns (minimum) and the 54 ns (maximum) in 3 ns increment levels.

For applications that do not require frequent reprogramming, the parallel inputs can be set using fixed logic levels, as would be produced by jumpers, DIP switches, or TTL levels as produced by computer systems. Maximum flexibility in parallel programming can be achieved when inputs are set by computer-generated data. By using the enable input pins for each respective programmed output and observing the input setup (t_{DSE}) and hold time (t_{DHE}) requirements, data can be latched on an 8-bit bus. If the enable pins, $\overline{EA}$ and $\overline{EB}$, are not used to latch data, they should be set to a logic level 1. After each change in the programmed delay value, a settling time (t_{EDV}) or (t_{PDV}) is required before the delayed output signal is reliably produced. Since the DS1045 is a CMOS design, undefined input pins should be connected to well defined logic levels and not left floating.

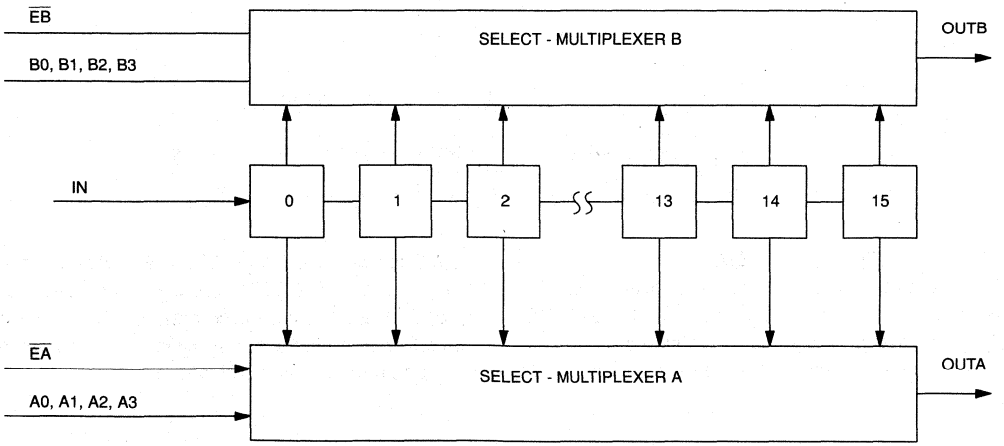
PART NUMBER TABLE Table 1

PART NUMBER	STEP ZERO DELAY	MAX DELAY TIME	MAX DELAY TOLERANCE
DS1045-3	9 ± 1 ns	54 ns	±2.5 ns
DS1045-4	9 ± 1 ns	69 ns	±3.3 ns
DS1045-5	9 ± 1 ns	84 ns	±4.1 ns

NOTE:

Additional delay step times are available from Dallas Semiconductor by special order. Consult factory for availability.

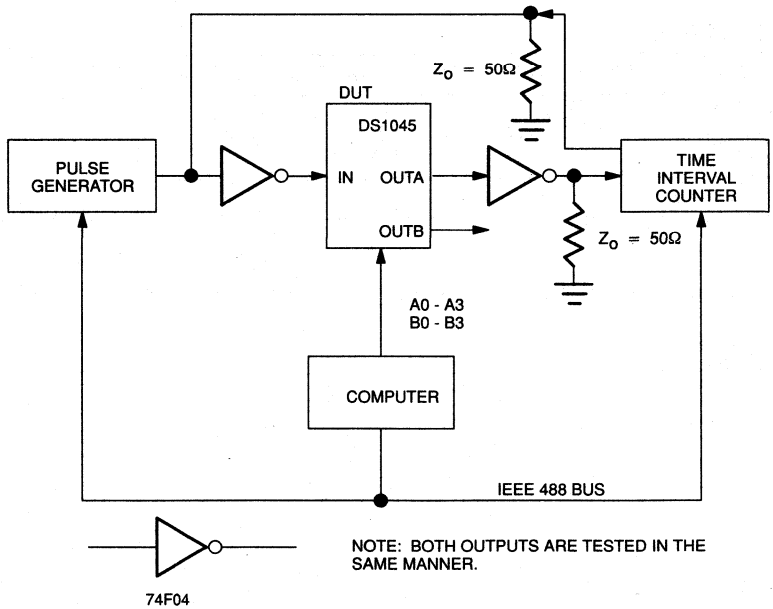
BLOCK DIAGRAM Figure 1



DELAY VS. PROGRAMMED VALUE Table 2

PART NUMBER	OUTPUT DELAY VALUE															
DS1045–3	9	12	15	18	21	24	27	30	33	36	39	42	45	48	51	54
DS1045–4	9	13	17	21	25	29	33	37	41	45	49	53	57	61	65	69
DS1045–5	9	14	19	24	29	34	39	44	49	54	59	64	69	74	79	84
	PROGRAM VALUES FOR EACH DELAY VALUE															
A0 OR B0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
A1 OR B1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
A2 OR B2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
A3 OR B3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

DS1045 TEST CIRCUIT Figure 2



TEST SETUP DESCRIPTION

Figure 2 illustrates the hardware configuration used for measuring the timing parameters of the DS1045. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected to the output. The DS1045 parallel inputs are controlled by an interface to a central computer. All measurements are fully automated with each instrument controlled by the computer over an IEEE 488 bus.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	250°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.0	5.25	V	1
Input Logic 1	V_{IH}		2.2		V_{CC} + 0.5	V	1
Input Logic 0	V_{IL}		-0.5		0.8	µA	1
Input Leakage	I_I	$0 \le V_I \le V_{CC}$	-1.0		1.0	mA	
Active Current	I_{CC}	V_{CC}=5.25V PERIOD=1 µs			35.0	mA	
Logic 1 Output Current	I_{OH}	V_{CC} = 4.75V V_{OH} = 4.0V			-1.0	mA	
Logic 0 Output Current	I_{OL}	V_{CC} = 4.75V V_{OL} = 0.5V	8			mA	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Period	t_{PERIOD}	4 x t_{WI}			ns	
Pulse Width	t_{WI}	100% of output delay size				
Input to Output Delay	t_{PLH}, t_{PHL}	Table 1				2
Parallel Input Change to Delay Invalid	t_{PDX}	0			ns	
Parallel Input Valid to Delay Valid	t_{PDV}		10		ns	
Enable Width	t_{EW}	15			ns	
Data Setup to Enable	t_{DSE}	10			ns	
Data Hold from Enable	t_{DHE}	0			ns	
Enable to Delay Invalid	t_{EDX}		5		ns	
Enable to Delay Valid	t_{EDV}		15		ns	

CAPACITANCE

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	

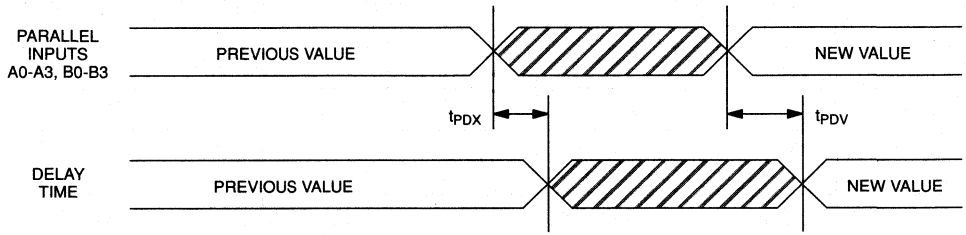
TEST CONDITIONS

T_A = 25°C ± 3°C
V_{CC} = 5.0V ± 0.1V
Input Pulse = 3.0V high to 0.0V low ± 0.1V
Input Source Impedance = 50 ohms maximum
Rise and fall times = 3.0 ns max. between 0.6V and 2.4V
Pulse Width = 250 ns
Period = 500 ns
Output Load = 74F04
Measurement Point = 1.5V on inputs and outputs
Output Load Capacitance = 15 pF

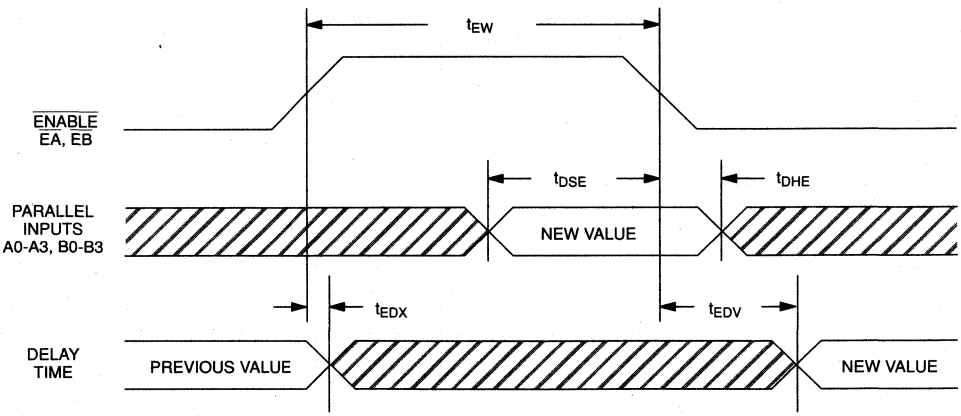
NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

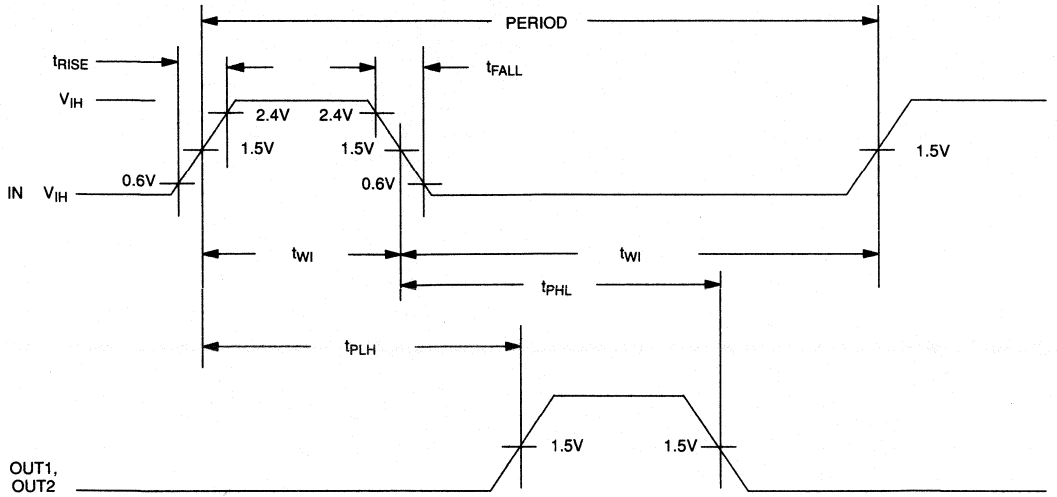
TIMING DIAGRAM: NON-LATCHED PARALLEL MODE, $\overline{EA}$, $\overline{EB}$ = V_{IH}



TIMING DIAGRAM: LATCHED PARALLEL MODE



TIMING DIAGRAM: DS1045 INPUTS TO OUTPUTS



TERMINOLOGY

PERIOD: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of the output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of the output pulse.

NOTES:

1. All voltages are referenced to ground.
2. @ V_{CC} = 5V and 25°C. Delay accurate on both rising and falling edges within tolerances given in Table 1.

SYSTEM EXTENSION

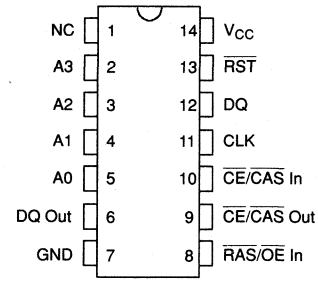
DALLAS SEMICONDUCTOR

DS1206
Phantom Serial Interface Chip

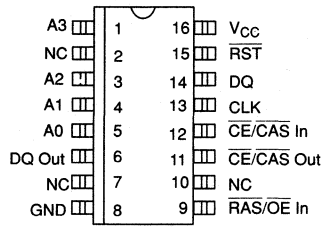
FEATURES

- Minimum expense add-on serial port
- Converts standard bytewide or DRAM memory waveforms into a 3-wire serial port
- Operation is transparent to memory
- Software-generated memory cycles activate serial port and transfer data
- High bandwidth – 1-bit data transfer per two memory cycles
- Intercepts memory signals so that pass-through connections to memory can be maintained
- Controls communications for as many as ten DS1201 Electronic Tags, DS1204U Electronic Keys, DS1207 TimeKeys or DS1290 Eliminators
- Low-power CMOS circuitry
- Optional 16-pin SOIC surface mount package

PIN ASSIGNMENT



14-Pin DIP (300 MIL)
See Mech. Drawing
Pg. 480



16-Pin SOIC (300 MIL)
See Mech. Drawing
Pg. 484

PIN DESCRIPTION

NC	–	No Connection
A0–A3	–	Memory Address Bus
DQ Out	–	Data Out To Memory Bus
GND	–	Ground
$\overline{RAS}/\overline{OE}$ In	–	Output Enable or $\overline{RAS}$ input from memory bus
$\overline{CE}/\overline{CAS}$ In	–	Chip enable or $\overline{CAS}$ from memory bus
$\overline{CE}/\overline{CAS}$ Out	–	Chip enable or $\overline{CAS}$ to memory circuit
CLK	–	Clock for Serial Port
DQ	–	Data I/O for Serial Port
$\overline{RST}$	–	Reset for Serial Port
V_{CC}	–	+5 Volts

DESCRIPTION

The DS1206 Phantom Serial Interface Chip is a CMOS circuit which intercepts the standardized memory bus found in computer systems and adapts the bus to a 3-wire serial port. Multiple memory cycles are used as a basis for generating the appropriate signals to control the serial port. A sequence of software-generated memory cycles encodes commands and transfers data with low pin count. The serial port signaling is derived from the memory address bus lines A0 through A3, the $\overline{CE}/\overline{CAS}$ signal and $\overline{RAS}/\overline{OE}$ signal without affecting

address space, thereby maintaining transparency to the memory bus. Communications are established under software control by an address pattern recognition sequence (serial port protocol) which disables a bytewide or DRAM memory via $\overline{CE}/\overline{CAS}$ output. An additional address sequence is required to generate the 3-wire port signals: $\overline{RESET}$ ($\overline{RST}$), Data (DQ), and Clock (CLK). The add-on serial port provides a minimum cost interface to the DS1201, DS1204U, DS1207, DS1223, and DS1290.

OPERATION

The main parts of the DS1206 are shown in the block diagram of Figure 1. Information presented on address inputs is latched into the DS1206 on the falling edge of a strobe signal derived from the logical combination of $\overline{CE}/\overline{CAS}$ In and $\overline{RAS}/\overline{OE}$ In. When redirecting information from a DRAM memory bus, both $\overline{RAS}$ and $\overline{CAS}$ inputs are required and the column addresses are used for signaling.

For a bytewide memory bus, only a $\overline{CE}$ input is required and the $\overline{RAS}/\overline{OE}$ input can be tied low or connected to the memory $\overline{OE}$ input signal. The rising edge of the strobe will cause the address information to be presented for comparison to the 4-bit serial interface protocol and to logic which will generate signals for the serial port. The serial interface protocol is derived from address inputs A0, A1, and A2.

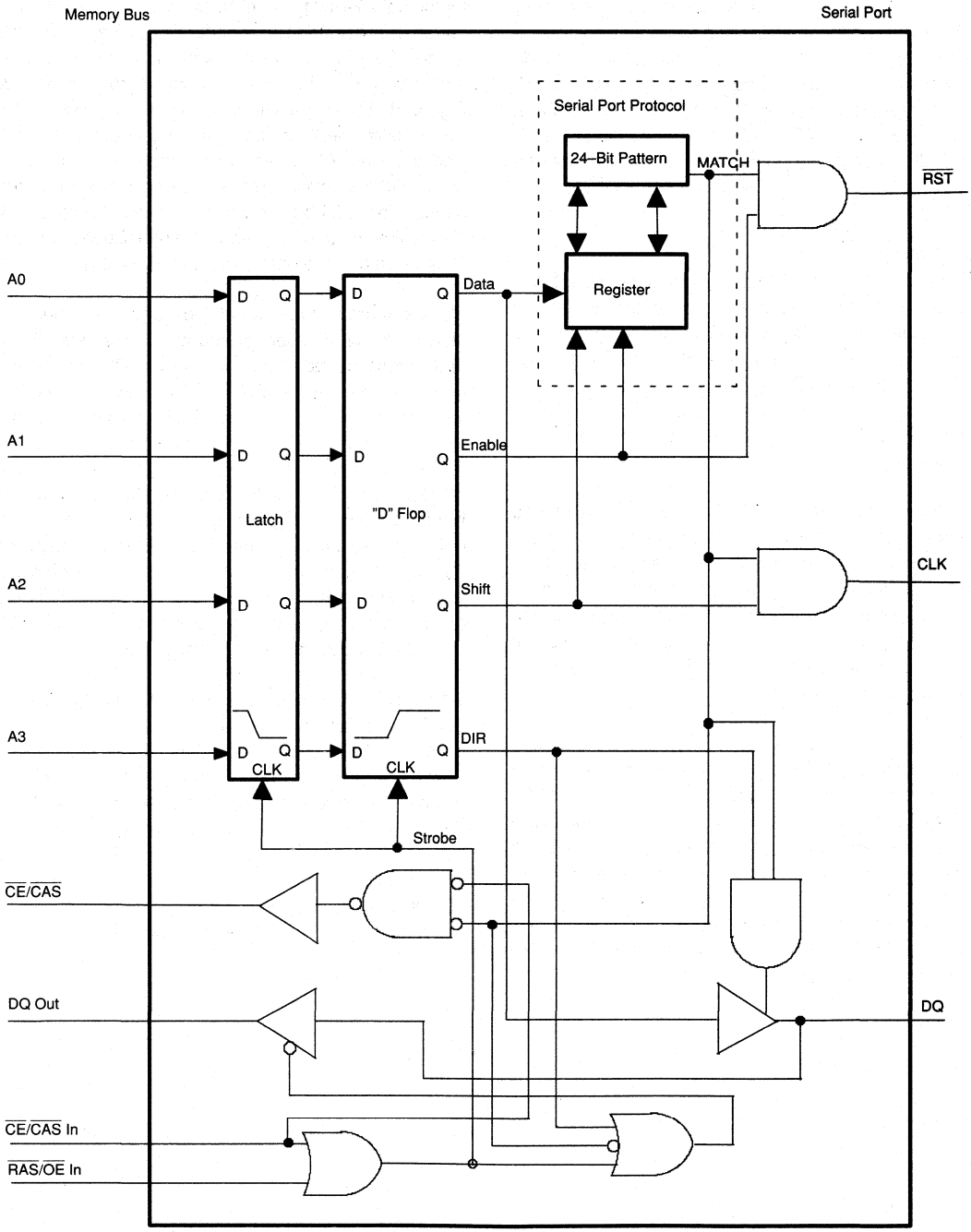
A1 is an enable signal which activates the communications sequence. A0 defines the data which is compared for recognition. A2 is used to clock in information defined by A0. Initially the A1 input must be set high to enable serial interface communications. A1 must remain high during the pattern recognition sequence and subsequent communications with the serial port after the protocol pattern match is established. If the A1 input is set low, all communications are terminated and future access to the serial port is denied.

Data transfer through the serial interface occurs by matching a 24-bit pattern as shown in Figure 2. This pattern is presented to a register on each rising edge of strobe. Data is input for comparison to the serial interface protocol at the end of each memory cycle (see Figure 3). The proper information must be presented on A0 to match the 24-bit pattern while keeping A1 high. Address input A2 is used to generate the shift signal which causes data to enter the 24-bit register for comparison to the 24-bit pattern. Information is loaded one bit at a time on the rising edge of shift. Each shift cycle must be generated from two memory cycles.

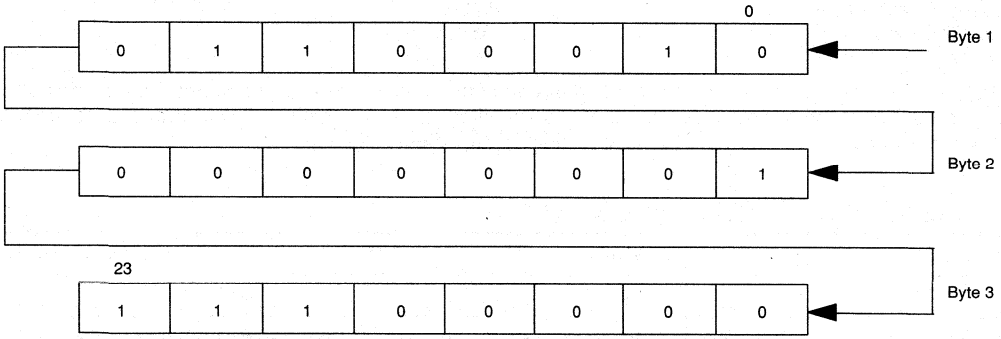
The first memory cycle sets A2 low and establishes the shift clock low. The second memory cycle sets A2 high and causes the transition necessary to shift a bit of data into the 24-bit register. Data on A0 is kept at the correct level for both memory cycles. Address input A3 is used to control the direction of data going to and from the serial port. This input is not used during pattern recognition of the protocol. After the 24-bit pattern has been correctly entered , a match signal is generated. The match signal is logically combined with the enable signal to generate the $\overline{RST}$ signal for the serial port. The match signal is also used to disable Chip Enable to the memory bus and to enable a gate which allows the serial port DQ to drive the DQ out line to the memory bus.

When $\overline{RST}$ is driven high, devices attached to the serial port become active. Subsequent shift signals derived from A2 will now be recognized as the serial port clock. The data signal for the serial bus is derived from A0 conditioned on the level of the direction signal derived from A3. When A3 is set high, data as defined by A0 will be sent out on the serial port DQ. When A3 is set low, devices attached to the serial port can drive the memory bus DQ out line. The data direction bit must be set low when reading data from the serial port DQ.

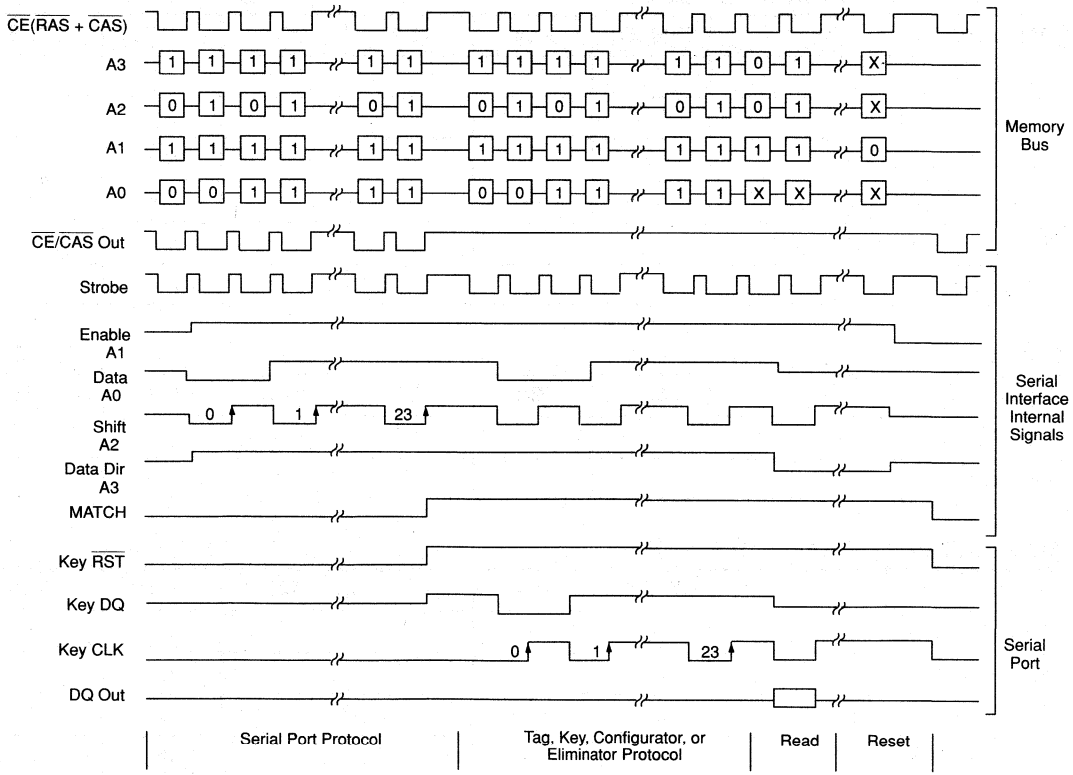
PHANTOM SERIAL INTERFACE BLOCK DIAGRAM Figure 1



SERIAL INTERFACE 24-BIT PROTOCOL Figure 2



PHANTOM SERIAL INTERFACE SIGNALS Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{CC} + 0.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
Supply	V_{CC}	4.5	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1		1	µA	
Output Leakage	I_{LO}			1	µA	
Output Current @ 2.4V	I_{OH}	-1			mA	
Output Current @ .4V	I_{OL}	+4			mA	
$\overline{RST}$ Output Current @ 3.8V	I_{OHR}	16			mA	
Supply Current	I_{CC}			6	mA	2

CAPACITANCE

(t_A=25°C)

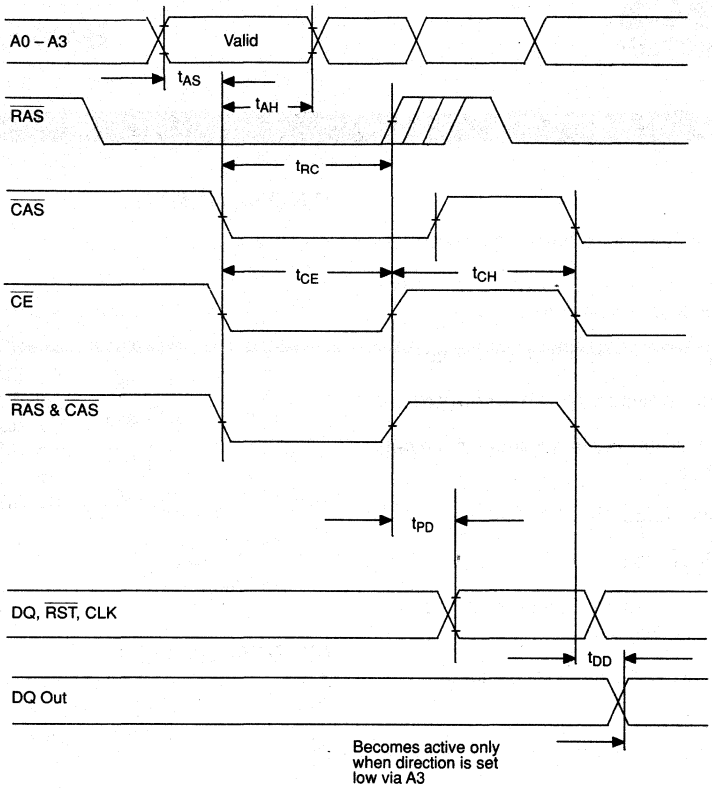
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
$\overline{RAS}$ to $\overline{CAS}$ Overlap	t_{RC}	60			ns	
$\overline{CE}$ Pulse Width	t_{CE}	60			ns	
Key Signals Valid	t_{PD}			60	ns	3
Key Data Out	t_{DD}	10			ns	3
$\overline{CE}$ Inactive	t_{CH}	30			ns	

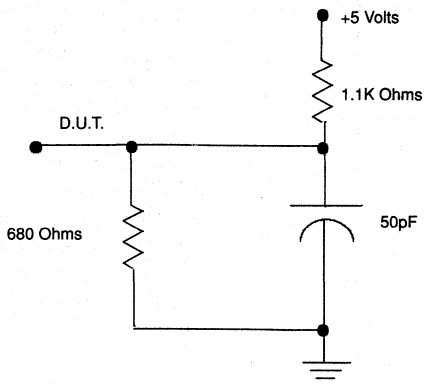
MEMORY BUS INPUTS



NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. Measured with a load as shown in Figure 4.

OUTPUT LOAD Figure 4



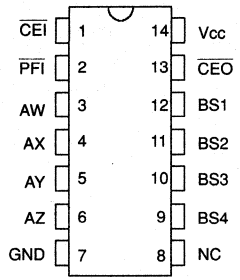
DALLAS SEMICONDUCTOR

DS1222
BankSwitch Chip

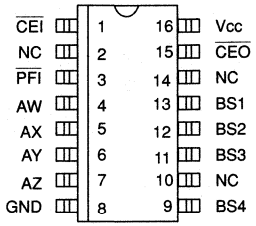
FEATURES

- Provides bank switching for 16 banks of memory
- Bank switching is software-controlled by a pattern recognition sequence on four address inputs
- Automatically sets all 16 banks off on power-up
- Bank switching logic allows only one bank on at a time
- Custom recognition patterns are available to prevent unauthorized access
- Full ±10% operating range
- Low-power CMOS circuitry
- Can be used to expand the address range of microprocessors and decoders
- Optional 16-pin SOIC surface mount package

PIN ASSIGNMENT



DS1222 14-Pin DIP
(300 Mil.)
See Mech. Drawing
Pg. 480



DS1222S16-Pin SOIC
(300 Mil.)
See Mech. Drawing
Pg. 484

PIN DESCRIPTION

A_W-A_Z	–	Address Inputs
$\overline{CEI}$	–	Chip Enable Input
$\overline{CEO}$	–	Chip Enable Output
NC	–	No Connection
BS1,BS2,	–	Bank Select Outputs
BS3,BS4	–	Bank Select Outputs
$\overline{PFI}$	–	Power Fail Input
V_{CC}	–	+5 Volts
GND	–	Ground

DESCRIPTION

The DS1222 BankSwitch Chip is a CMOS circuit designed to select one of sixteen memory banks under software control. Memory bank switching allows for an increase in memory capacity without additional address lines. Continuous blocks of memory are enabled by selecting the proper memory bank through a pattern recognition sequence on four address inputs. Custom patterns available from Dallas Semiconductor can provide security through uniqueness and prevent unauthorized access. By combining the DS1222 with the DS1212 Nonvolatile Controller x16 Chip, up to 16 banks of static RAMs can be selected.

OPERATION – BANK SWITCHING

Initially, on power-up all four bank select outputs are low and the chip enable output ($\overline{CEO}$) is held high. (Note: the power fail input [$\overline{PFI}$] must be low prior to power-up to assure proper initialization.) Bank switching is achieved by matching a predefined pattern stored within the DS1222 with a 16-bit sequence received on four address inputs. Prior to entering the 16-bit pattern, which sets the bank switch, a read cycle of 1111 on address inputs AW through AZ should be executed to guarantee that pattern entry starts with bit 0. Each set of address inputs is clocked into the DS1222 when $\overline{CEI}$ is driven low. All 16 inputs must be consecutive read cycles. The first eleven cycles must match the exact bit pattern as

shown in Table 1. The last five cycles must match the exact bit pattern as shown for addresses AX, AY, and AZ. However, address line AW defines the bank number to be enabled as per Table 2.

Switching to a selected bank of memory occurs on the rising edge of $\overline{CEI}$ when the last set of bits is input and a match has been established. After bank selection $\overline{CEO}$ always follows $\overline{CEI}$ with a maximum propagation delay of 15 ns. The bank selected is determined by the levels set on Bank Select 1 through Bank Select 4 as per Table 2. These levels are held constant for all memory cycles until a new memory bank is selected.

ADDRESS BIT SEQUENCE Table 1

	BIT SEQUENCE															
ADDRESS INPUTS	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
A_W	1	0	1	0	0	0	1	1	0	1	0	x	x	x	x	x
A_X	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1
A_Y	1	0	1	0	0	0	1	1	0	1	0	1	1	1	0	0
A_Z	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1

X See Table 2

BANK SELECT CONTROL Table 2

Bank	**A_W Bit Sequence**					**Outputs**			
Selected	**11**	**12**	**13**	**14**	**15**	**BS1**	**BS2**	**BS3**	**BS4**
*Banks Off	0	X	X	X	X	Low	Low	Low	Low
Bank 0	1	0	0	0	0	Low	Low	Low	Low
Bank 1	1	0	0	0	1	High	Low	Low	Low
Bank 2	1	0	0	1	0	Low	High	Low	Low
Bank 3	1	0	0	1	1	High	High	Low	Low
Bank 4	1	0	1	0	0	Low	Low	High	Low
Bank 5	1	0	1	0	1	High	Low	High	Low
Bank 6	1	0	1	1	0	Low	High	High	Low
Bank 7	1	0	1	1	1	High	High	High	Low
Bank 8	1	1	0	0	0	Low	Low	Low	High
Bank 9	1	1	0	0	1	High	Low	Low	High
Bank 10	1	1	0	1	0	Low	High	Low	High
Bank 11	1	1	0	1	1	High	High	Low	High
Bank 12	1	1	1	0	0	Low	Low	High	High
Bank 13	1	1	1	0	1	High	Low	High	High
Bank 14	1	1	1	1	0	Low	High	High	High
Bank 15	1	1	1	1	1	High	High	High	High

*$\overline{CEO}$ = V_{IH} independent of $\overline{CEI}$

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current	I_{LO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	2
Output Current @ 0.4V	I_{OL}			+4.0	mA	2
Operating Current	I_{CC}			15	mA	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

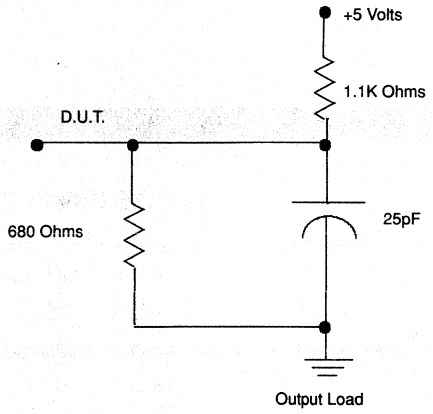
(0°C to 70°C; V_{CC} = 5V± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	5			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	40			ns	
Propagation Delay	t_{PD}			15	ns	2
Power Fail Input to First $\overline{CE}$	t_{PF}	50			ns	
Chip Enable Low	t_{CW}	110			ns	

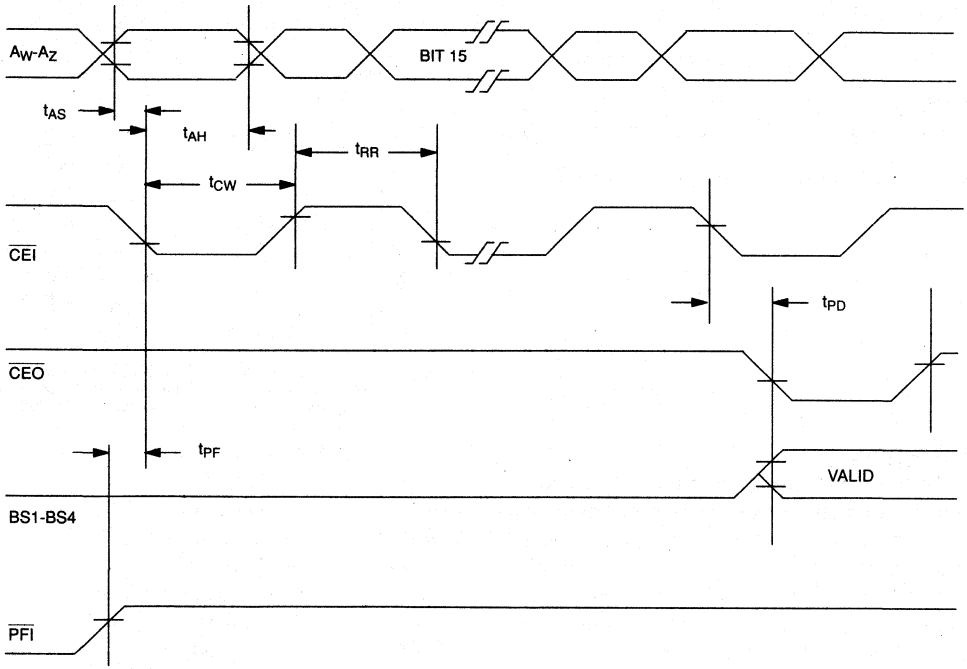
NOTES:

1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 1.

OUTPUT LOAD Figure 1



TIMING DIAGRAM-ACCESS TO BANK SWITCH



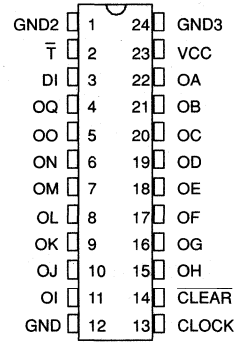
DALLAS SEMICONDUCTOR

DS129x Eliminator

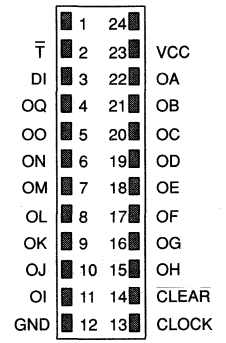
FEATURES

- Replaces 8 or 16 hard-to-get-at manual switches
- Options printed circuit board via software
- Modular expansion by cascading packages
- Set or interrogate with only three signals
- Requires no pull-up resistors
- Links to system bus with the DS1206 Phantom Serial Interface Chip
- Low-power CMOS
- Switch setting changes occur simultaneously
- DS1290 and DS1292 maintain settings in the absence of power; DS1291 and DS1293 are volatile
- Over 10 years of data retention for DS1290 and DS1292

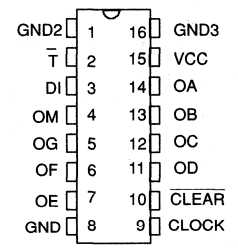
PIN ASSIGNMENT



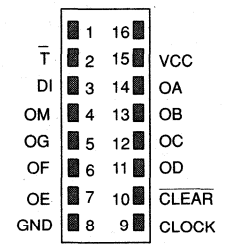
DS1293 24-Pin DIP (300 Mil) See Mech. Drawing Pg. 480



DS1292 24-Pin Encapsulated Package (450 Mil) See Mech. Drawing – Pg. 492



DS1291 16-Pin DIP (300 Mil) See Mech. Drawing Pg. 480



DS1290 16-Pin Encapsulated Package (450 Mil) See Mech. Drawing – Pg. 492

DESCRIPTION

The DS129x Eliminator replaces manual switches used to option printed circuit boards. Up to sixteen output pins can be set to a logic level or interrogated by three signals: clock, data and transfer. The Eliminator can be controlled with software using the DS1206 Phantom Interface to synthesize the clock, data and transfer signals from a system bus. Multiple packages can be strung together for modular expansion. Once programmed, the DS1290 and DS1292 will maintain high or low level outputs, duplicating the effects of a mechanical switch and pull-up resistor. The technical support needed to configure a system is minimized with the Eliminator, Phantom Interface and menu-driven software.

PIN DESCRIPTION

$\overline{T}$	–	Transfer
DI	–	Data Input
O_A–O_Q	–	Switch Outputs
CLOCK	–	Clock Input
$\overline{CLEAR}$	–	All Outputs Set Low
V_{CC}	–	+5 Volts
GND	–	Ground
GND2	–	Missing on DS1292. Must be grounded on DS1293.
GND3	–	Missing on DS1292. Must be grounded on DS1293.

OPERATION

The DS1292/DS1293 Eliminator is a 16-bit shift register that has a clocked serial input, an asynchronous clear, and an output transfer control (see "Block Diagram" in Figure 1). The DS1290/DS1291 Eliminator is an 8-bit shift register that has a clocked serial input, an asynchronous clear, and an output transfer control. Data can be entered into the registers only when the transfer input ($\overline{T}$) is at a high level. While at a high level, the transfer function allows serial entry of data via the data input pin (DI). The outputs 0_Q through 0_B remain in the state that was set prior to $\overline{T}$ being driven to a high level. Output 0_A will change state as new data is entered. This output provides a method of feeding back actual output settings prior to setting the $\overline{T}$ input low (Figure 2). When the $\overline{T}$ input is driven low, new data that has been input into the 16-bit shift register is now locked at outputs 0_Q through 0_A. When the $\overline{T}$ input is low, all clock and data inputs are ignored. Valid data is clocked into the eliminator while $\overline{T}$ is high on the low-to-high transition of the CLOCK input. Data can be changed while the CLOCK input is high or low, but only data meeting the setup requirements will enter the shift register. The $\overline{CLEAR}$ input will always set all outputs to low level regardless of the level of the CLOCK or $\overline{T}$ input.

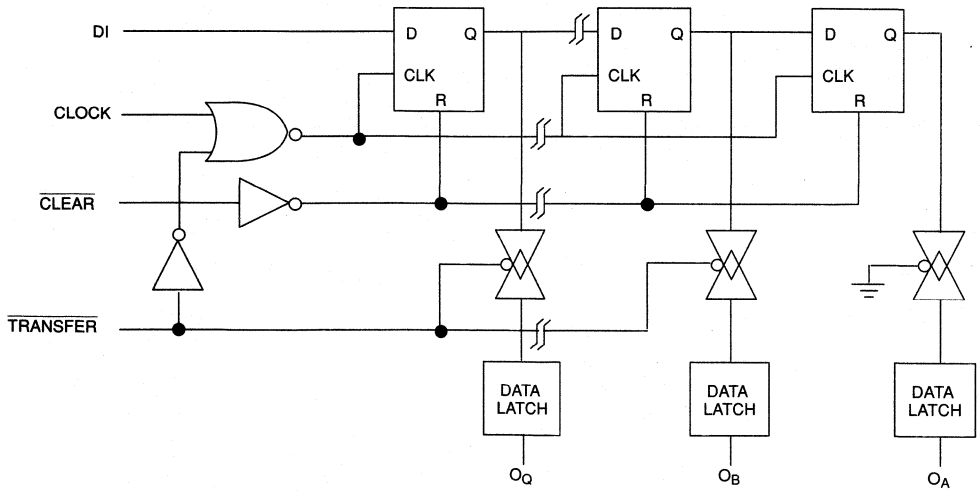
DATA RETENTION MODE

The DS129x Eliminator provides full functional capability when V_{CC} is greater than 4.5 volts and will ignore all inputs when V_{CC} reaches 4.25 volts typical. In this manner, the settings of each register remain intact during power transients. As V_{CC} falls below approximately 3 volts, an internal power switching circuit connects a lithium energy source to the shift register to maintain data. During power-up when V_{CC} rises above approximately 3 volts, the power switching circuit connects external V_{CC} to the shift register and disconnects the lithium energy source. Normal operation can resume after V_{CC} exceeds 4.5 volts for 10 ms minimum. During power transients the 16 outputs will track the level of V_{CC} if set to logic 1 and will remain at ground level if set to Logic 0.

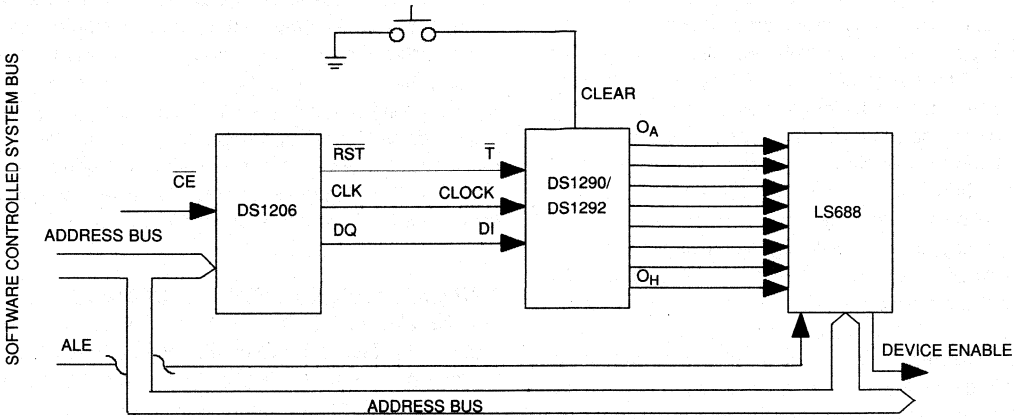
TYPICAL APPLICATION – ELIMINATOR

The DS129x and DS1206 combine to make a programmable nonvolatile DIP switch that can be transparently set in systems without disturbing other operations. Because the switches are nonvolatile, they need only be set once; they will remain in the programmed state indefinitely. The block diagram of Figure 2 shows the Eliminator implemented with the DS1206 Phantom Serial Interface Chip. The DS1206 samples four address lines and the chip enable signal looking for a special pattern for 24 consecutive cycles (see the DS1206 data sheet). When a proper match is found, the address lines and one data line become control and data signals that are used to program and verify the settings of the DS129x. All of the signaling sent to the DS1206 and subsequently to the DS1292 is generated by software-controlled read cycles that have no effect on the rest of system operation. The clear signal can be used to restore a system back to an unconfigured state.

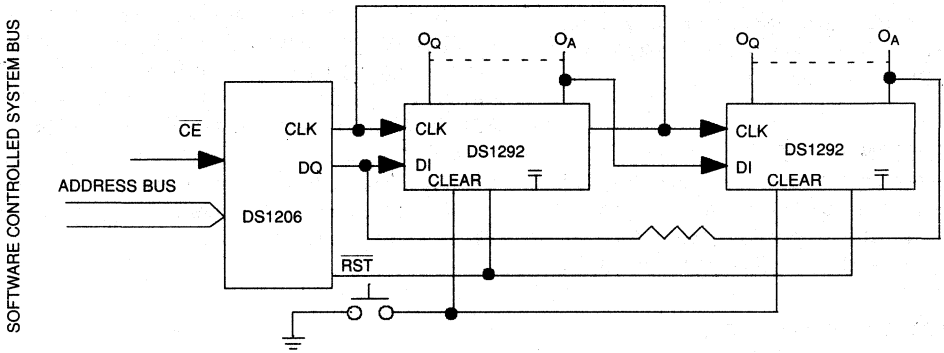
BLOCK DIAGRAM - DS129x Figure 1



PHANTOM INTERFACE AND ELIMINATOR TYPICAL APPLICATION Figure 2



MODULAR EXPANSION OF THE ELIMINATOR Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}		3	5	mA	
Input Leakage	I_{IL}	-1.0		+1.0	µA	4
Output Leakage	I_{LO}	-1.0		+1.0	µA	
Logic 1 Output @ 2.4V	I_{OH}	-1.0			mA	2
Logic 0 Output @ 0.4V	I_{OL}			4.0	mA	2

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

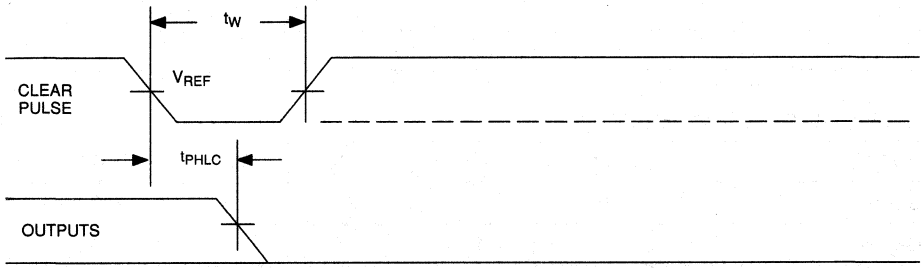
(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	f_{CLOCK}			10	MHz	
Width of Clock Pulse	tw_{CLOCK}	50			ns	3
Width of Clear Pulse	tw_{CLEAR}	50			ns	3
Data Setup Time	t_{SU}	30			ns	3
Data Hold Time	t_H	10			ns	3
Propagation Delay Time High to Low Level Clear to Output	t_{PHLC}			70	ns	3
Propagation Delay Time Low to High Level Clock to Output	t_{PLH}			50	ns	3

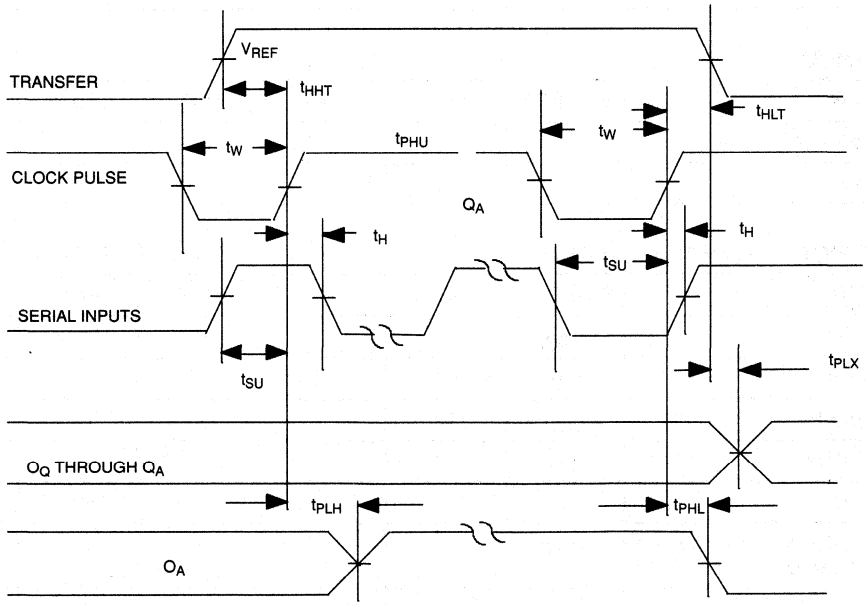
AC ELECTRICAL CHARACTERISTICS (cont'd)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Propagation Delay Time High to Low Level Clock to Output	t_{PHL}			50	ns	3
Recovering on Power-Up	t_{REC}	10			ms	
Propagation Delay Time High to Low Level Transfer to O Out	t_{PLX}			50	ns	3
Transfer High to Clock Input High	t_{HHT}	50			ns	3
Transfer Low from Clock Input High	t_{HLT}	50			ns	3

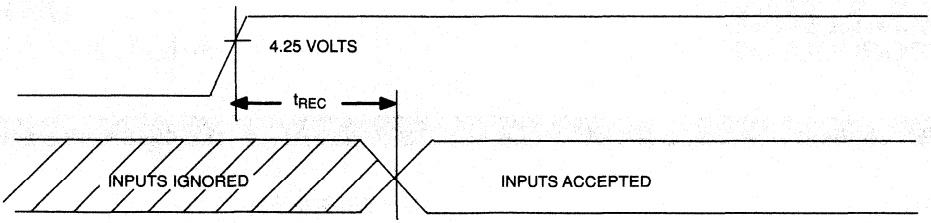
TIMING DIAGRAM: CLEAR CONTROL (3)



TIMING DIAGRAM: TRANSFER DATA (3)



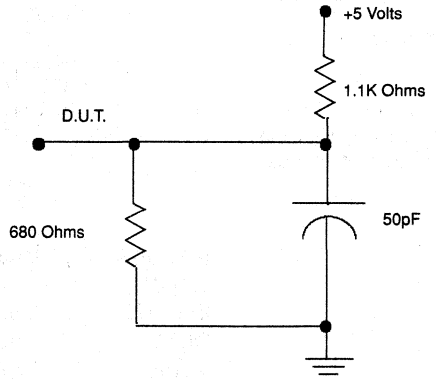
TIMING DIAGRAM: POWER-UP (3)



NOTES:

1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 4.
3. V_{REF} = 1.5 volts.
4. Clock and transfer inputs have internal pull-down resistors of 20K ohms typical. Clear has an internal pull-up resistor of 20K ohms typical.

OUTPUT LOAD Figure 4



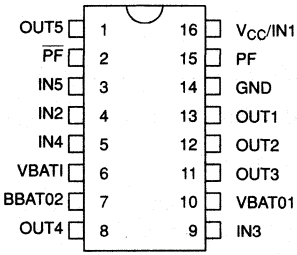
DALLAS SEMICONDUCTOR

DS1336
Afterburner Chip

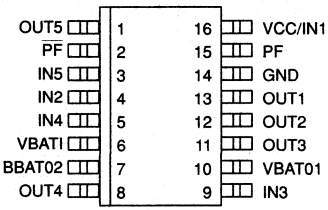
FEATURES

- Provides power switching of up to 1.5 amps at voltages between 3 and 5 volts
- Five separate power switches
- Selectable battery switches for use with battery-backed systems
- Very low on impedance of 0.7Ω
- Battery backup current of 4 mA
- Diode-isolated battery path
- Available in 16-pin DIP or 16-pin SOIC surface mount package
- Low voltage drop battery path
- Connects directly to a variety of Dallas Semiconductor devices adding increased switching capability for large battery backup current applications

PIN ASSIGNMENT



16-Pin DIP (300 mil)
See Mech. Drawing – Pg. 480



16-Pin SOIC (300 mil)
See Mech. Drawing – Pg. 484

PIN DESCRIPTION

V_{CC}/IN1	-	+5V Input and Input 1
IN2 - IN5	-	Inputs 2 - 5
OUT1 - 5	-	Outputs 1 - 5
V_{BATIN}	-	External Battery Input
V_{BAT01}	-	Diode Protected Battery Output
V_{BAT02}	-	Low Voltage Drop Battery Output
PF, $\overline{PF}$	-	Power Fail Inputs
GND	-	Ground

DESCRIPTION

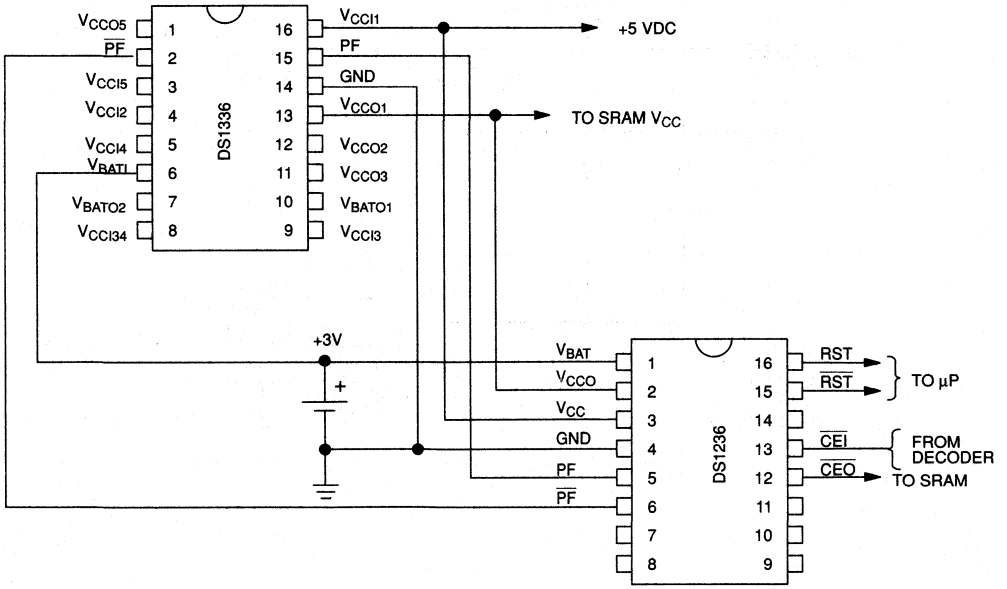
The DS1336 Afterburner Chip is designed to provide power switching between a primary power supply (V_{CC}) and a backup battery power supply (V_{BAT}). Five V_{CC} and two battery paths are provided which can be used individually or in parallel to supply uninterrupted power in applications such as SRAM networks. When used with one of the Dallas power monitoring devices listed in Section 10, Page 119, Table 1, the DS1336 allows a load to be switched from its main power supply V_{CC} to a battery backup supply when V_{CC} falls out of tolerance. A user may selectively tie together any combination of the output pins to provide the desired high current supply, providing up to 300mA per OUT pin or a maximum of 1.5A. Depending upon the user's backup supply load requirements, either of the V_{BAT} outputs may be tied to the OUT pins to supply current when V_{CC} is out of tolerance. The DS1336 switches back to the higher current V_{CC} from battery current when PF and $\overline{PF}$ become inactive.

OPERATION

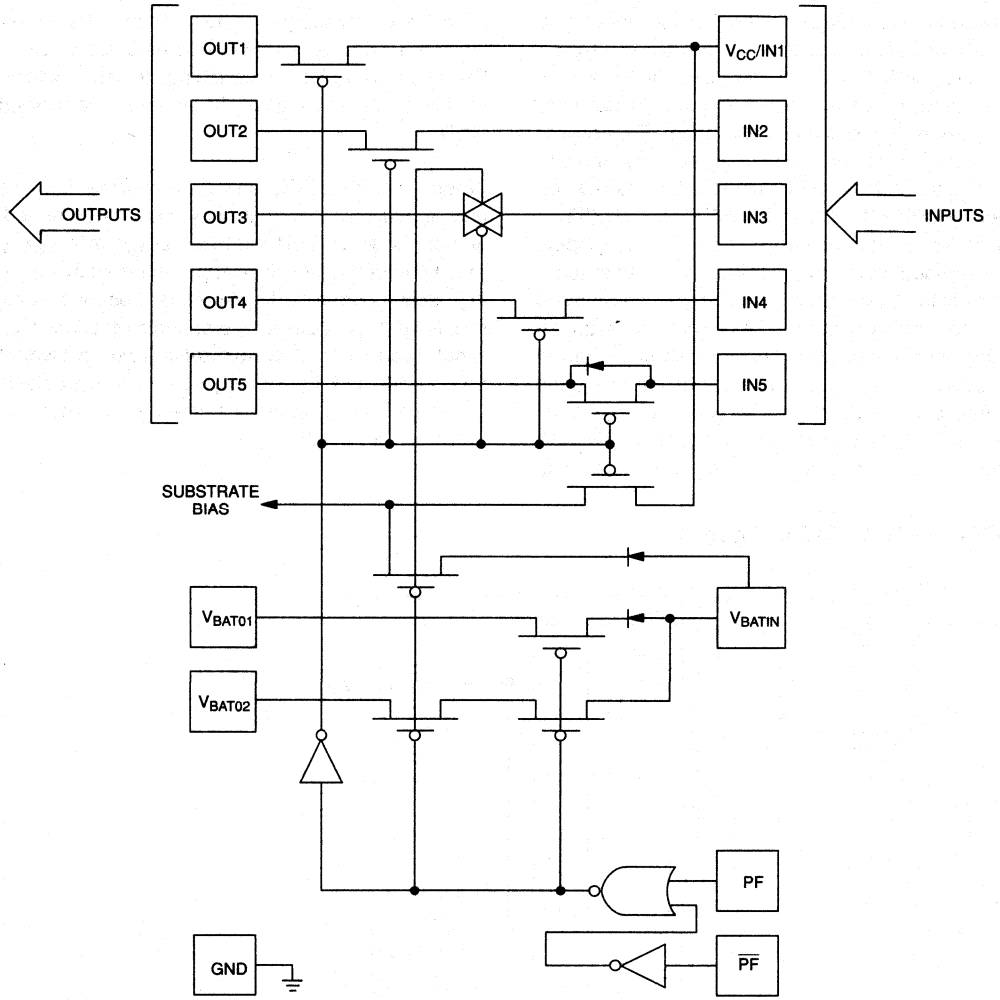
The required PF or $\overline{PF}$ input which controls the switching between the main V_{CC} and backup battery can be supplied by any of the devices listed in Table 1. All of the devices provide the DS1336 with a PF or $\overline{PF}$ signal, switching between a main supply V_{CC} and backup supply V_{BAT} when V_{CC} falls out of tolerance. For applications requiring switching from the V_{CC} supply inputs to V_{BAT}, the required PF or $\overline{PF}$ input to the DS1336 can be provided by the DS1236, DS1239, DS5001, or DS5340. For applications requiring switching from the V_{CC} inputs to the V_{BAT} input when V_{CC} begins falling out of tolerance, any of the Dallas Semiconductor devices listed in Table 1 can provide the DS1336 with the required switching input. A typical application is shown in Figure 1. For applications where switching between V_{CC} and V_{BAT} must occur at a voltage level such that V_{CC} is still greater than V_{BAT}, the OUT5 pin is recommended as it provides a diode path which will provide for a gradual transition between V_{CC} and V_{BAT}. OUT5 can be tied to the other OUTPUT pins to provide a gradual transition for all five current paths. In applications where tri-state switching is desired, OUT5 should be omitted. Only the $\overline{PF}$/PF pin is required for switching. In cases where the PF input will not be used, it should be connected to GND.

When either PF or $\overline{PF}$ is active, either of the V_{BATOX} outputs is available, although they should not be tied together (Figure 2, "DS1336 Block Diagram"). V_{BATO1} is recommended for sensitive applications such as providing backup current to timekeepers, because its diode isolated path provides for increased protection. V_{BATO2} is not recommended for applications where it would be tied to an OUTPUT pin supplying a voltage greater than that of the backup battery because V_{BATO2} is not a diode isolated current path.

TYPICAL APPLICATION Figure 1



DS1336 BLOCK DIAGRAM Figure 2



DALLAS SEMICONDUCTOR DEVICES WHICH PROVIDE PF OR $\overline{PF}$ INPUT TO DS1336 Table 1

DEVICE	SWITCH > V_{BAT}	SWITCH AT V_{BAT}	DEVICE	SWITCH > V_{BAT}	SWITCH AT V_{BAT}
DS1211	X		DS1238	X	X
DS1212	X		DS1239	X	X
DS1231	X		DS1259	X	
DS1232	X		DS1260	X	
DS1233	X		DS1610	X	
DS1233A		X	DS1632	X	
DS1233D	X		DS1833	X	
DS1234	X		DS5001	X	X
DS1236	X	X	DS5340	X	X
DS1237	X				

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC CHARACTERISTICS

(t_A = 0°C to 70°C; V_{CC} = +5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC1}	3.0	5.0	5.5	V	1
Supply Current	I_{CC1}		0.25	1	mA	
Supply Current	I_{CC2}		50	100	nA	3
Input Low Voltage	V_{IL}			0.8	V	1
Input High Voltage	V_{IH}	2.0		V_{CC}	V	1
Current Output $V_{CC}=V_{CC1}$, PF=0, $\overline{PF}$=1	I_{CCO}			300	mA	2
Current Output V_{CC}=0, PF=1, $\overline{PF}$=0	I_{BATO2}			4	mA	4
Current, Forward Bias of V_{CC5} Diode	I_{FB}			20	mA	
Off Impedance	R_{OFF1}	5			MΩ	5
Off Impedance	R_{OFF2}	10			MΩ	6
On Impedance	R_{ON1}			0.7	Ω	7
On Impedance	R_{ON2}			50	Ω	8

AC CHARACTERISTICS

(t_A = 0°C to 70°C; V_{CC} = +5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Propagation Delay	t_{PD}		10		ns	9
Switch Delay Power Fail	t_{PF}		100		ns	
Switch Delay Power On	t_{PON}			100	ns	
Capacitance PF, $\overline{PF}$	C_I			7	pF	

NOTES:

1. All voltages referenced to ground.
2. I_{CCO} with a voltage drop of 0.2V from any V_{CCO} output.
3. V_{CC}=0, V_{BATIN}=3.0V.
4. V_{BATO2} with a voltage drop of 1.0V.
5. R_{OFF1} applies to $V_{CCO1,2,3,4}$.
6. R_{OFF2} applies to $V_{BATO1,2}$.
7. Applies to V_{CCO1-5}, 300 mA.
8. Applies to $V_{BATO1-2}$, 4 mA.
9. V_{CCI3} to V_{CCO3} delay when used as chip enable control for write protection of a memory device. In this application a current 8 mA source current on V_{CCI3} with 50 pF load on V_{CCO3} can be accommodated.

DALLAS SEMICONDUCTOR

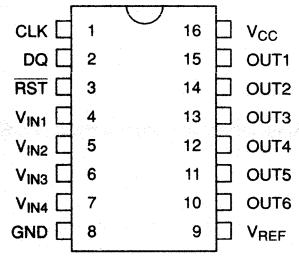
DS1611
Programmable System Monitor

FEATURES

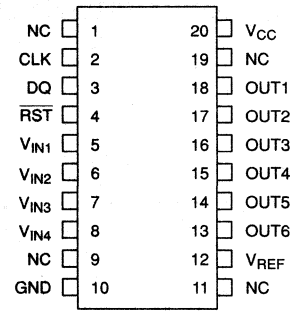
- Monitors tolerance of up to four different supply voltages, between 2.7V to 18V
- Provides six programmable voltage monitoring outputs OUTX
- All monitor settings are maintained in the absence of power in a backup EEPROM array
- System access is through 3–wire serial interface
- Available in an industrial temperature operation range of –40°C to +85°C
- Operates from single 2.7 to 5.5 volt supply
- 1.25V voltage reference output
- Voltage trip points for each OUTx output are user–programmable

OUTPUTS	VOLTAGE RANGE	RESOLUTION
1, 2, 3	2.7V to 6V	100 mV
4, 5, 6	6V to 12V	250 mV
4, 5, 6	12V to 18V	500 mV

PIN ASSIGNMENT



16–PIN DIP OR SOIC



20–PIN TSSOP

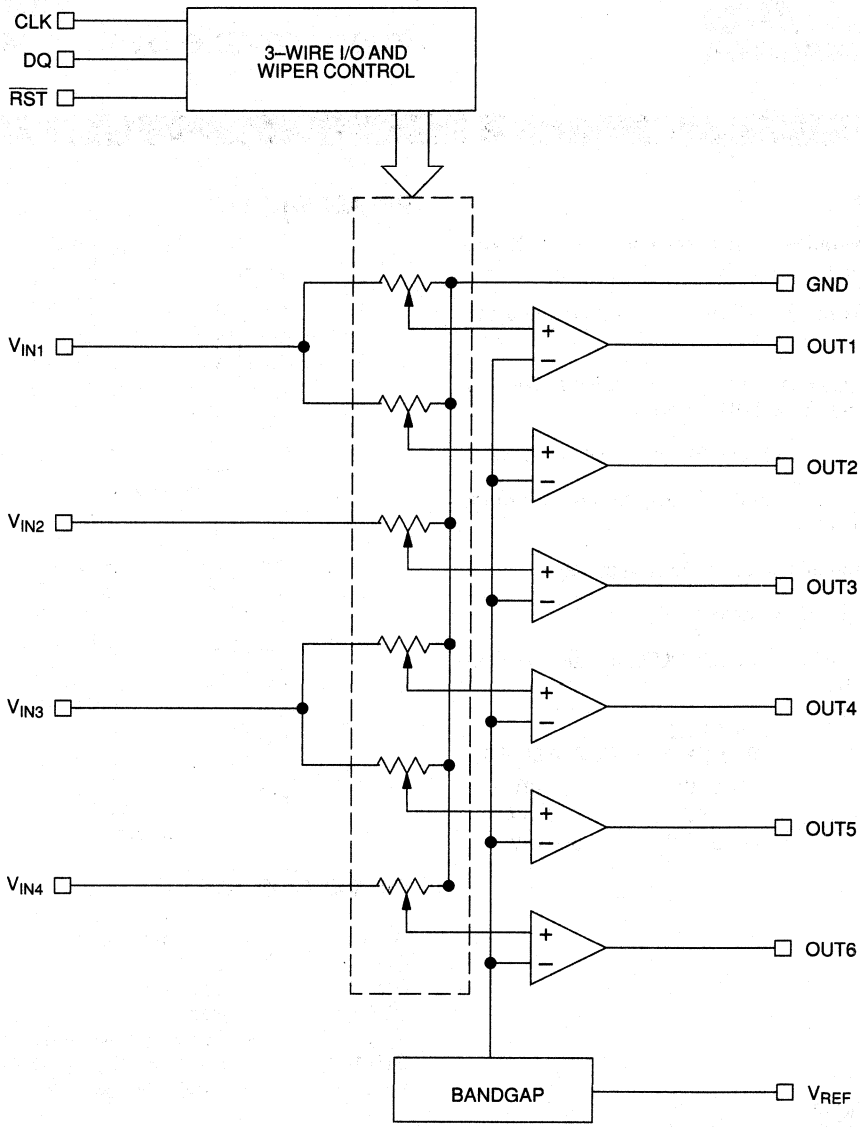
PIN DESCRIPTION

V_{CC}	– Supply Voltage
GND	– System Ground
CLK	– Clock
DQ	– Data I/O
$\overline{RST}$	– Reset
V_{IN1-4}	– Power Supply Monitor Inputs
OUT1–6	– Power Supply Monitor Outputs
V_{REF}	– 1.25V voltage reference

DESCRIPTION

The DS1611 Programmable System Monitor provides critical system power supply monitoring functions for four independent power supply inputs. A precision temperature–compensated reference and comparator circuit is used to monitor the status of the power supplies (V_{IN} 1–4). Users may program the DS1611 to monitor the input voltages for voltage–in–tolerance for any voltage between 2.7V and 18V. When an out–of–tolerance condition is detected, an internal power fail signal is generated which forces the corresponding OUTX output to the active state. When the voltage input returns to an in–tolerance condition, the OUTX signal is kept in the active state for approximately 200 ms to allow the power supply and processor to stabilize. Multiple user programmable OUTX outputs are provided so that a system can monitor its supplies over a range of voltages to execute an orderly system shutdown during a power brownout or failure. The DS1611 also provides a 1.25V voltage reference output.

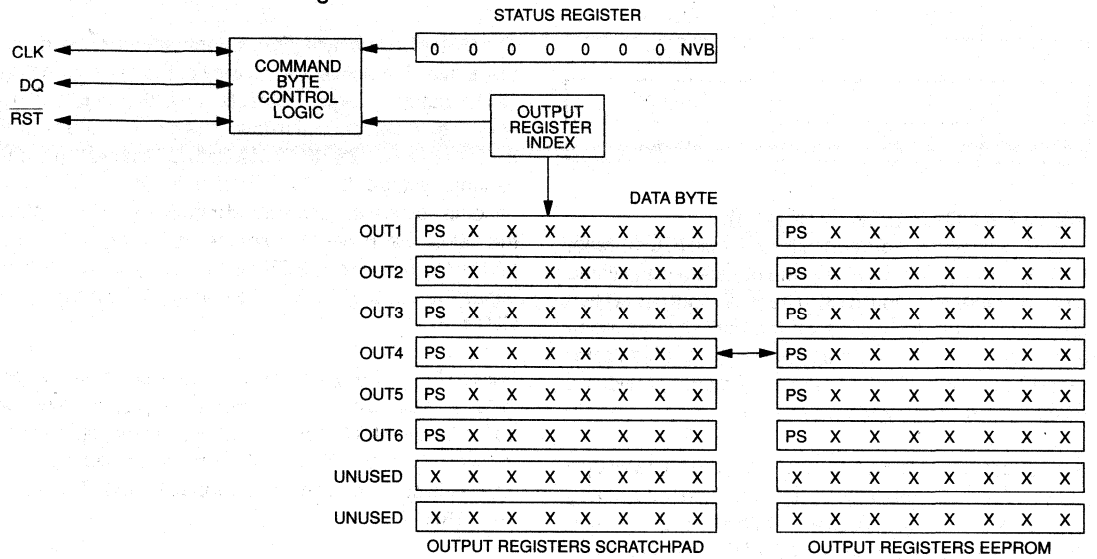
DS1611 FUNCTIONAL BLOCK DIAGRAM Figure 1



OPERATION

The user programmable voltage monitor trip point settings are maintained in scratchpad during normal operation and can be transferred to an EEPROM array for nonvolatile storage in the absence of power. The scratchpad memory locations can be individually read and written as needed, but the EEPROM can only be read or written via block transfers to and from the scratchpad. Block transfers, status register reads, and scratchpad accesses are all initiated by a command byte (see Table 1). Scratchpad accesses and status register read operations require that additional data be read or written following the command byte. The command byte is always input starting with the LSB (bit 0).

REGISTER STRUCTURE Figure 2



COMMAND BYTE

Each data transfer is initiated by a command byte (see Table 1). The MSB of bit 7 is reserved for internal use and must be logic 1 for all valid operations. The lower seven bits of the command byte specify what type of data transfer is to be performed. These bits must be set to the value 0101010 for a block transfer from scratchpad to EEPROM (EEPROM write) or to the value 1000101 for a block transfer from EEPROM to scratchpad (EEPROM read). To read or write a single output register in the scratchpad, bits 6, 5, and 4 of the command byte should be set to 111 with bits 3, 2, and 1 (A2, A1, A0) containing the binary address of the output register to be indexed. Table 2, Output Register Index shows where the six output registers are mapped in the scratchpad memory space. Bit 0 (R/$\overline{W}$) specifies whether a read or write operation to the scratchpad is to be performed. R/$\overline{W}$ must be logic 1 for a read operation or logic 0 for a write operation. Note that after bit 7 of a block transfer command byte is written, $\overline{RST}$ must transition low.

COMMAND BYTE Table 1

COMMAND	7	6	5	4	3	2	1	0
EEPROM Read (Block Transfer)	1	1	0	0	0	1	0	1
EEPROM Write (Block Transfer)	1	0	1	0	1	0	1	0
Scratchpad Read/Write (Single Byte)	1	1	1	1	A2	A1	A0	R/$\overline{W}$
Scratchpad Read/Write (Burst)	1	1	1	0	0	0	0	R/$\overline{W}$
Read Status Register	1	1	0	1	1	0	1	1

A2, A1, A0 = Output Register Index R/$\overline{W}$ = Read/Write Bit

OUTPUT REGISTER INDEX Table 2

A_2	A_1	A_0	OUTX
0	0	0	OUT1
0	0	1	OUT2
0	1	0	OUT3
0	1	1	OUT4
1	0	0	OUT4
1	0	1	OUT6
1	1	0	Unused
1	1	1	Unused

RESET AND CLOCK CONTROL

The 3–wire serial port consists of clock (CLK), reset ($\overline{RST}$), and data I/O (DQ). All data transfers are initiated by driving the $\overline{RST}$ input high. The $\overline{RST}$ input serves two functions. First, $\overline{RST}$ turns on the control logic which allows access to the shift register for the address/command sequence. Second, the $\overline{RST}$ signal provides a method of terminating data transfers.

A clock cycle is a sequence of falling edge followed by a rising edge. For data inputs, data must be valid during the rising edge of the clock and data bits are output on the falling edge of the clock. If the $\overline{RST}$ input is low all data transfer terminates and the DQ pin goes to a high impedance state. At power–up, $\overline{RST}$ must be a logic 0 for t_{REC} after V_{CC} rises above 2.7 volts. Also, CLK must be a logic 0 when $\overline{RST}$ is initially driven to a logic 1 state.

SCRATCHPAD WRITE/READ

Following the eight CLK cycles that specify a scratchpad write command, a scratchpad data byte (see Table 3) is input on the rising edge of the next eight CLK cycles. Additional CLK cycles are ignored should they inadvertently occur. Data is input starting with the LSB (bit 0).

Following the eight CLK cycles that specify a scratchpad read command, a scratchpad data byte is output on the falling edge of the next eight CLK cycles. Note that the first data bit to be transmitted occurs on the falling edge after the last bit of the command byte is written. Additional CLK cycles are ignored should they inadvertently occur. Also, the DQ pin is tristated upon each rising edge of CLK. Data is output starting with the LSB (bit 0).

The MSB of a data byte (PS), polarity select, determines the active high/active low polarity of the corresponding OUTX output. Logic 1 selects an active high setting while logic 0 selects active low. The binary value held in the lower seven bits (INC) of a data byte specify a comparison voltage for that voltage input. OUTX will become active if the associated input votlage falls below this value. Each increment of the OUTX registers adds 100 mV to the minimal 2.7V trip points of the OUT1–3 or either 250 mV or 500 mV to the minimal 6.0V trip point of OUT4–6.

For OUT1–3, the reference voltage is computed to be 2.7V + (100 mV * INC). For example, a value of 10000000 in OUT2 indicates an active high trip point of 2.7V + (100 mV * 0) = 2.7V. A value of 00010010 in OUT3 indicates and active low trip point of 2.7V + (100 mV * 18) = 4.5V.

Foru OUT4–6, the reference voltate is 6V + (250 mV * min(INC, 24)) + (500 mV * max (INC – 24, 0)). In other words, the first 24 increments are 250 mV in size and increments thereafter are 500 mV in size. For example, a value of 00100000 in OUT6 indicates an active low trip point of 6V + (250 mV * 24) + (500 mV * 8) = 16V.

Binary INC values in OUT1–3 should not exceed 0100001, corresponding to 2.7V + 3.3V or the maximum 6V trip point, nor should INC values in OUT4–6 exceed 0100100, corresponding to 6V + 12V or the maximum 18V trip point. Binary INC values greater than these will be accepted but will set the trip points to the maximum trip point voltage, either 6V or 18V.

SCRATCHPAD DATA Table 3

		INC							
A2–A0	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
000	PS	X	X	X	X	X	X	X	OUT1
001	PS	X	X	X	X	X	X	X	OUT2
010	PS	X	X	X	X	X	X	X	OUT3
011	PS	X	X	X	X	X	X	X	OUT4
100	PS	X	X	X	X	X	X	X	OUT5
101	PS	X	X	X	X	X	X	X	OUT6
110	X	X	X	X	X	X	X	X	Unused
111	X	X	X	X	X	X	X	X	Unused

PS = Polarity Select Bit
Note: On power–up, data in the EEPROM is automatically transferred to scratchpad.

BURST MODE

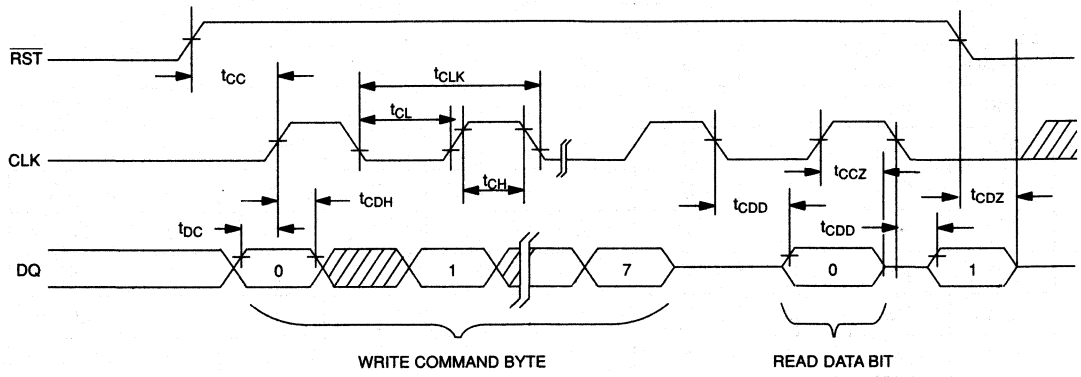
Scratchpad read and write burst modes may be specified by the command byte. Burst mode permits continuous read and write capability. Reads or writes in burst mode start with bit 0 of OUT1 output register and will continue through address 111 and wrap around continuously until $\overline{RST}$ is asserted low. Single byte and burst modes are illustrated in Figure 5.

3-WIRE INTERFACE

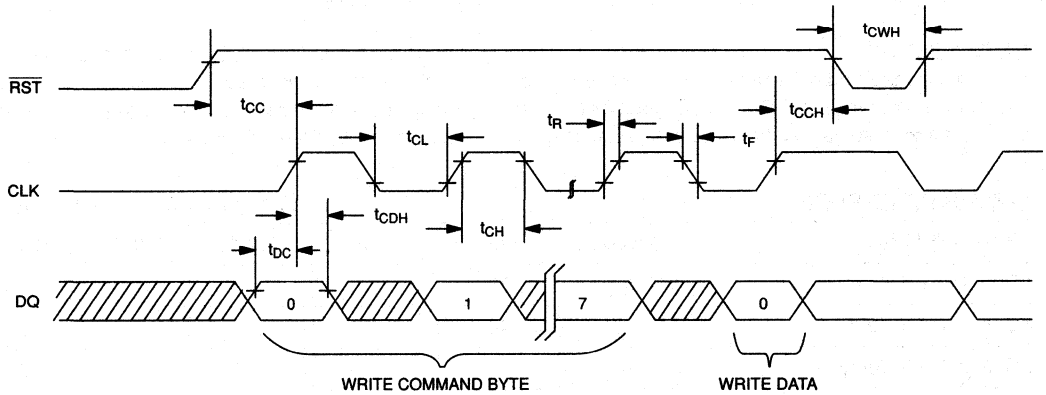
(0°C to 70°C; V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	5
CLK to Data Hold	t_{CDH}	40			ns	5
CLK to Data Delay	t_{CDD}			100	ns	5, 6, 7
CLK Low Time	t_{CL}	250			ns	5
CLK High Time	t_{CH}	250			ns	5
CLK Frequency	t_{CLK}	DC		2.0	MHz	5
CLK Rise & Fall	t_R,t_F			500	ns	
$\overline{RST}$ to CLK Setup	t_{CC}	1			µs	5
CLK to $\overline{RST}$ Hold	t_{CCH}	60			ns	5
$\overline{RST}$ Inactive Time	t_{CWH}	250			ns	5
CLK to DQ High Z	t_{CCZ}			50	ns	5
$\overline{RST}$ Inactive Time	t_{CEH}	20			ms	5, 8
RST to DQ High Z	t_{CDZ}			50	ns	5

TIMING DIAGRAM: SCRATCHPAD READ Figure 3

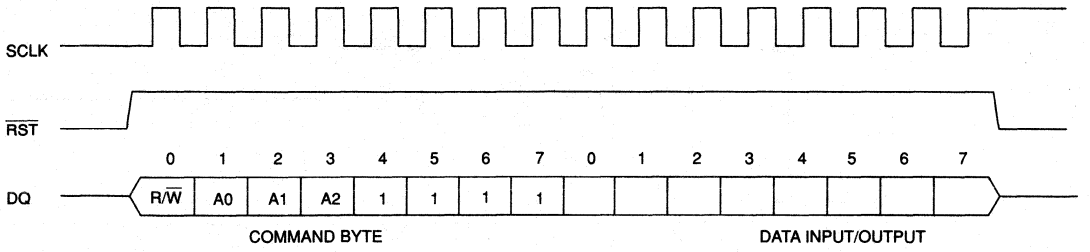


TIMING DIAGRAM: SCRATCHPAD WRITE Figure 4

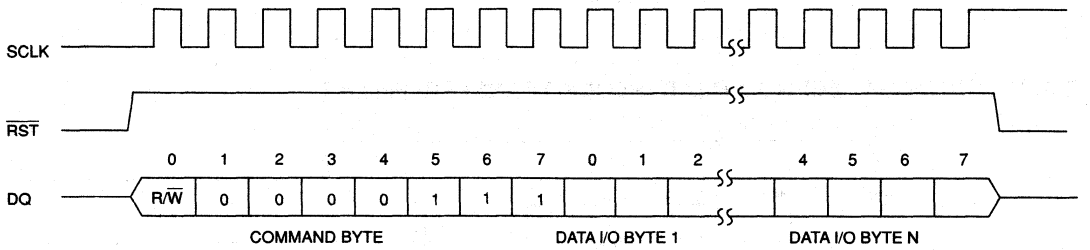


SCRATCHPAD READ/WRITE SUMMARY Figure 5

SINGLE BYTE READ/WRITE



BURST MODE READ/WRITE



BLOCK TRANSFER

Data is transferred to the output registers scratchpad from the output registers EEPROM following a EEPROM read (block transfer) command word. An EEPROM write (block transfer) will transfer data from the output registers scratchpad to the output registers eeprom. $\overline{RST}$ should be asserted low for t_{CEH} following an EEPROM write to ensure completion of EEPROM write. Another way of checking the status of the EEPROM output registers is by reading the status registers.

STATUS REGISTER

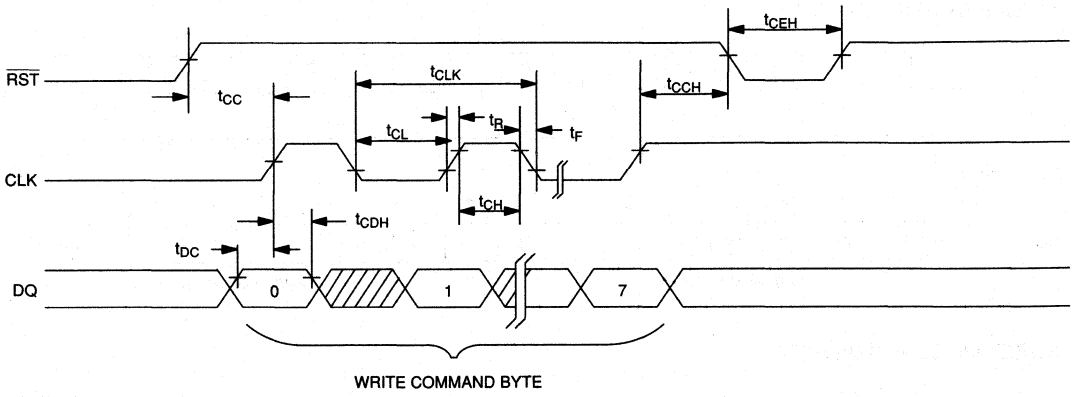
The LSB (bit 0) of the status registers contains a nonvolatile busy flag (MVB). This bit specifies whether an EEPROM write block transfer is in progress (see Table 4). Following the eight CLK cycles that specify a status register read cycle, the status register is output on the falling edge of the next eight CLK cycles. A status register read occurs exactly as a scratchpad read and data is output starting with LSB (bit 0).

STATUS REGISTER (READ ONLY) Table 4

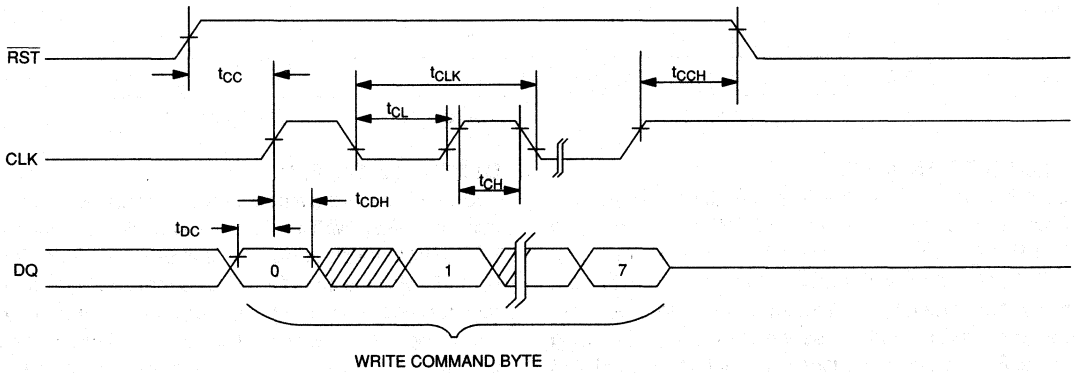
7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	NVB	Status Register

NVB = Nonvolatile Busy Flag (write to EEPROM in process)
"1" = Copy from scratchpad to EEPROM in progress
"0" – EEPROM is not busy
NOTE: A copy to EEPROM may take from 2 ms to 20 ms (taking longer at lower supply voltages).

TIMING DIAGRAM: EEPROM WRITE (BLOCK TRANSFER) Figure 6



TIMING DIAGRAM: EEPROM READ (BLOCK TRANSFER) Figure 7



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{IN3-4} in Reference to Ground	–0.3V to +20.0V
Voltage on All Other Pins in Reference to Ground	–0.3V to +7.0V
Operating Temperature	–40°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	2.7		5.5	V	1
Voltage Monitors	V_{IN1}–V_{IN2} V_{IN3}–V_{IN4}	0.0 0.0		6.6 19.6	V V	1 1
Logic 1	V_{IH}	2.0		V_{CC}+0.3	V	1
Logic 0	V_{IL}	–0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=2.7V to 5.5V)

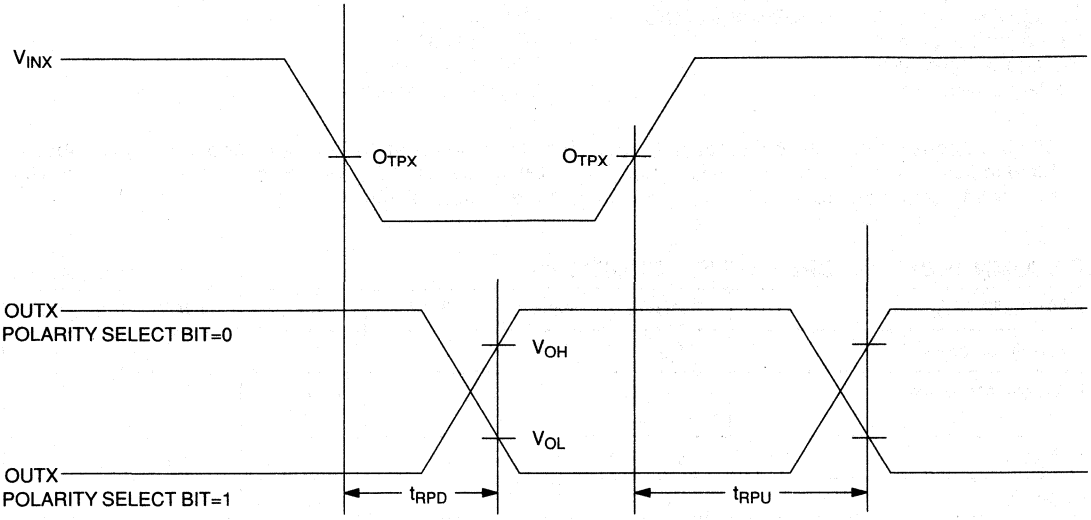
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	–1.0		+1.0	µA	
Voltage Monitor Input Current V_{IN1-4}	I_{VM}	–5.0		+5.0	µA	
Output Current @ 2.4V	I_{OH}	–1.0			mA	
Output Current @ 0.4V	I_{OL}			2.0	mA	
Operating Current	I_{CC}			400	µA	2
OUT1–3 Voltage Trip Points	O_{TP1-3}	2.7		6.0	V	1, 3
OUT4–6 Voltage Trip Points	O_{TP4-6}	6.0		18.0	V	1, 4

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			10	pF	

TIMING DIAGRAM: V_{INX} FALLING OUT OF TOLERANCE Figure 8



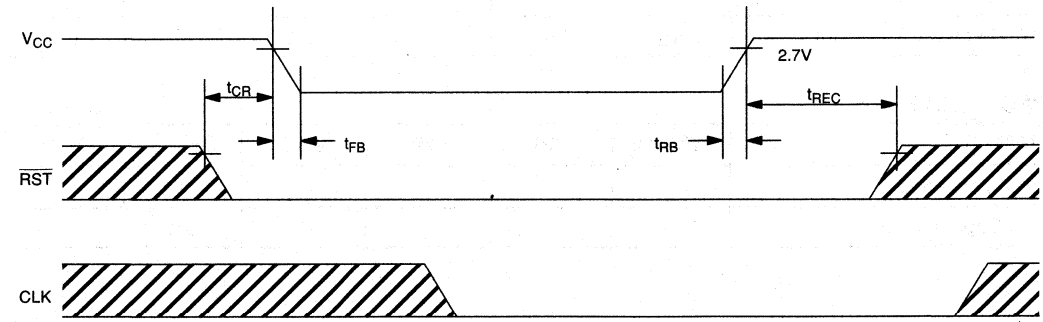
V_{INX} POWER SENSING

($0°C$ to $70°C$; V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{INX} Detect to $\overline{OUTX}$ Active	t_{RPD}			100	µs	
V_{INX} Detect to $\overline{OUTX}$ Inactive	t_{RPU}	100	200	300	ms	

NOTE: V_{CC} must be stable to ensure proper power sensing.

TIMING DIAGRAM: POWER DOWN/UP Figure 9



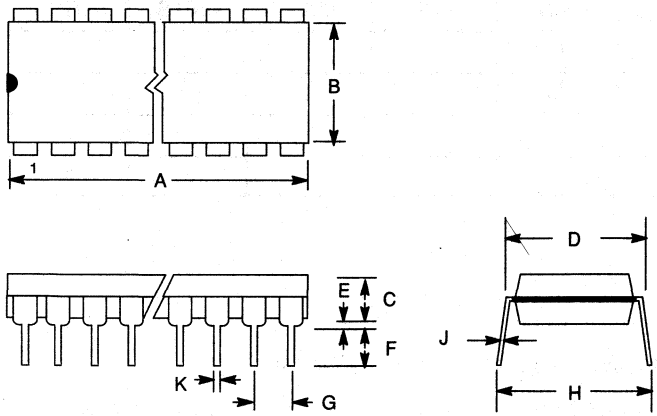
(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Slew Rate Power Down	t_{FB}	0			µs	
V_{CC} Slew Rate Power Up	t_{RB}	30			µs	
Recovery at Power Up	t_{REC}			1	ms	
$\overline{RST}$ Inactive before Power Down	t_{RC}	10			ms	9

NOTES:

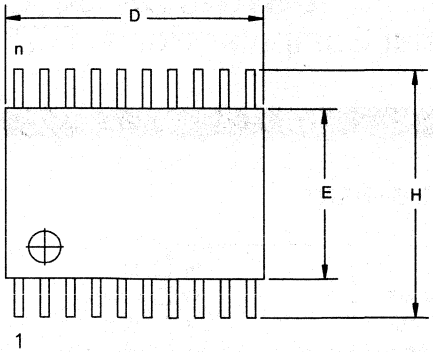
1. All voltages referenced to ground.
2. Measured with outputs open.
3. OUT1–OUT3 trip points can be varied between 2.7V and 6V in 100 mV increments.
4. OUT4–OUT6 trip points can be varied between 6V and 12V in 250 mV increments or between 12V and 18V in 500 mV increments.
5. V_{IH}=2.0V or V_{IL}=0.8V with 10 ns maximum rise and fall times.
6. V_{OH}=2.4V and V_{OL}=0.4V.
7. Load capacitance = 50 pF.
8. t_{CEH} must be met to ensure data integrity.
9. t_{CR} must be met following an EEPROM write to ensure data integrity.

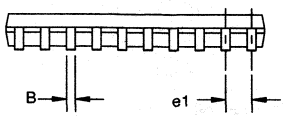
16–PIN DIP (300 MIL)

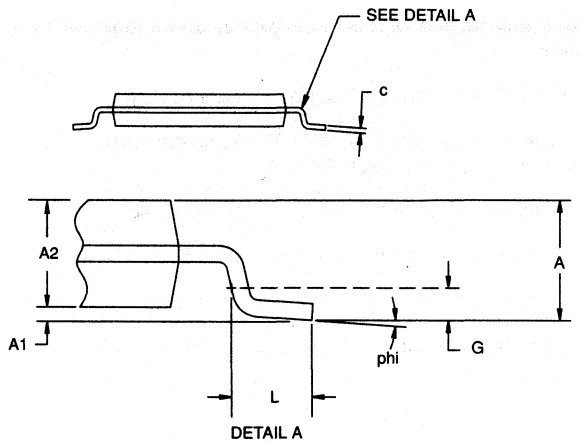


PKG	16-PIN	
DIM	MIN	MAX
A IN. MM	0.740 18.80	0.780 19.81
B IN. MM	0.240 6.10	0.260 6.60
C IN. MM	0.120 3.05	0.140 3.56
D IN. MM	0.300 7.62	0.325 8.26
E IN. MM	0.015 0.38	0.040 1.02
F IN. MM	0.120 3.04	0.140 3.56
G IN. MM	0.090 2.29	0.110 2.79
H IN MM	0.320 8.13	0.370 9.40
J IN MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

DS1611 20-PIN TSSOP







DIM	MIN	MAX
A MM	–	1.10
A1 MM	0.05	–
A2 MM	0.75	1.05
c MM	0.09	0.18
L MM	0.50	0.70
e1 MM	0.65 BSC	
B MM	0.18	0.30
D MM	6.40	6.90
E MM	4.40 NOM	
G MM	0.25 REF	
H MM	6.25	6.55
phi	0°	8°

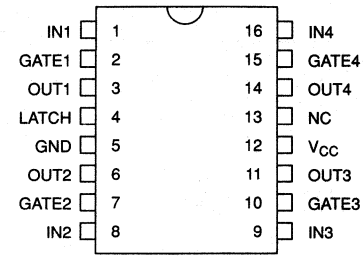
DALLAS SEMICONDUCTOR

DS1640/DS1640C
Personal Computer Power FET

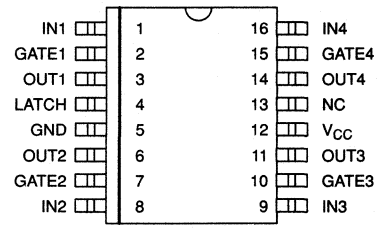
FEATURES

- Contains four P channel power FET switches that can each supply over 300 mA @ 0.2 volts drop
- Controlled directly from CMOS or TTL level signals
- Fast switching time of less than 10 µs at rated supply current
- 16-pin DIP or 16-pin SOIC surface mount package
- Positive logic signal turns each FET on and ground or low level signal turns each FET off
- Off condition allows less than 50 nA of current flow
- Low control gate capacitance of less than 5 pF
- FET gates can either follow inputs or be latched
- Designed for use with power supplies ranging from +3 to +5 volts

PIN ASSIGNMENT



16-Pin DIP (300 Mil)
See Mech. Drawing – Pg. 480



16-Pin SOIC (300 Mil)
See Mech. Drawing – Pg. 484

PIN DESCRIPTION

V_{CC}	-	+3 to +5 Volt Input
GND	-	Ground
IN1-IN4	-	FET Sources
OUT1-OUT4	-	FET Drains
GATE1-GATE4	-	FET Control Gates
NC	-	No Connection
LATCH	-	Gate Inputs Latch Control

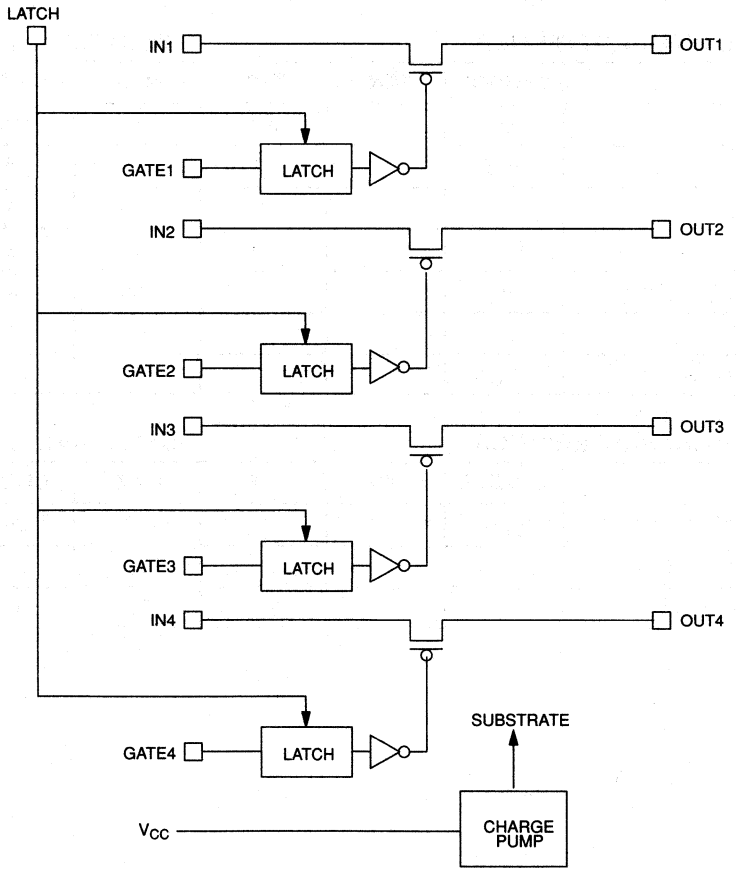
DESCRIPTION

The DS1640 contains four P channel power MOS FET's designed as switches to conserve power in personal computer systems. When connected to power management control units, power consuming devices like disk drives or display panel backlights can be routinely shut down to conserve battery or main power supply energy. The P channel power MOS FET's are individually controlled and are capable of handling 300 mA each continuously with less than 0.2 volts drop from input to output. The device requires a +3 → +5 volt power supply input which is used to power internal logic and to operate a gate bias generator.

OPERATION

With +3 ➛ +5 volts applied between the V_{CC} pin and ground, any one of four inputs can be connected or disconnected from its respective output based on the bias applied to the control gate (see Figure 1). A set of four internal latches is controlled by the latch input. The logic levels passed to the FET gates are controlled by the gate inputs and latch pin status. When the latch pin is logic 0, the gate input levels are inverted and passed directly to the control gates, enabling the switches to be switched both independently and asynchronously. With a transition from logic 0 to logic 1 on the latch pin, the input levels present on the gate inputs are locked by the four internal latches, maintaining the corresponding FET gates at those levels. As long as the latch input is maintained at logic 1, the FET gate levels are maintained. When the latch input is returned to logic 0, the gate inputs again are inverted and passed to the FET control gates without being latched. A TTL or CMOS logic 1 turns a switch completely on and TTL or CMOS logic 0 turns a switch completely off. The four switches can be operated independently or two or more can be connected in parallel for added current carrying capability. The four switches contained within the DS1640 are not designed to be operated in a linear manner. When V_{CC} is not applied to the DS1640 or if V_{CC} is not within nominal limits, the output levels and current carrying capability of the four switches are not guaranteed. When all four gate inputs are off (logic 0) the device enters a low V_{CC} current standby mode because the onboard charge pump is turned off. The gate and latch inputs are CMOS-compatible throughout the entire V_{CC} range and are TTL-compatible when V_{CC} falls between 4.5 and 5.5V.

DS1640 BLOCK DIAGRAM Figure 1



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	3.0		5.5	V	1, 2
Logic 0 Input 3.0 V ≤ V_{CC} ≤ 4.5 V	V_{IL2}	-0.3		+0.5	V	
Logic 0 Input 4.5 V ≤ V_{CC} ≤ 5.0 V	V_{IL1}	-0.3		+0.8	V	1
Logic 1 Input 3.0 V ≤ V_{CC} ≤ 5.0 V	V_{IH}	2.0		V_{CC}+0.5	V	1, 7
Source Voltage	V_{SOURCE}			V_{CC}+0.5	V	1, 7

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = +5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC1}		0.3	1	mA	3
Supply Current	I_{CC2}		0.1	1	µA	4
Switch Off Leakage	I_{SL}			100	nA	
Switch On Resistance	R_{ON}		0.3	.67	Ω	
Switch Current @ V_F = 200 mV	I_S			300	mA	5
Input Leakage	I_{IL}	-1		+1	µA	6
Gate Input Capacitance	C_G			5	pF	7

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = +5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Switching Time (OFF ON)	t_{STON}			10	µs	
Switching Time (ON OFF)	t_{STOFF}			10	µs	
Minimum Time to Engage Latch	t_{LM}			50	ns	

NOTES:

1. All voltages are referenced to ground.
2. When V_{CC} is below minimum limits output levels are not guaranteed.
3. I_{CC1} is the supply current with one or more switches on.
4. I_{CC2} is when all switches are off and all inputs are within 0.5V of a supply rail.
5. Each switch is capable of carrying 300 mA maximum at 200 mV forward drop.
6. Input leakage applies to the four gate inputs and the latch input only.
7. Applies to each of four gate inputs and the latch input.

Dallas Semiconductor devices are built to the highest quality standards and manufactured for long term reliability. All DS1640 devices are made using the same quality materials and manufacturing methods. However, consumer versions of the DS1640 are not exposed to environmental stresses that some commercial device manufacturing flows require. Devices that are designated as consumer product have a "C" designator in the product number. For example, the DS1640C is a consumer grade product.

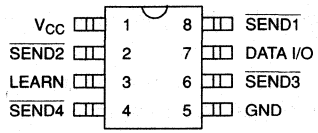
DALLAS SEMICONDUCTOR

DS1651
3-Code Lock
DS1652
Key Match Memory System

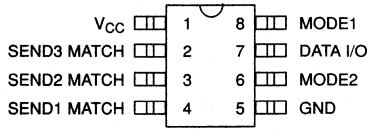
FEATURES

- The two–chip lock and key system forms the basis of a secure access system
- The match memory system is compatible with a variety of RF, serial, ultrasound, and optical transmission media
- The user–programmable 64–bit code or internally generated random 64–bit code prevents unauthorized copying of keys
- Each key and lock system is capable of generating and recognizing 3-code match conditions
- Keys are programmed from lock codes only under controlled user access/secure conditions
- Low–cost, economical
- Lock codes can be changed as many times as necessary
- 3V operation, 5V for programming
- Operating range of -25°C to +85°C
- All stored 64–bit codes in the lock and key are nonvolatile and retain the security code in the absence of power
- Applications include building entry, garage door openers, automobile entry and ignition, and local and remote identification

PIN ASSIGNMENT



DS1652 8-Pin DIP (300 Mil) and
DS1652S 8-Pin SOIC (200 Mil)
See Mech. Drawings
Pgs. 480 & 483



DS1651 8-Pin DIP (300 Mil) and
DS1651S 8-Pin SOIC (200 Mil)
See Mech. Drawings
Pgs. 480 & 483

DS1652 PIN DESCRIPTION

GND	-	Ground
DATA I/O	-	Serial Data Input/Output
$\overline{\text{SEND1}}$	-	Send Input 1
$\overline{\text{SEND2}}$	-	Send Input 2
$\overline{\text{SEND3}}$	-	Send Input 3
$\overline{\text{SEND4}}$	-	Send Input 4
LEARN	-	Learn Input

DS1651 PIN DESCRIPTION

MODE2	-	Function Control Pin
MODE1	-	Function Control Pin
V_{CC}	-	+3V to +5V Input
GND	-	Ground
DATA I/O	-	Serial Data Input/Output
SEND1 MATCH	-	Code Match Signal for SEND1
SEND2 MATCH	-	Code Match Signal for SEND2
SEND3 MATCH	-	Code Match Signal for SEND3

DESCRIPTION

The DS1651 Lock and DS1652 Key operate in combination to limit access of any secure system or area to keyholders. Both the DS1651 Lock and DS1652 Key contain a 64–bit memory which acts as the security code, controlling access. The code memory within the DS1651 Lock can be user–programmed with a known 64–bit code, or the DS1651 can generate a 64–bit code from a random number generator within the DS1651. Once set, the code is nonvolatile and can then be transferred to one or more DS1652 Key(s) under secure conditions.

To gain access to the lock, the key's code must be transmitted to the lock via some user transmission media such as RF, optical, IR, ultrasound, or another serial medium. Upon receiving a transmission of a 64–bit key code, a DS1651 Lock will compare the requesting key's 64–bit code to the lock's programmed 64–bit code. If the key code matches the lock code, the lock generates a match signal, which can be used to allow access to the secure system.

OPERATION DS1651 LOCK

The main functional components of both the DS1651 and DS1652 are shown in Figures 3 and 4. The diagrams show that the internal functions of the lock and key are similar. From Figure 3, the primary components of the lock are its 64–bit–wide registers. The 64–bit code memories are the physical "lock" and contain the pattern against which all keys are measured for access. The 64–bit data memory records the 64–bit pattern transmitted by a potential key. The pulse input interpreter and reset generator accepts serial input data from the input pin.

The DS1651 Lock has four functional modes, which are controlled by the lock's mode control pins. The four modes are defined as follows:

MODE2	MODE1	FUNCTIONAL MODE
0	0	Operation Mode: Receiving codes from key(s).
0	1	Learn Mode: Program with user–provided 64–bit codes.
1	0	Duplicate Mode: Transmit 64-bit code memory contents.
1	1	Learn Mode: Program with internally generated, random 64 bits.

The Learn and Duplicate modes can only be entered from Operation mode. The DS1651 samples the level of MODE1 and MODE2 10 ms after a transition on either pin. This sample is used to tell the DS1651 in which mode it should be operating.

In the Learn modes, the DS1651 Lock's code memory can be either programmed directly by the user or programmed using a random set of 1's and 0's created by the DS1651's random number generator. A user must have physical access to the DS1651 to place it in Learn mode. To place the DS1651 Lock in Learn mode, the DS1651's V_{CC} input must be at 4.5V minimum with MODE1 or both MODE1 and MODE2 pins driven high, telling the DS1651 to enable the contents of its code memory to be rewritten. If MODE1 is high, then the DS1651 enables its code memory to be rewritten using a user–defined 64–bit code, which it expects to see on its data I/O pin. At the end of sending the 64–bit code to the DS1651, the mode pins must both be driven low, returning the lock to operation mode, before entering any other mode. (See timing diagram "Learn Modes DS1651 Lock.") If MODE2 and MODE1 are high, then the DS1651 Lock performs an internal operation in which it uses its internal random number generator to create a 64 bit pattern of 1's and 0's and loads it into the code data memory, from LSB to MSB. When all 64 bits have been written, the DS1651 has a new code memory that can be programmed into DS1652 Keys. After this operation is completed, the mode pins must both be driven low to return the DS1651 to operation mode, before entering any other mode.

The DS1651 will not reprogram its 64–bit code memory using its internal random number generator until another transition from 0 to 1 is seen on both its MODE2 and MODE1 pins.

For the DS1651 Lock to transfer its code memory into a DS1652 Key, the DS1651 must be in Duplication mode. To enter Duplication mode, the MODE2 pin must be driven high. The transition from 0 to 1 on the MODE2 pin and its maintenance at 1 causes the DS1651 Lock to transmit a reset signal followed by its 64–bit code memory through its data input/output pin. The lock will transmit the code only once. If another transmission is required, the mode pin must be driven to zero before being returned to 1 to send another 64–bit code copy. The data input/output pin of the DS1651 Lock must be physically connected to the data input pin of the target DS1652 Key in order to transfer a code from the lock to a key to be used with that lock. The target key must also be in Learn mode (see the section entitled "Operation DS1652 Key") for the key to accept as code the information transmitted by the lock. With these timing and hardware conditions satisfied, DS1652 Key programming can be performed quickly (<1 s) and easily with only one serial connection between the DS1651 and DS1652.

The DS1651 Lock is in its operation mode with its mode pins inactive. The receipt of a signal on the input/output pin which is active high for at least 720 µs is treated as a reset signal from a key about to transmit its code. The interpreted pattern of 1's and 0's sampled in the 2 ms

wide windows is written into the data memory for comparison to the lock's code memories. If the comparison shows a match with one of the memories, then the DS1651 drives the appropriate SENDX MATCH signal. If the code does not match, the DS1651 performs no operations, but waits for the next reset signal.

OPERATION DS1652 KEY

The operation of the DS1652 Key is similar to that of the DS1651 (Figure 4). The key is programmed with code generated by the DS1651 Lock with the lock in Duplication mode and the key in Learn mode.

For the DS1652 Key to be programmed, the LEARN pin must be driven active high. The DS1652 Key's data input pin must be physically connected to the DS1651 Lock's data input/output pin for the DS1652 Key to successfully accept a code from a DS1651 Lock. Once connected and in the Learn mode, the DS1652 Key is ready to accept its 64–bit code. The DS1652 Key will recognize the 720 µs wide active high reset signal and will use the rising edge of each subsequent signal to determine the contents of 64 consecutive 2 ms wide data windows as logic 1 or logic 0. The contents of the 64 consecutive windows, transmitted by the lock, become latched into the nonvolatile 64–bit code memory of the DS1652 Key. The key will perform no other operations until the LEARN pin becomes inactive, returning the DS1652 to its operation mode. The DS1652 Key will transmit a reset signal and its code memory out of its data output pin a maximum of three times as long as the $\overline{\text{SENDX}}$ input is asserted. The DS1652 Key will transmit a version of the code that is specifically tailored to the $\overline{\text{SENDX}}$ input being triggered. (See diagram entitled "DS1691 Lock, Match Signals.")

SERIAL PULSE PROTOCOL

The DS1651 and DS1652 transmit and receive data serially, according to the protocol listed in the timing diagrams.

The transmission and reception of data begins with the rising edge of the 720 µs reset signal. The DS1651 and DS1652 then begin looking for data in 2 ms windows. Each data window begins with the rising edge of a pulse. The duration of the pulse determines whether a logical one or logical 0 is present in that window (logical one pulse duration is six times as long as logical zero pulse duration).

For 128 ms, the DS1651 or DS1652 will time the duration of the active pulse in each window. Once the pulse is interpreted as a 1 or a 0, the data bit is written to the appropriate register (depending on the mode of the device). This iterative process continues through all 64 bits until they are written. For the DS1651 Lock, after 64 bits are written, a compare operation is performed. For the DS1652, after 64 bits are written, the key can be returned to its operation mode for use.

OPERATION, LOCK AND KEY

The DS1651 Lock and DS1652 Key provide a security code matching system which can be used as the code control logic of any security system. The unique DS1651 Lock provides the system designer with the option of pre-programming a lock or series of locks with a known set of 64–bit codes that can only be changed by having physical access to the lock. If known codes are not required, the DS1651 can generate its own 64–bit code randomly. If the random number generator of the DS1651 Lock is used, not even the person programming the lock knows the 64–bit code.

The DS1652 Key is programmed from the DS1651 Lock and can be repeatedly reprogrammed to accept new codes. This feature not only prolongs the usable life of the key, but also provides the user the ability to recycle keys from one lock to be programmed for use with another lock. Materials invested in building keys are never obsoleted because keys can always be reprogrammed.

A significant contribution to maintaining the security of the DS1651 Lock is limiting the manner by which a lock can program a key with the code to open the lock. The only way in which a DS1652 Key will accept a code is to connect its input pin directly to the data input/output pin of a DS1651 Lock. Therefore the only method of transferral is by physically connecting the device holding the DS1652 Key with the device holding the DS1651 Lock. A quick and efficient method of implementing this interface is illustrated in Figure 1.

By designing the system key with three external leads, one tied to LEARN, one tied to ground, and one tied to the data I/O pin, the system key can accept a new code from a system lock only through these three connections. Once placed in a system lock, the DS1651 Lock could be enabled to transmit its code memory to the key. Because of the physical connection required for the

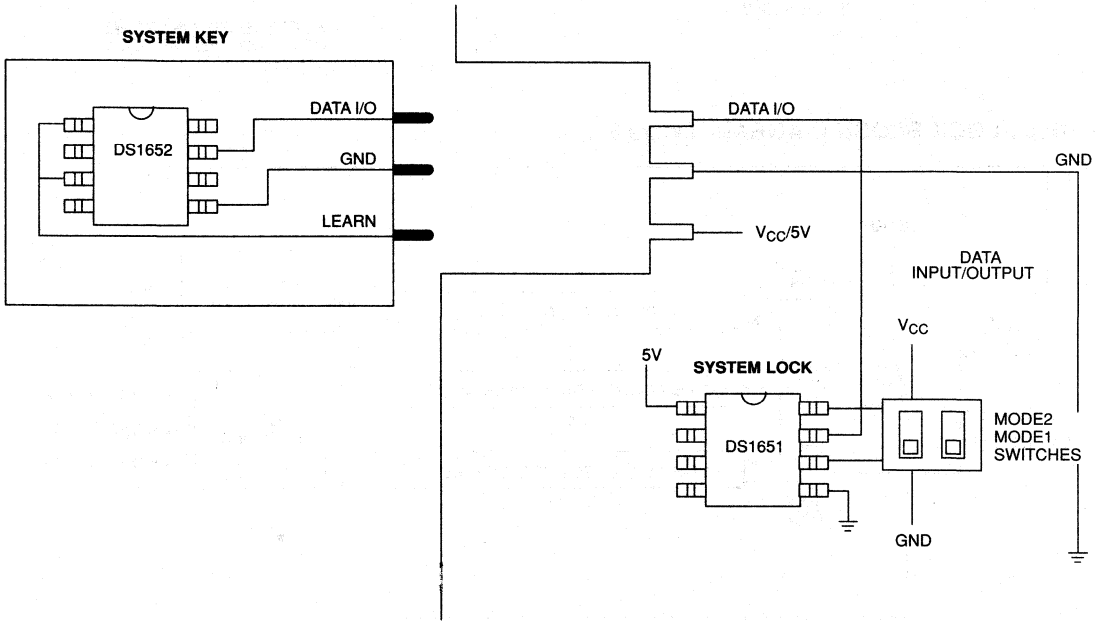
code data transfer, the lock and key combination is kept secure.

The method chosen to duplicate the key does not have to be the suggested method. This method is suggested as a way that

1. limits who can program keys
2. limits who can generate codes for the lock
3. limits who can, by generating a new code, invalidate the existing programmed keys.

As many keys as needed can be programmed. As required for security purposes or in case of the loss of a key, a new code can be generated and redistributed to the remaining keys. This enables the security system to continually reuse keys and obsolete the codes in any keys that become lost or stolen.

INTERIOR OF LOCK SECURED AREA Figure 1

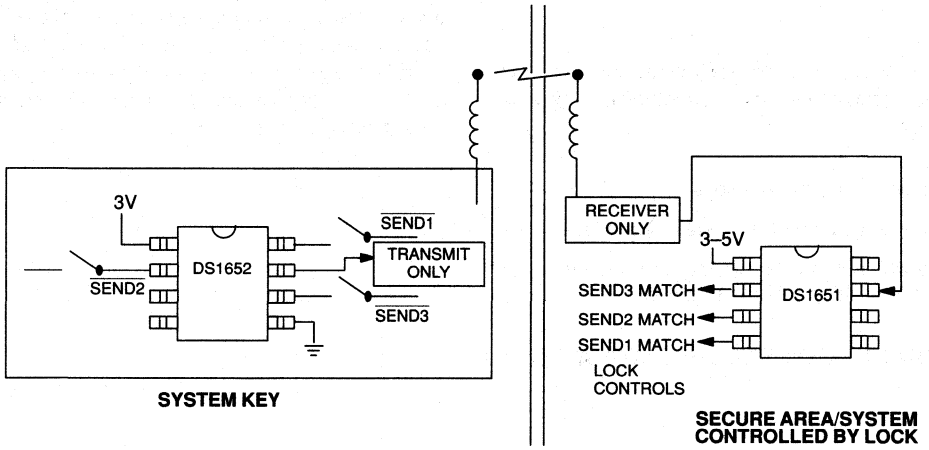


TYPICAL APPLICATION

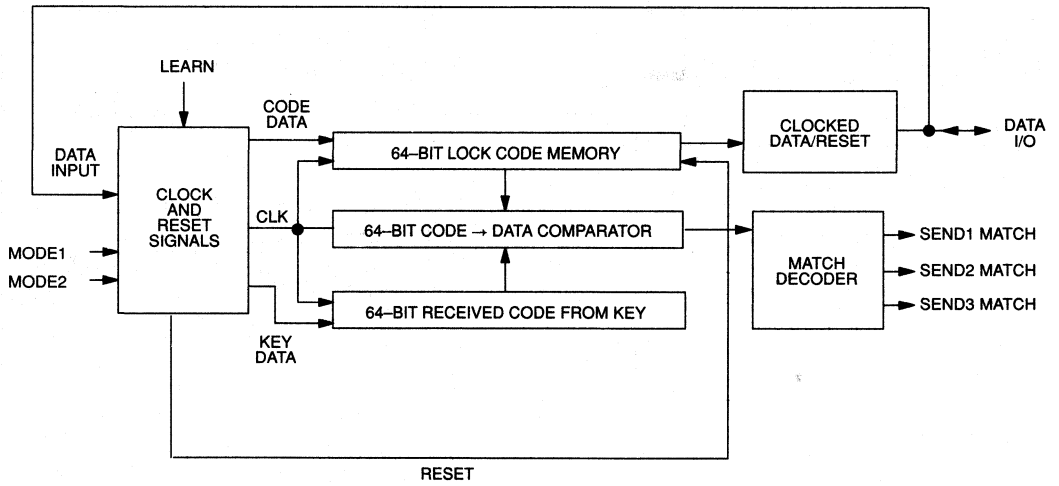
One of the easiest ways to implement the lock and key system is to use an RF transmitter to link the data input/output pin of the DS1652 Key to the DS1651's input pin.

For implementation, any transmission media capable of transmitting and receiving signals at the resolution required of the DS1651 and DS1652's serial pulse protocol can be used to link the key to a lock.

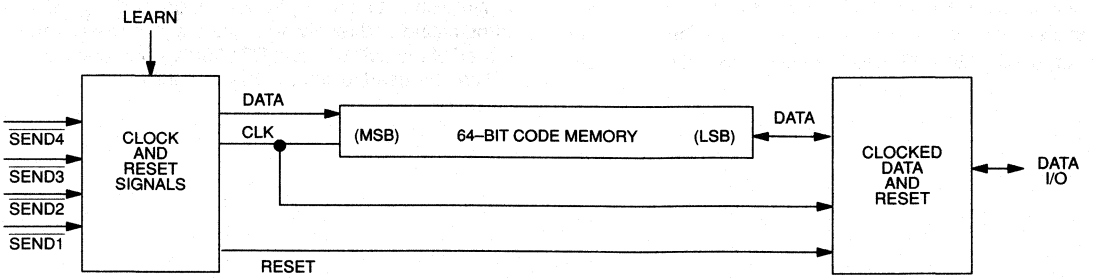
TYPICAL APPLICATION Figure 2



DS1651 LOCK BLOCK DIAGRAM Figure 3



DS1652 KEY BLOCK DIAGRAM Figure 4



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to –V	-0.5V to +7.0V
Operating Temperature	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 15 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-25°C to +85°C) DS1651 and DS1652

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	2.7	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.0	-	V_{CC}+0.3	V	1, 5
Logic 0 Input	V_{IL}	-0.3	-	+0.8	V	1, 5

DC ELECTRICAL CHARACTERISTICS

(-25°C to +85°C) DS1651

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current, Operation Mode	I_{CC1}		3	4	mA	2
Supply Current, Learn Mode	I_{CC2}		3	4	mA	2
Supply Current, Idle State	I_{CC3}		75	100	nA	2
V_{CC} Voltage, Learn Mode	V_{CCL}	4.5	5.0	5.5	V	1
Output High, Voltage	V_{OH}	2.4			V	1, 6
Output High, Current	I_{OH}	–1			mA	
Output Low, Voltage	V_{OL}	0.4			V	1, 6
Output Low, Current	I_{OL}	4			mA	
I/O Leakage Current	I_{IO}	-1		+1	µA	4

DC ELECTRICAL CHARACTERISTICS

(-25°C to +85°C) DS1652

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current, Send Mode	I_{CC1}		3	4	mA	2
Supply Current, Learn Mode	I_{CC2}		3	4	mA	2
Supply Current, Idle State	I_{CC3}	50	75	100	nA	2
V_{CC} Voltage, Learn Mode	V_{CCL}	4.5	5.0	5.5	V	1
Input Leakage (Data I/O pin)	I_{L1}	-1		+1	µA	3
Output High, Voltage	V_{OH}	2.4			V	1, 6
Output High, Current	I_{OH}	4			mA	
Output Low, Voltage	V_{OL}	0.4			V	1, 6
Output Low, Current	I_{OL}	1			mA	

AC ELECTRICAL CHARACTERISTICS DS1651 LOCK AND DS1652 KEY DATA TRANSMISSION PARAMETERS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Active	t_R	540	720	900	µs	
Logic 1 Active	t_1	90	120	150	µs	
Logic 0 Active	t_0	15	20	25	µs	
SEND1 MATCH, SEND2 MATCH, and SEND3 MATCH	t_M	400	500	600	ms	
Data Sample Window	t_{DS}	1.5	2.0	2.5	ms	
Active Signal Pulse Width, Data I/O	t_{PW}	10		1080	µs	
Active Signal Pulse Width $\overline{\text{SEND1}}$ and $\overline{\text{SEND2}}$	t_S	100			ms	
Delay Between Last Mode Pin Transition to Operation Mode Change	t_T		10		ms	

CAPACITANCE

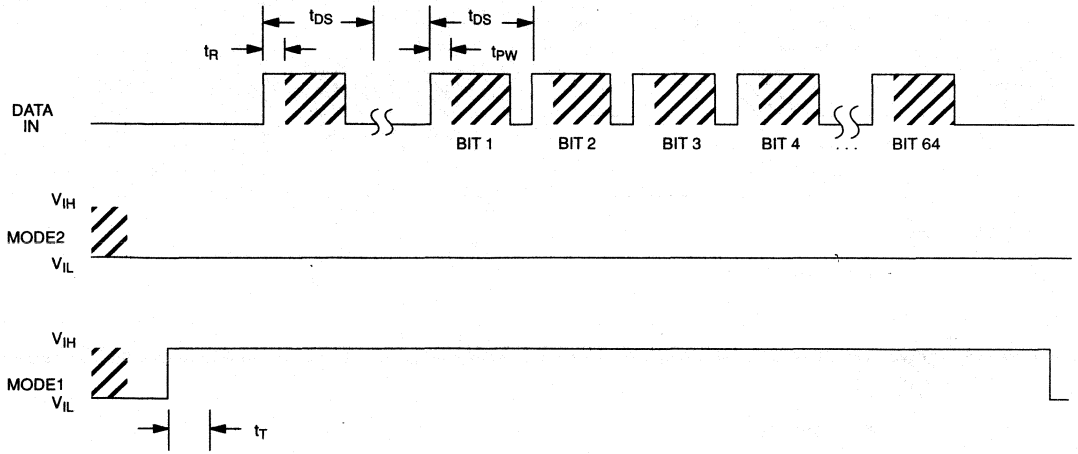
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

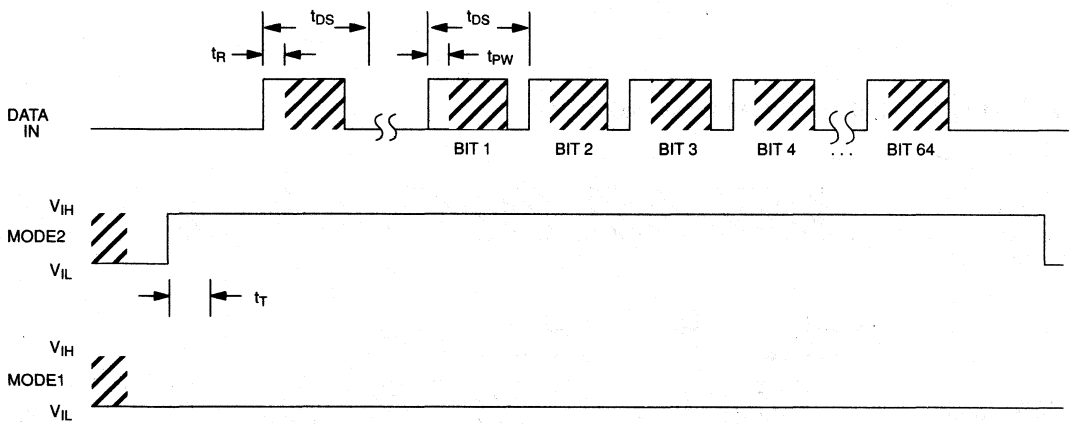
NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. Input leakage applies to DS1652 data I/O pin in input mode only.
4. Input/output leakage applies to the DS1651 data input/output pin.
5. The DS1652 $\overline{\text{SEND1}}$, $\overline{\text{SEND2}}$, $\overline{\text{SEND3}}$, and $\overline{\text{SEND4}}$ inputs are internally pulled up with 25KΩ resistors and require input levels of <0.5V for logic 0, and >V_{CC}–0.5V for logic 1. The DS1652 learn pin has an internal 10KΩ pulldown.
6. Valid for V_{CC}=5.0V ± 10%.

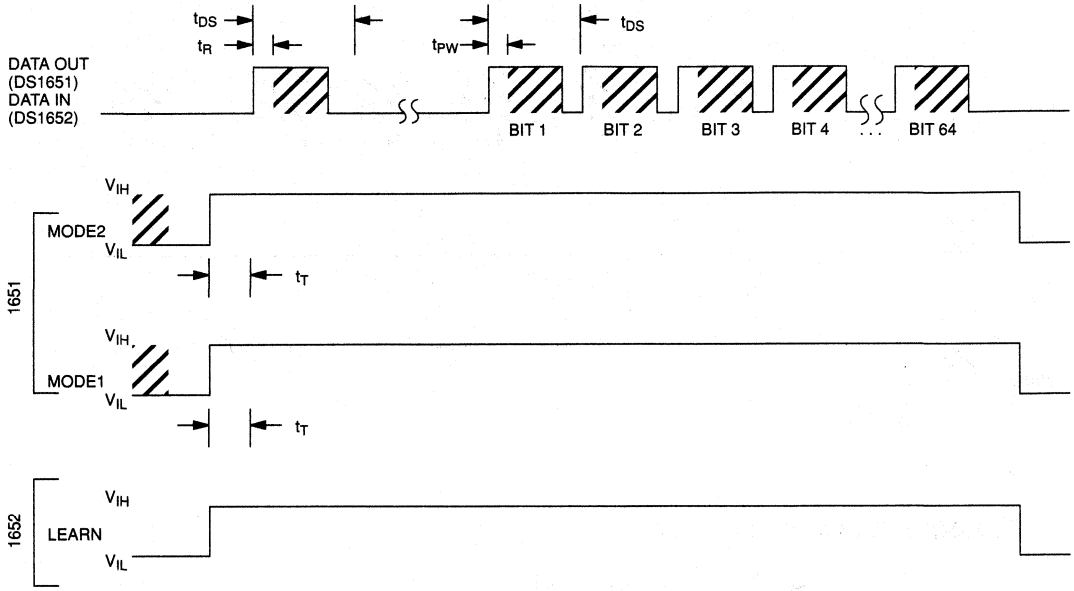
LEARN MODE DS1651 LOCK; USER PROGRAMMING



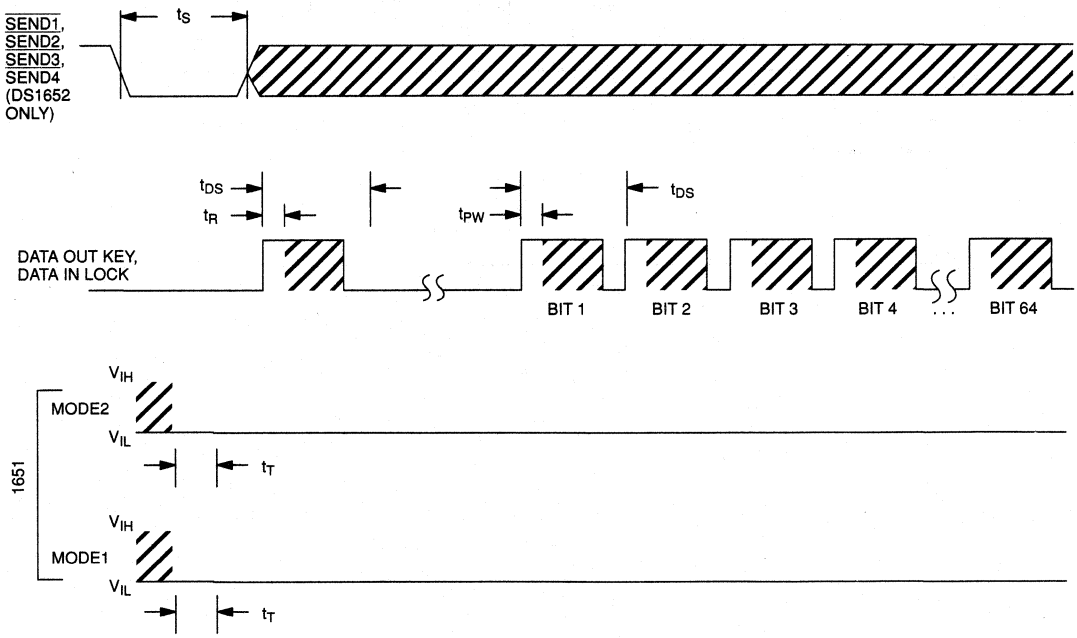
DS1652 LOCK; DUPLICATION MODE



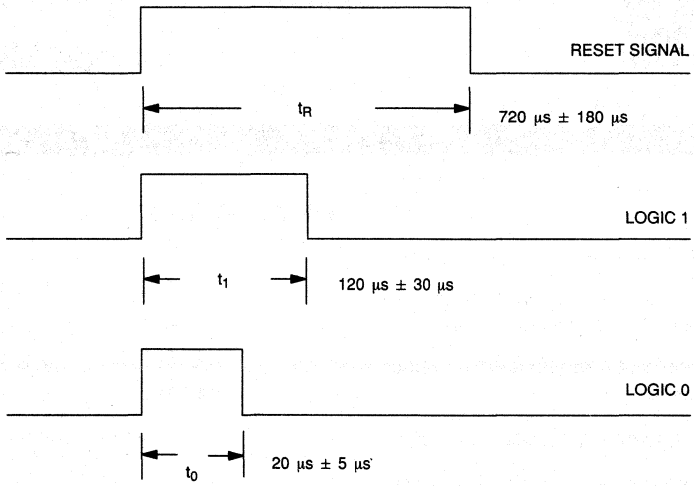
LEARN MODE DS1652 KEY; LEARN MODE DS1651 LOCK, INTERNAL PROGRAMMING



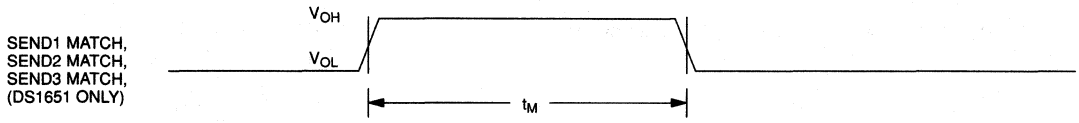
OPERATION DS1651 LOCK AND DS1652 KEY



LOGIC TIMING DIAGRAMS



DS1651 LOCK, MATCH SIGNALS



When the DS1651 Lock's code comparator determines that code data it has received matches one of its code data memories, the appropriate match signal is driven active for the above diagram.

INPUT TRIGGERED	64 CODE TRANSMITTED AS:								
$\overline{SEND1}$	b_0	b_1	b_2	b_3	b_4	. . .	b_{61}	b_{62}	b_{63}
$\overline{SEND2}$	$\overline{b_0}$	$\overline{b_1}$	$\overline{b_2}$	$\overline{b_3}$	$\overline{b_4}$	. . .	$\overline{b_{61}}$	$\overline{b_{62}}$	$\overline{b_{63}}$
$\overline{SEND3}$	b_0	$\overline{b_1}$	b_2	$\overline{b_3}$	b_4	. . .	$\overline{b_{61}}$	b_{62}	$\overline{b_{63}}$
$\overline{SEND4}$	$\overline{b_0}$	b_1	$\overline{b_2}$	b_3	$\overline{b_4}$	. . .	b_{61}	$\overline{b_{62}}$	b_{63}

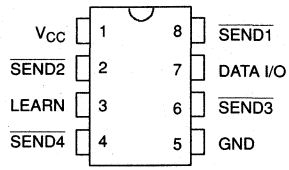
DALLAS SEMICONDUCTOR

DS1652B
Code Memory Key

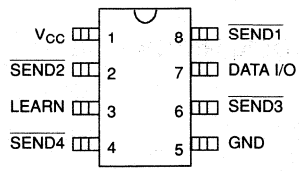
FEATURES

- The key forms the basis of a secure access system
- The DS1652B is compatible with a variety of RF, serial, ultrasound, and optical transmission media
- The user–programmable 64–bit code prevents unauthorized copying of keys
- Each key capable of generating 4–code conditions
- Keys are programmed from an externa! device only under controlled user access/secure conditions
- Low–cost, economical
- Key codes can be changed as many times as necessary
- 3V operation, 5V for programming
- Operating range of –25°C to +85°C
- All stored 64–bit codes in the key are nonvolatile and retain the security code in the absence of power
- Applications include building entry, garage door openers, automobile entry and ignition, and local and remote identification

PIN ASSIGNMENT



8-Pin DIP (300 Mil)
See Mech. Drawing
Pg. 480



8-Pin SOIC (200 Mil)
See Mech. Drawing
Pg. 483

PIN DESCRIPTION

V_{CC}	–	+3V to +5V Input
GND	–	Ground
DATA I/O	–	Serial Data Input/Output
$\overline{SEND1}$	–	Send Input 1
$\overline{SEND2}$	–	Send Input 2
$\overline{SEND3}$	–	Send Input 3
$\overline{SEND4}$	–	Send Input 4
LEARN	–	Learn Input

DESCRIPTION

The DS1652B Code Memory Key operates as part of a system to limit access of any secure system or area to keyholders. The DS1652B key contains a 64–bit memory which acts as the security code, controlling access. Once set, the code is nonvolatile.

To gain access to a locked system, the key's code must be transmitted to the lock via some user transmission media such as RF, optical, IR, ultrasound, or another serial medium. Upon receiving a transmission of a 64–bit key code, a lock system must compare the requesting key's 64–bit code to the lock system's programmed code. If the key code matches the lock system code, the lock system must generate a match signal, which can be used to allow access to the secure system.

OPERATION DS1652B KEY

The operation of the DS1652B key is shown in Figure 1. The key is programmed with code from an external source with the key in Learn mode.

For the DS1652B key to be programmed, the LEARN pin must be driven active high, with V_{CC} on the DS1652B at least 4.5V. The DS1652B key's data input/output pin must be physically connected to the external programming device for the DS1652B key to successfully accept a code. Once connected and in the Learn mode, the DS1652B key is ready to accept its 64–bit code. The DS1652B key will recognize the 1600 µs wide active high reset signal, and will use the rising edge of each subsequent signal to determine the contents of 64 consecutive 2 ms wide data windows as logic 1 or logic 0. The contents of the 64 consecutive windows, transmitted by the external programming device, become latched into the nonvolatile 64–bit code memory of the DS1652B key. The key will perform no other operations until the LEARN pin becomes inactive, returning the DS1652B to its operation mode. The DS1652B key will transmit a reset signal and its code memory out of its data input/output pin a maximum of ten times as long as the $\overline{SENDX}$ input is asserted. The DS1652B key will transmit a version of the code that is specifically tailored to the $\overline{SENDX}$ input being triggered. (See Logic Timing Diagrams.)

SERIAL PULSE PROTOCOL

The DS1652B transmits and receives data serially, according to the protocol listed in the timing diagram.

The transmission and reception of data begins with the rising edge of the 1600 µs reset signal. The DS1652B then begins looking for data in 2 ms windows. Each data window begins with the rising edge of a pulse. The duration of the pulse determines whether a logical one or logical zero is present in that window (logical one pulse duration is twice as long as logical zero pulse duration).

For 128 ms, the DS1652B will time the duration of the active pulse in each window. Once the pulse is interpreted as a 1 or a 0, the data bit is written to the 64–bit code memory. This iterative process continues through all 64 bits until they are written. For the DS1652B, after 64 bits are written, the key may be returned to its operation mode for use.

OPERATION, LOCK AND KEY

The DS1652B key provides a security code matching system which can be used as the code control logic of any security system.

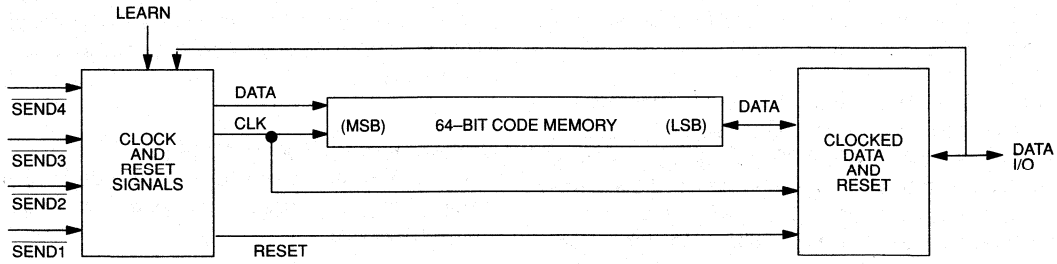
The DS1652B key is programmed from an external programming device and can be repeatedly reprogrammed to accept new codes. This feature not only prolongs the usable life of the key, but also provides the user the ability to recycle keys from one lock to be programmed for use with another lock. Materials invested in building keys are never obsoleted because keys may always be reprogrammed.

A significant contribution to maintaining the security of a DS1652B key based system is limiting the manner by which a key may be programmed with the code to open the lock. The only way in which a DS1652B key will accept code is to connect its data input/output pin directly to the external programming device. Therefore the only method of transferral is by physically connecting the device holding the DS1652B key with the device holding the programmer. A quick and efficient method of implementing this interface is illustrated in Figure 2.

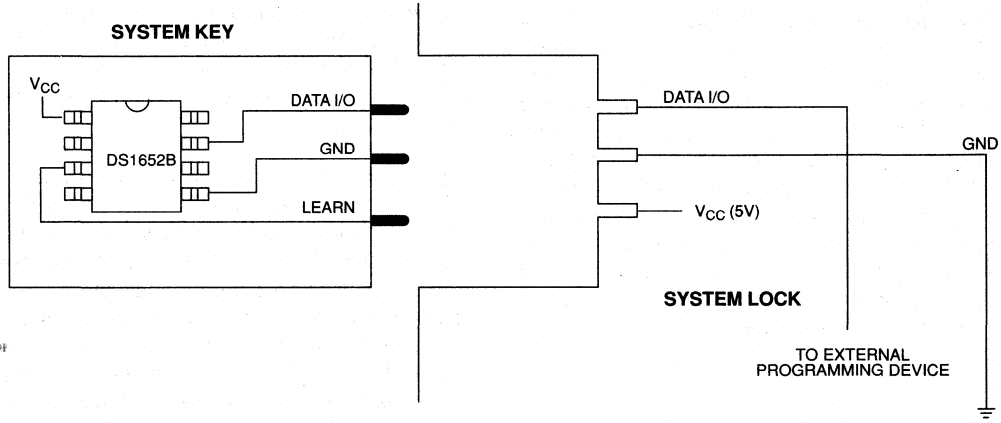
By designing the system key with three external leads, one tied to V_{CC} (5V), one tied to ground, and one tied to the input pin, the system key can accept a new code from a system lock only through these three connections.

As many keys as needed can be programmed. As required for security purposes, or in case of the loss of a key, a new code can be generated and redistributed to the remaining keys. This enables the security system to continually reuse keys and obsolete the codes in any keys that become lost or stolen.

DS1652B KEY BLOCK DIAGRAM Figure 1



INTERIOR OF LOCK SECURED AREA Figure 2

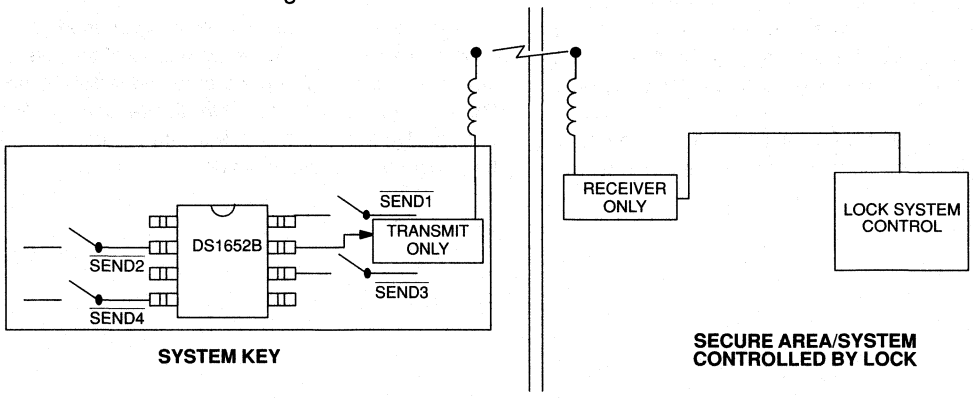


TYPICAL APPLICATION

One of the easiest ways to implement the lock and key system is to use an RF transmitter to link the data input/output pin of the DS1652B key to the system lock.

For implementation, any transmission media capable of transmitting and receiving signals at the resolution required of the DS1652B's serial pulse protocol can be used to link the key to the user's lock system.

TYPICAL APPLICATION Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-25°C to +85°C) DS1652B

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	2.7	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.0	–	V_{CC}+0.3	V	1, 4, 5, 6
Logic 0 Input	V_{IL}	–0.3	–	+0.8	V	1, 5, 6

DC ELECTRICAL CHARACTERISTICS

(-25°C to +85°C) DS1652B

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current, Send Mode	I_{CC1}		3	4	mA	2
Supply Current, Learn Mode	I_{CC2}		3	4	mA	2
Supply Current, Idle State	I_{CC3}		75	100	nA	2
V_{CC} Voltage, Learn Mode	V_L	4.5	5	5.5	V	1, 5
Input Leakage (Data Input)	I_{L1}	–1		+1	µA	3
Output High, Voltage	V_{OH}	2.4			V	1
Output High, Current	I_{OH}	–1			mA	
Output Low, Voltage	V_{OL}	0.4			V	1
Output Low, Current	I_{OL}	4			mA	

AC ELECTRICAL CHARACTERISTICS DS1652B KEY DATA TRANSMISSION PARAMETERS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Active	t_R	1200	1600	2000	µs	
Logic 1 Active	t_1	600	800	1000	µs	
Logic 0 Active	t_0	300	400	500	µs	
Data Sample Window	t_{DS}	1.5	2.0	2.5	ms	
Active Signal Pulse Width, Data I/O	t_{PW}	300		2000	µs	
Active Signal Pulse Width $\overline{SEND1}$, $\overline{SEND2}$, $\overline{SEND3}$, and $\overline{SEND4}$	t_S	10			ms	
Delay Between LEARN Pin Transition and Operation Mode Change	t_T			10	ms	
Delay Between Minimum $\overline{SENDX}$ Assertion and Data Out Transmitted	t_{SD}			100	µs	
Number of Words Transmitted for 1 $\overline{SENDX}$ Input Recognized		10				

CAPACITANCE

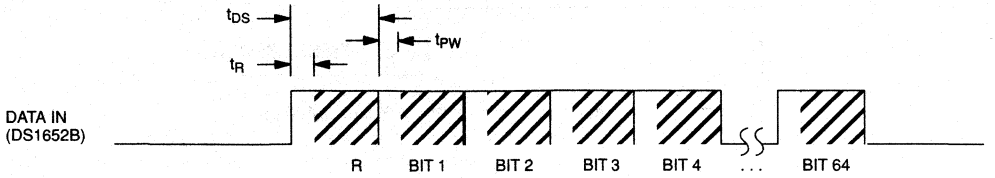
(t_A = 25°C)

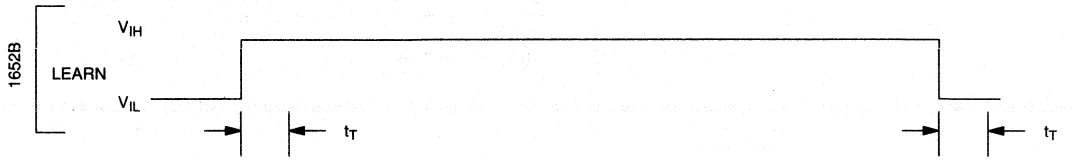
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

NOTES:

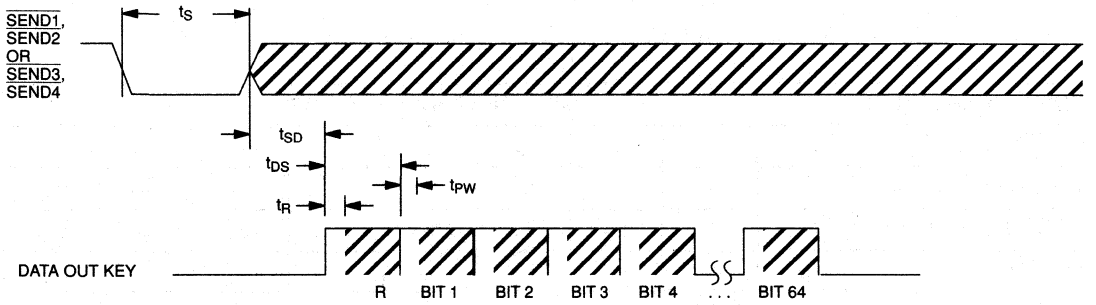
1. All voltages are referenced to ground.
2. Measured with outputs open.
3. Input leakage applies to DS1652B data input only.
4. Absolute maximum rating is 7.0V on any pin.
5. The DS1652B LEARN pin is internally pulled down with approximately a 10KΩ resistor.
6. The DS1652B $\overline{SEND1}$, $\overline{SEND2}$, $\overline{SEND3}$, and $\overline{SEND4}$ inputs are internally pulled up with approximately 25KΩ resistors.

LEARN MODE DS1652B KEY

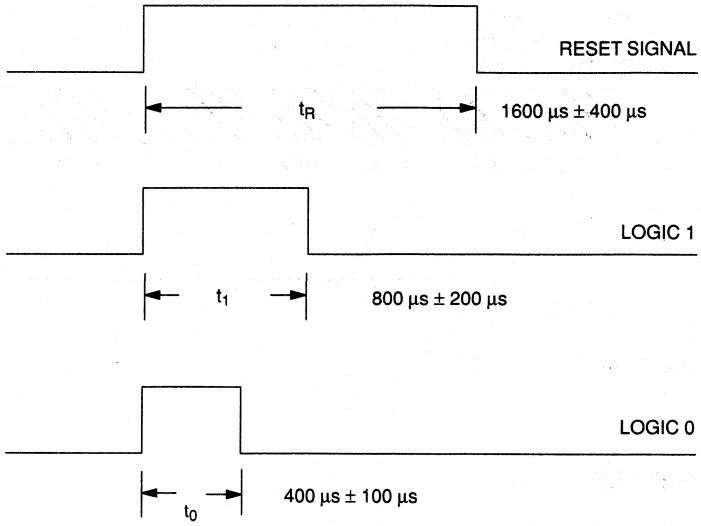




OPERATION DS1652B KEY



LOGIC TIMING DIAGRAMS



INPUT TRIGGERED	64 CODE TRANSMITTED AS:								
$\overline{\text{SEND1}}$ (DATA)*	b_0	b_1	b_2	b_3	b_4	. . .	b_{61}	b_{62}	b_{63}
$\overline{\text{SEND2}}$ ($\overline{\text{DATA}}$)	$\overline{b_0}$	$\overline{b_1}$	$\overline{b_2}$	$\overline{b_3}$	$\overline{b_4}$	. . .	$\overline{b_{61}}$	$\overline{b_{62}}$	$\overline{b_{63}}$
$\overline{\text{SEND3}}$ ($\overline{\text{ODD}}$)	b_0	$\overline{b_1}$	b_2	$\overline{b_3}$	b_4	. . .	$\overline{b_{61}}$	b_{62}	$\overline{b_{63}}$
$\overline{\text{SEND4}}$ ($\overline{\text{EVEN}}$)	$\overline{b_0}$	b_1	$\overline{b_2}$	b_3	$\overline{b_4}$	. . .	b_{61}	$\overline{b_{62}}$	b_{63}

*The bit pattern transmitted by the $\overline{\text{SEND1}}$ trigger it the unaltered contents of the DS1652B code memory. $\overline{\text{SEND2}}$, $\overline{\text{SEND3}}$, and $\overline{\text{SEND4}}$ transmit modified versions of this code a listed above.

DALLAS SEMICONDUCTOR

DS1653
4-Code Lock
DS1652
Key Match Memory System

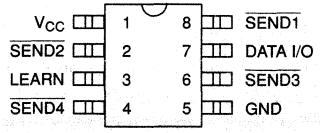
FEATURES

- The two–chip lock and key system form the basis of a secure access system
- The match memory system is compatible with a variety of RF, serial, ultrasound, and optical transmission media
- The user–programmable 64–bit code or internally generated random 64–bit code prevents unauthorized copying of keys
- Each key and lock system is capable of generating and recognizing 4-code match conditions
- Keys are programmed from lock codes only under controlled user access/secure conditions
- Low–cost, economical
- Lock codes can be changed as many times as necessary
- 3V operation, 5V for programming
- Operating range of -25°C to +85°C
- All stored 64–bit codes in the lock and key are nonvolatile and retain the security code in the absence of power
- Applications include building entry, garage door openers, automobile entry and ignition, and local and remote identification

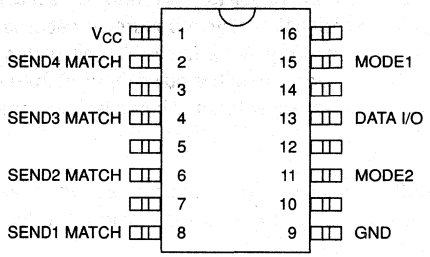
DESCRIPTION

The DS1653 Lock and DS1652 Key operate in combination to limit access of any secure system or area to keyholders. Both the DS1653 Lock and DS1652 Key contain a 64–bit memory which acts as the security code, controlling access. The code memory within the DS1653 Lock can be user programmed with a known 64–bit code, or the DS1653 can generate a 64–bit code from an internal random number generator. Once set, the code is nonvolatile and can then be transferred to one or more DS1652 Key(s) under secure conditions.

PIN ASSIGNMENT



DS1652 8-Pin DIP (300 Mil) and
DS1652S 8-Pin SOIC (200 Mil)
See Mech. Drawings
Pgs. 480 & 483



DS1653 16-Pin DIP (300 Mil) and
DS1653S 16-Pin SOIC (300 Mil)
See Mech. Drawings
Pgs. 480 & 484

DS1652 PIN DESCRIPTION

GND	-	Ground
DATA I/O	-	Serial Data Input/Output
$\overline{SEND1}$	-	Send Input 1
$\overline{SEND2}$	-	Send Input 2
$\overline{SEND3}$	-	Send Input 3
$\overline{SEND4}$	-	Send Input 4
LEARN	-	Learn Input
V_{CC}	-	+3V to +5V Input

DS1653 PIN DESCRIPTION

MODE2	-	Function Control Pin
MODE1	-	Function Control Pin
V_{CC}	-	+3V to +5V Input
GND	-	Ground
DATA I/O	-	Serial Data Input/Output
SEND1 MATCH	-	Code Match Signal for SEND1
SEND2 MATCH	-	Code Match Signal for SEND2
SEND3 MATCH	-	Code Match Signal for SEND3
SEND4 MATCH	-	Code Match Signal for SEND4

To gain access to the lock, the key's code must be transmitted to the lock via some user transmission media such as RF, optical, IR, ultrasound, or another serial medium. Upon receiving a transmission of a 64–bit key code, a DS1653 Lock will compare the requesting key's 64–bit code to the lock's programmed 64–bit code. If the key code matches the lock code, the lock generates a match signal, which can be used to allow access to the secure system.

OPERATION DS1653 LOCK

The main functional components of both the DS1653 and DS1652 are shown in Figures 3 and 4. The diagrams show that the internal functions of the lock and key are similar. From Figure 3, the primary components of the lock are its 64–bit–wide registers. The 64–bit code memories are the physical "lock" and contain the pattern against which all keys are measured for access. The 64–bit data memory records the 64–bit pattern transmitted by a potential key. The pulse input interpreter and reset generator accepts serial input data from the input pin.

The DS1653 Lock has four functional modes, which are controlled by the lock's mode control pins. The four modes are defined as follows:

MODE2	MODE1	FUNCTIONAL MODE
0	0	Operation Mode: Receiving codes from key(s).
0	1	Learn Mode: Program with user–provided 64–bit codes.
1	0	Duplicate Mode: Transmit 64-bit code memory contents.
1	1	Learn Mode: Program with internally generated random 64 bits.

The Learn and Duplicate modes can only be entered from Operation mode. The DS1653 samples the level of MODE1 and MODE2 10 ms after a transition on either pin. This sample is used to tell the DS1653 in which mode it should be operating.

In the Learn modes, the DS1653 Lock's code memory can be either programmed directly by the user or programmed using a random set of 1's and 0's created by the DS1653's random number generator. A user must have physical access to the DS1653 to place it in Learn mode. To place the DS1653 Lock in Learn mode, the DS1653's V_{CC} input must be at 4.5V minimum with MODE1 or both MODE1 and MODE2 pins driven high, telling the DS1653 to enable the contents of its code memory to be rewritten. If MODE1 is high, then the DS1653 enables its code memory to be rewritten using a user–defined, 64–bit code, which it expects to see on its data I/O pin. At the end of sending the 64–bit code to the DS1653, the mode pins must both be driven low, returning the lock to operation mode, before entering any other mode. (See timing diagram "Learn Modes DS1653 Lock.") If MODE2 and MODE1 are high, then the DS1653 Lock uses its internal random number generator to create a 64–bit pattern of 1's and 0's and loads it into the code data memory, from LSB to MSB. When all 64 bits have been written, the DS1653 has a new code memory that can be programmed into DS1652 Keys. After this operation is completed, the mode pins must both be driven low to return the DS1653 to operation mode before entering any other mode.

The DS1653 will not reprogram its 64–bit code memory using its internal random number generator until another transition from 0 to 1 is seen on both its MODE2 and MODE1 pins.

For the DS1653 Lock to transfer its code memory into a DS1652 Key, the DS1653 Lock must be in duplication mode. To enter the duplication mode, the MODE2 pin must be driven high. The transition from 0 to 1 on the MODE2 pin, and its maintenance at 1 causes the DS1653 Lock to transmit a reset signal followed by its 64–bit code memory through its data input/output pin. The lock will transmit the code only once. If another transmission is required, the mode pin must be driven to zero before being returned to 1 to send another 64–bit code copy. The data input/output pin of the DS1653 Lock must be physically connected to the data input pin of the target DS1652 Key in order to transfer a code from the lock to a key to be used with that lock. The target key must also be in Learn mode (see operation DS1652 Key) for the key to accept as code the information transmitted by the lock. With these timing and hardware conditions satisfied DS1652 Key programming can be performed quickly (<1 s) and easily with only one serial connection between the DS1653 and DS1652.

The DS1653 Lock is in its Operation mode with its mode pins inactive. The receipt of a signal on the input/output pin which is active high for at least 720 µs is treated as a reset signal from a key about to transmit its code. The interpreted pattern of 1's and 0's sampled in the 2 ms wide windows is written into the data memory for com-

parison to the lock's code memories. If the comparison shows a match with one of the memories, then the DS1653 drives the appropriate SENDX MATCH signal. If the code does not match, the DS1653 performs no operations, but waits for the next reset signal.

OPERATION DS1652 KEY

The operation of the DS1652 Key is similar to that of the DS1653 (Figure 2). The key is programmed with code generated by the DS1653 Lock with the lock in duplication mode and the key in Learn mode.

For the DS1652 Key to be programmed, the LEARN pin must be driven active high. The DS1652 Key's data input pin must be physically connected to the DS1653 Lock's data input/output pin for the DS1652 Key to successfully accept a code from a DS1653 Lock. Once connected and in the Learn mode, the DS1652 Key is ready to accept its 64–bit code. The DS1652 Key will recognize the 720 µs wide active high reset signal, and will use the rising edge of each subsequent signal to determine the contents of 64 consecutive 2 ms wide data windows as logic 1 or logic 0. The contents of the 64 consecutive windows, transmitted by the lock, become latched into the nonvolatile 64–bit code memory of the DS1652 Key. The key will perform no other operations until the LEARN pin becomes inactive, returning the DS1652 to its operation mode. The DS1652 Key will transmit a reset signal and its code memory out of its data output pin a maximum of three times as long as the $\overline{\text{SENDX}}$ input is asserted. The DS1652 Key will transmit a version of the code that is specifically tailored to the $\overline{\text{SENDX}}$ input being triggered. (See diagram "DS1693 Match Signals".)

SERIAL PULSE PROTOCOL

The DS1653 and DS1652 transmit and receive data serially, according to the protocol listed in the timing diagrams.

The transmission and reception of data begins with the rising edge of the 720 µs reset signal. The DS1653 and DS1652 then begin looking for data in 2 ms windows. Each data window begins with the rising edge of a pulse. The duration of the pulse determines whether a logical one or logical zero is present in that window (logical one pulse duration is six times as long as logical zero pulse duration).

For 128 ms, the DS1653 or DS1652 will time the duration of the active pulse in each window. Once the pulse is interpreted as a 1 or a 0, the data bit is written to the appropriate register (depending on the mode of the device). This iterative process continues through all 64 bits until they are written. For the DS1653 Lock, after 64 bits are written a compare operation is performed. For the DS1652, after 64 bits are written, the key can be returned to its operation mode for use.

OPERATION, LOCK AND KEY

The DS1653 Lock and DS1652 Key provide a security code matching system which can be used as the code control logic of any security system. The unique DS1653 Lock provides the system designer with the option of pre-programming a lock or series of locks with a known set of 64–bit codes that can only be changed by having physical access to the lock. If known codes are not required, the DS1653 can generate its own 64–bit code randomly. If the random number generator of the DS1653 Lock is used, not even the person programming the lock knows the 64–bit code.

The DS1652 Key is programmed from the DS1653 Lock and can be repeatedly reprogrammed to accept new codes. This feature not only prolongs the usable life of the key, but also provides the user the ability to recycle keys from one lock to be programmed for use with another lock. Materials invested in building keys are never obsoleted because keys can always be reprogrammed.

A significant contribution to maintaining the security of the DS1653 Lock is limiting the manner by which a lock can program a key with the code to open the lock. The only way in which a DS1652 Key will accept code is to connect its input pin directly to the data input/output pin of a DS1653 Lock. Therefore the only method of transferral is by physically connecting the device holding the DS1652 Key with the device holding the DS1653 Lock. A quick and efficient method of implementing this interface is illustrated in Figure 1.

By designing the system key with three external leads, one tied to LEARN, one tied to ground, and one tied to the data I/O pin, the system key can accept a new code from a system lock only through these three connections. Once placed in a system lock, the DS1653 Lock

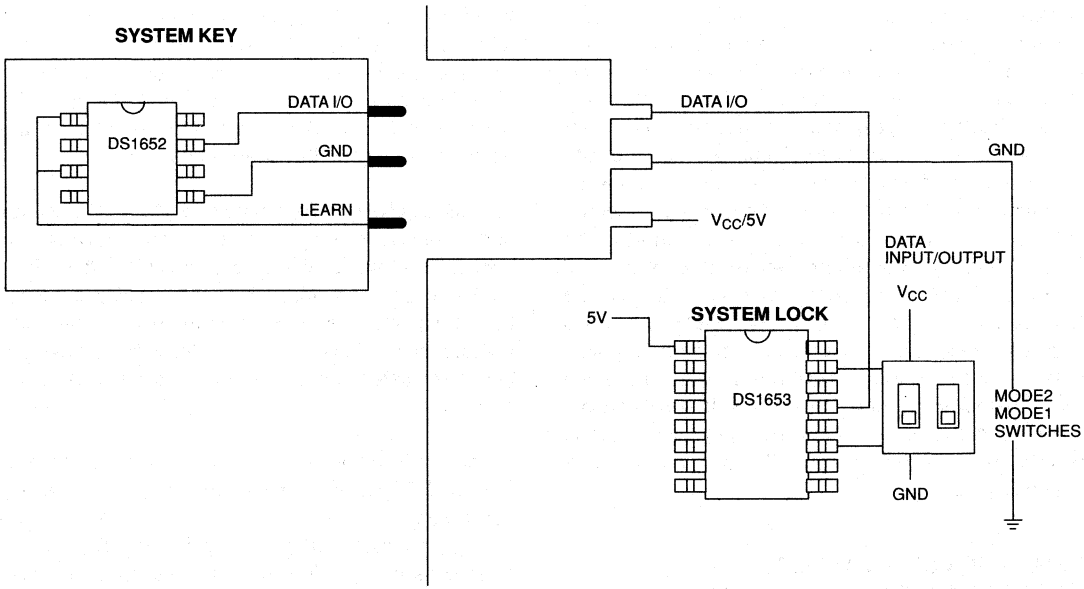
could be enabled to transmit its code memory to the key. Because of the physical connection required for the code data transfer, the lock and key combination is kept secure.

The method chosen to duplicate the key does not have to be the suggested method. This method is suggested as a way that

1. limits who can program keys
2. limits who can generate codes for the lock
3. limits who can, by generating a new code, invalidate the existing programmed keys.

As many keys as needed can be programmed. As required for security purposes or in case of the loss of a key, a new code can be generated and redistributed to the remaining keys. This enables the security system to continually reuse keys and obsolete the codes in any keys that become lost or stolen.

INTERIOR OF LOCK SECURED AREA; PROGRAMMING MODE Figure 1

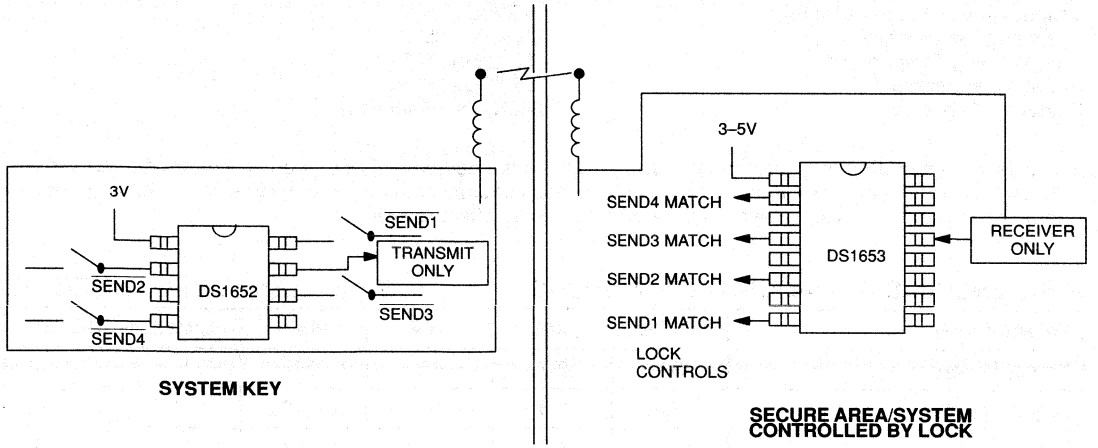


TYPICAL APPLICATION

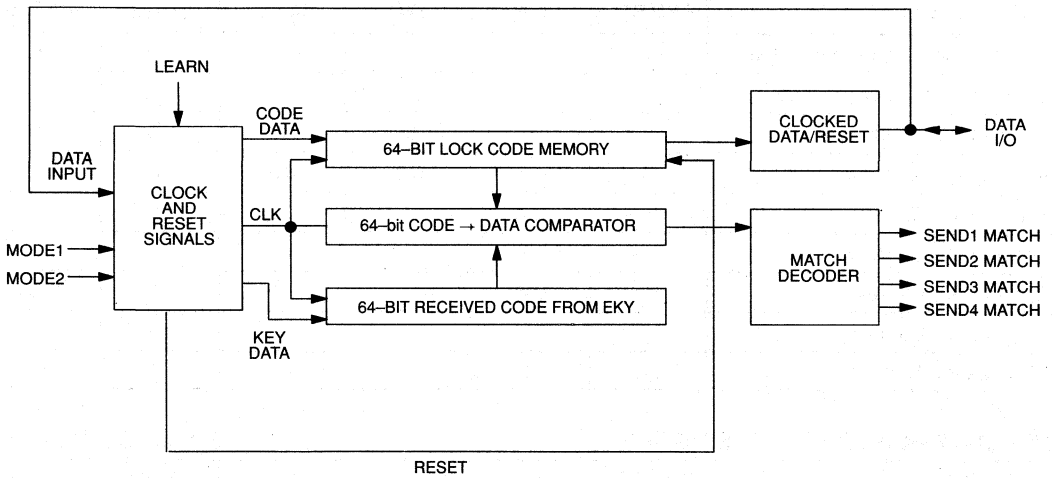
One of the easiest ways to implement the lock and key system is to use an RF transmitter to link the data input/output pin of the DS1652 Key to the DS1653's input pin.

For implementation, any transmission media capable of transmitting and receiving signals at the resolution required of the DS1653 and DS1652's serial pulse protocol can be used to link the key to a lock.

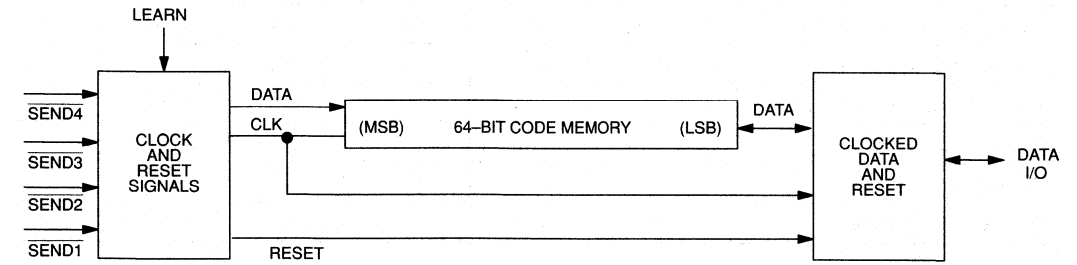
TYPICAL APPLICATION Figure 2



DS1653 LOCK BLOCK DIAGRAM Figure 3



DS1652 KEY BLOCK DIAGRAM Figure 4



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to -V	-0.5V to +7.0V
Operating Temperature	-25°C to +85°C
Programming Temperature	-10°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 15 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-25°C to + 85°C) DS1653 and DS1652

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	2.7	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.0	-	V_{CC}+0.3	V	1, 5, 6
Logic 0 Input	V_{IL}	-0.3	-	+0.8	V	1, 5, 6

DC ELECTRICAL CHARACTERISTICS

(-25°C to 85°C) DS1653

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current, Operation Mode	I_{CC1}		3	4	mA	2
Supply Current, Learn Mode	I_{CC2}		3	4	mA	2
Supply Current, Idle State	I_{CC3}		75	100	nA	2
V_{CC} Voltage, Learn Mode	V_{CCL}	4.5	5.0	5.5	V	1, 5
Output High, Voltage	V_{OH}	2.4			V	1, 7
Output High, Current	I_{OH}	–1			mA	
Output Low, Voltage	V_{OL}	0.4			V	1, 7
Output Low, Current	I_{OL}	4			mA	
I/O Leakage Current	I_{IO}	-1		+1	µA	4

DC ELECTRICAL CHARACTERISTICS

(-25°C to 85°C) DS1652

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current, Send Mode	I_{CC1}		3	4	mA	2
Supply Current, Learn Mode	I_{CC2}		3	4	mA	2
Supply Current, Idle State	I_{CC3}	50	75	100	nA	2
V_{CC} Voltage, Learn Mode	V_{CCL}	4.5	5.0	5.5	V	1, 5
Input Leakage (Data Input)	I_{L1}	-1		+1	µA	3
Output High, Voltage	V_{OH}	2.4			V	1, 7
Output High, Current	I_{OH}	4			mA	
Output Low, Voltage	V_{OL}	0.4			V	1, 7
Output Low, Current	I_{OL}	1			mA	

AC ELECTRICAL CHARACTERISTICS DS1653 LOCK AND DS1652 KEY DATA TRANSMISSION PARAMETERS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Reset Active	t_R	540	720	900	µs	
Logic 1 Active	t_1	90	120	150	µs	
Logic 0 Active	t_0	15	20	25	µs	
SEND1 MATCH, SEND2 MATCH, SEND3 MATCH, and SEND4 MATCH	t_M	400	500	600	ms	
Data Sample Window	t_{DS}	1.5	2.0	2.5	ms	
Active Signal Pulse Width, Data I/O	t_{PW}	10		1080	µs	
Active Signal Pulse Width $\overline{\text{SEND1}}$ and $\overline{\text{SEND2}}$	t_S	100			ms	
Delay Between Last Mode Pin Transition to Operation Mode Change	t_T		10		ms	

CAPACITANCE

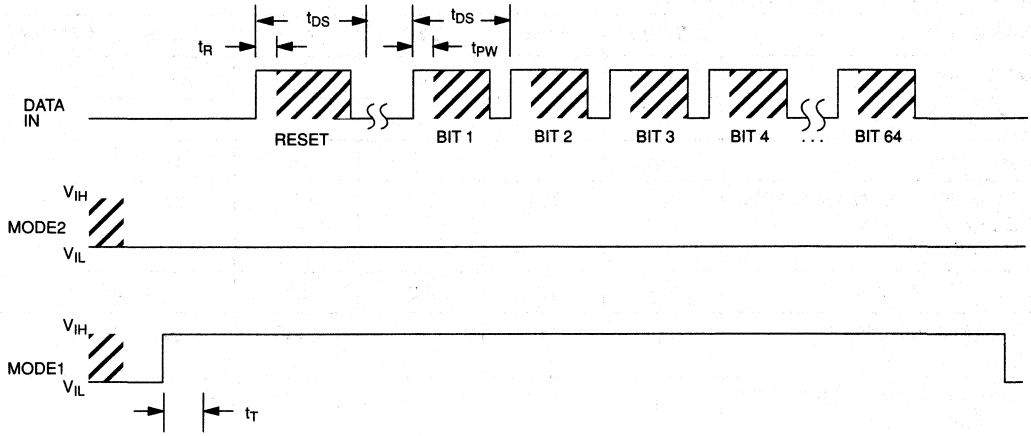
(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

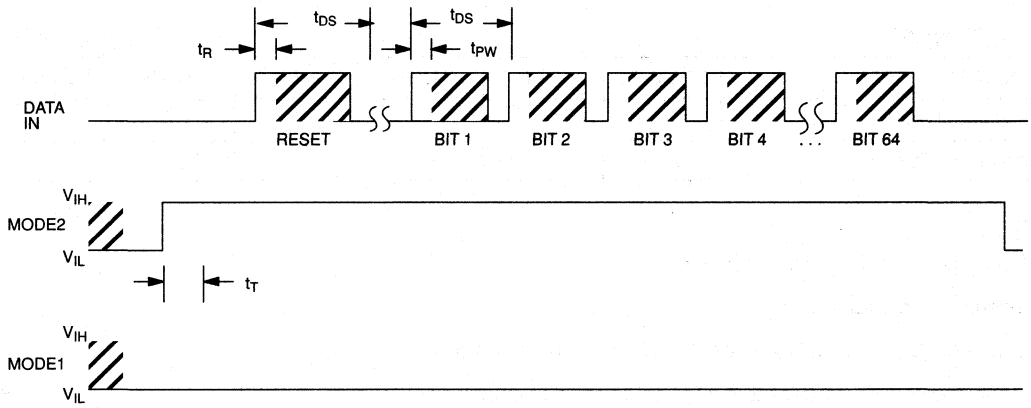
NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. Input leakage applies to DS1652 data I/O pin in input mode only.
4. Input/output leakage applies to the DS1653 data input/output pin.
5. The DS1652 LEARN pin has an internal pulldown.
6. Temperature range for programming is -10°C to +85°C.
7. These output voltages are valid for a typical V_{CC} of 5.0V ± 10%.

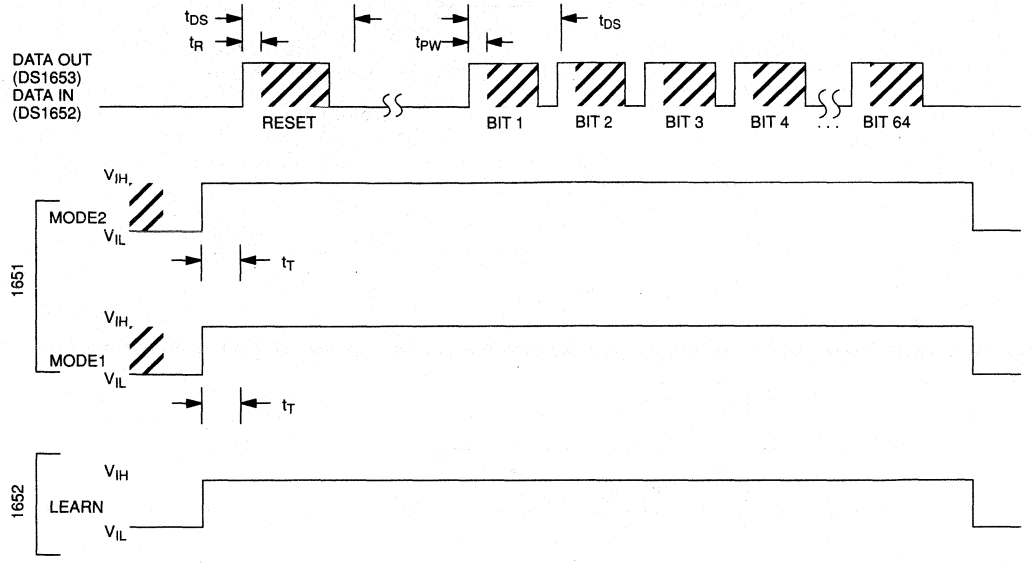
LEARN MODE DS1653 LOCK; USER PROGRAMMING



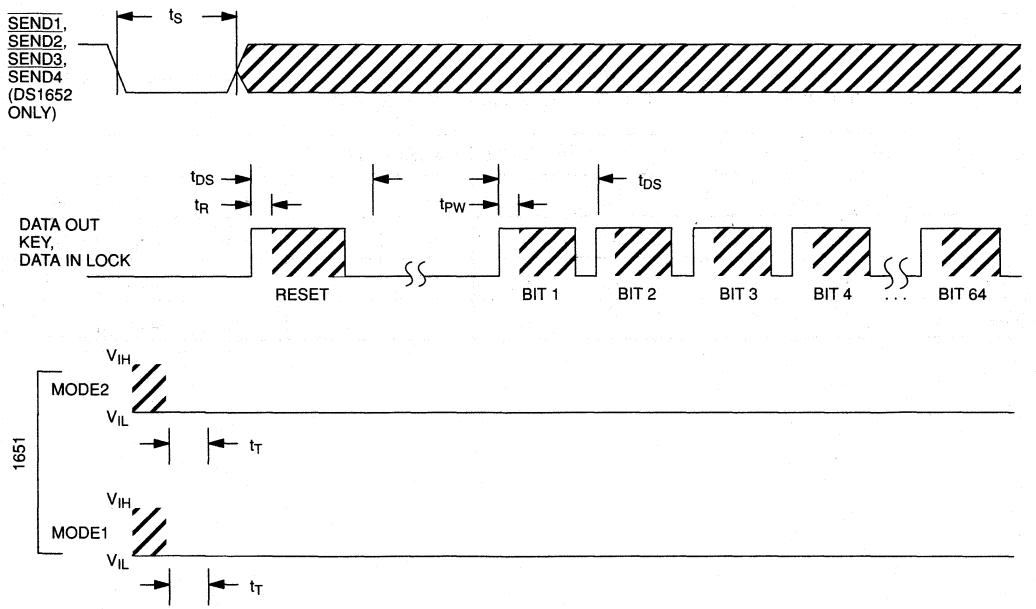
DS1653 LOCK; DUPLICATION MODE



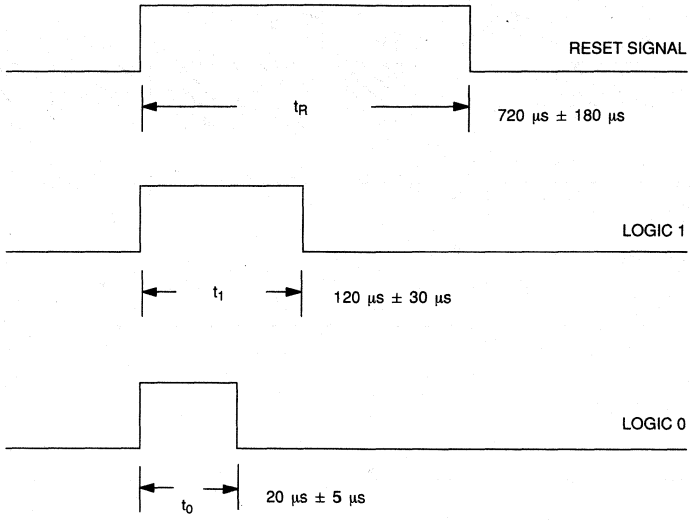
LEARN MODE DS1652 KEY; LEARN MODE DS1653 LOCK, INTERNAL PROGRAMMING



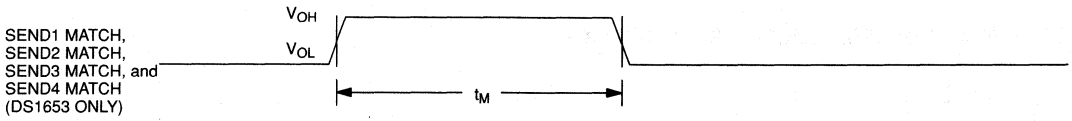
OPERATION DS1653 LOCK AND DS1652 KEY



LOGIC TIMING DIAGRAMS



DS1653 LOCK, MATCH SIGNALS



When the DS1653 Lock's code comparator determines that code data it has received matches one of its code data memories, the appropriate match signal is driven active for the above diagram.

INPUT TRIGGERED	64 CODE TRANSMITTED AS:								
$\overline{SEND1}$	b_0	b_1	b_2	b_3	b_4	. . .	b_{61}	b_{62}	b_{63}
$\overline{SEND2}$	$\overline{b_0}$	$\overline{b_1}$	$\overline{b_2}$	$\overline{b_3}$	$\overline{b_4}$	. . .	$\overline{b_{61}}$	$\overline{b_{62}}$	$\overline{b_{63}}$
$\overline{SEND3}$	b_0	$\overline{b_1}$	b_2	$\overline{b_3}$	b_4	. . .	$\overline{b_{61}}$	b_{62}	$\overline{b_{63}}$
$\overline{SEND4}$	$\overline{b_0}$	b_1	$\overline{b_2}$	b_3	$\overline{b_4}$	. . .	b_{61}	$\overline{b_{62}}$	b_{63}

THERMAL MANAGEMENT

PRELIMINARY

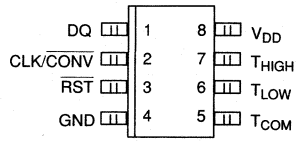
DALLAS SEMICONDUCTOR

DS1620
Digital Thermometer and Thermostat

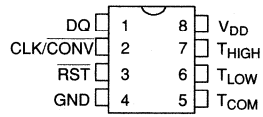
FEATURES

- Requires no external components
- Measures temperatures from –55°C to +125°C in 0.5°C increments. Fahrenheit equivalent is –67°F to 257°F in 0.9°F increments
- Temperature is read as a 9–bit value
- Converts temperature to digital word in 1 second
- Thermostatic settings are user–definable and non–volatile
- Data is read from/written via a 3–wire serial interface (CLK, DQ, $\overline{RST}$)
- Applications include thermostatic controls, industrial systems, consumer products, thermometers, or any thermally sensitive system
- 8–pin DIP or SOIC package

PIN ASSIGNMENT



DS1620S
8–PIN SOIC (200 MIL)
See Mech. Drawing
Pg. 483



DS1620
8–PIN DIP
See Mech. Drawing
Pg. 480

PIN DESCRIPTION

DQ	– 3–Wire Input/Output
CLK/$\overline{CONV}$	– 3–Wire Clock Input and Standalone Convert Input
$\overline{RST}$	– 3–Wire Reset Input
GND	– Ground
T_{HIGH}	– High Temperature Trigger
T_{LOW}	– Low Temperature Trigger
T_{COM}	– High/Low Combination Trigger
V_{DD}	– Power Supply Voltage (+5V)

DESCRIPTION

The DS1620 Digital Thermometer and Thermostat provides 9–bit temperature readings which indicate the temperature of the device. With three thermal alarm outputs, the DS1620 can also act as a thermostat. T_{HIGH} is driven high if the DS1620's temperature is greater than or equal to a user–defined temperature TH. T_{LOW} is driven high if the DS1620's temperature is less than or equal to a user–defined temperature TL. T_{COM} is driven high when the temperature exceeds TH and stays high until the temperature falls below that of TL.

User–defined temperature settings are stored in non–volatile memory, so parts can be programmed prior to insertion in a system, as well as used in standalone applications without a CPU. Temperature settings and temperature readings are all communicated to/from the DS1620 over a simple 3–wire interface.

OPERATION–READING TEMPERATURE

The DS1620 measures temperatures through the use of an onboard, proprietary temperature measurement technique. The temperature reading is provided in a 9–bit, two's complement format. Table 1 describes the exact relationship of output data to measured temperature. The data is transmitted serially through the 3–wire serial interface, LSB first. The DS1620 can measure temperature over the range of –55°C to +125°C in 0.5°C increments. For Fahrenheit usage, a lookup table or conversion factor must be used.

Since data is transmitted over the 3–wire bus LSB first, temperature data can be written to/read from the DS1620 as either a 9–bit word (taking $\overline{RST}$ low after the 9th (MSB) bit), or as two transfers of 8–bit words, with the most significant 7 bits being ignored or set to zero, as illustrated in Table 1. After the MSB, the DS1620 will output 0's.

Note that temperature is represented in the DS1620 in terms of a $^1/_2$°C LSB, yielding the following 9–bit format:

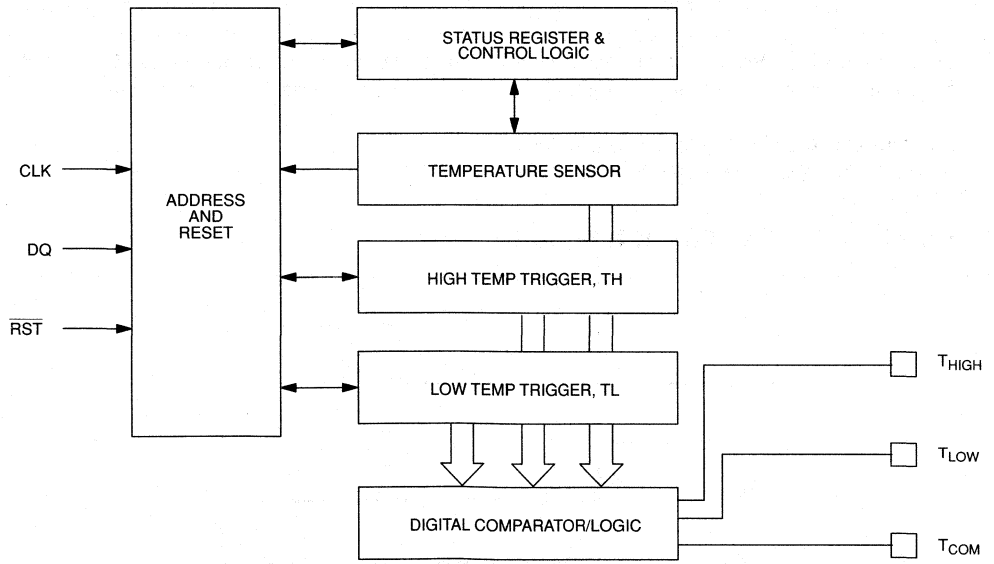
MSB								LSB							
X	X	X	X	X	X	X	1	1	1	0	0	1	1	1	0

T = –25°C

TEMPERATURE/DATA RELATIONSHIPS Table 1

TEMP	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
+125°C	0 11111010	00FA
+25°C	0 00110010	0032h
$^1/_2$°C	0 00000001	0001h
0°C	0 00000000	0000h
–$^1/_2$°C	1 11111111	01FFh
–25°C	1 11001110	01CEh
–55°C	1 10010010	0192h

DS1620 FUNCTIONAL BLOCK DIAGRAM Figure 1



DETAILED PIN DESCRIPTION Table 2

PIN	SYMBOL	DESCRIPTION
1	DQ	**Data Input/Output pin** for 3–wire communication port.
2	CLK/$\overline{CONV}$	**Clock input pin** for 3–wire communication port. When the DS1620 is used in a standalone application with no 3–wire port, this pin can be used as a convert pin. Temperature conversion will begin on the falling edge of $\overline{CONV}$.
3	$\overline{RST}$	**Reset input pin** for 3–wire communication port.
4	GND	**Ground pin.**
5	T_{COM}	**High/Low Combination Trigger.** Goes high when temperature exceeds TH; will reset to low when temperature falls below TL.
6	T_{LOW}	**Low Temperature Trigger.** Goes high when temperature falls below TL.
7	T_{HIGH}	**High Temperature Trigger.** Goes high when temperature exceeds TH.
8	V_{DD}	**Supply Voltage.** 5V input power pin.

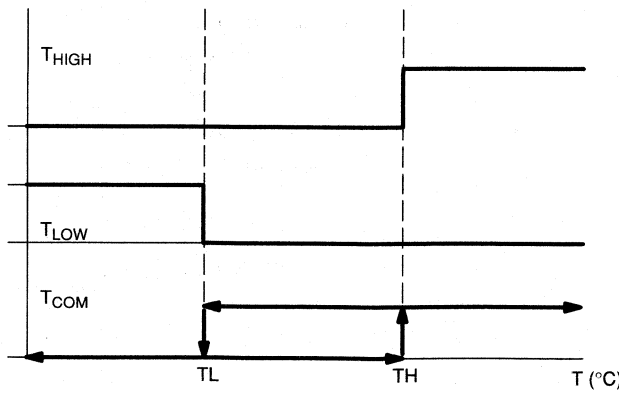
OPERATION–THERMOSTAT CONTROLS

Three thermally triggered outputs, T_{HIGH}, T_{LOW}, and T_{COM}, are provided to allow the DS1620 to be used as a thermostat, as shown in Figure 2. When the DS1620's temperature meets or exceeds the value stored in the high temperature trip register, the output T_{HIGH} becomes active (high) and remains active until the DS1620's measured temperature becomes less than the stored value in the high temperature register, TH. The T_{HIGH} output can be used to indicate that a high temperature tolerance boundary has been met or exceeded, or as part of a closed loop system can be used to activate a cooling system and to deactivate it when the system temperature returns to tolerance.

The T_{LOW} output functions similarly to the T_{HIGH} output. When the DS1620's measured temperature equals or falls below the value stored in the low temperature register, the T_{LOW} output becomes active. T_{LOW} remains active until the DS1620's temperature becomes greater than the value stored in the low temperature register, TL. The T_{LOW} output can be used to indicate that a low temperature tolerance boundary has been met or exceeded, or as part of a closed loop system, can be used to activate a heating system and to deactivate it when the system temperature returns to tolerance.

The T_{COM} output goes high when the measured temperature meets or exceeds TH, and will stay high until the temperature equals or falls below TL. In this way, any amount of hysteresis can be obtained.

THERMOSTAT OUTPUT OPERATION Figure 2



OPERATION AND CONTROL

The DS1620 must have temperature settings resident in the TH and TL registers for thermostatic operation. A configuration/status register is also used to determine the method of operation that the DS1620 will use in a particular application, as well as indicating the status of the temperature conversion operation. The configuration register is defined as follows:

CONFIGURATION/STATUS REGISTER

DONE	THF	TLF	X	X	X	CPU	1SHOT

where

X = Don't Care

DONE = Conversion Done bit. 1=conversion complete, 0=conversion in progress.

THF = Temperature High Flag. This bit will be set to 1 when the temperature is greater than or equal to the value of TH. It will remain 1 until reset by writing 0 into this location or by removing power from the device. This feature provides a method of determining if the DS1620 has ever been subjected to temperatures above TH while power has been applied.

TLF = Temperature Low Flag. This bit will be set to 1 when the temperature is less than or equal to the value of TL. It will remain 1 until reset by writing 0 into this location or by removing power from the device. This feature provides a method of determining if the DS1620 has ever been subjected to temperatures below TL while power has been applied.

CPU = CPU use bit. If CPU=0, the CLK/$\overline{\text{CONV}}$ pin acts as a conversion start control, when $\overline{\text{RST}}$ is low. If CPU is 1, the DS1620 will be used with a CPU communicating to it over the 3–wire port, and the operation of the CLK/$\overline{\text{CONV}}$ pin is as a normal clock in concert with DQ and $\overline{\text{RST}}$.

1SHOT = One–Shot Mode. If 1SHOT is 1, the DS1620 will perform one temperature conversion upon reception of the Start Convert T protocol. If 1SHOT is 0, the DS1620 will continuously perform temperature conversion.

For typical thermostat operation, the DS1620 will operate in continuous mode. However, for applications where only one reading is needed at certain times, and to conserve power, the one–shot mode may be used. Note that the thermostat outputs (T_{HIGH}, T_{LOW}, T_{COM}) will remain in the state they were in after the last valid temperature conversion cycle when operating in one–shot mode.

OPERATION IN STANDALONE MODE

In applications where the DS1620 is used as a simple thermostat, no CPU is required. Since the temperature limits are nonvolatile, the DS1620 can be programmed prior to insertion in the system. In order to facilitate operation without a CPU, the CLK/$\overline{\text{CONV}}$ pin (pin 3) can be used to initiate conversions. Note that the CPU bit must be set to 0 in the configuration register to use this mode of operation.

To use the CLK/$\overline{\text{CONV}}$ pin to initiate conversions, $\overline{\text{RST}}$ must be low and CLK/$\overline{\text{CONV}}$ must be high. If CLK/$\overline{\text{CONV}}$ is driven low and then brought high in less than 10 ms, one temperature conversion will be performed and then the DS1620 will return to an idle state. If CLK/$\overline{\text{CONV}}$ is driven low and remains low, continuous conversions will take place until CLK/$\overline{\text{CONV}}$ is brought high again. With the CPU bit set to 0, the CLK/$\overline{\text{CONV}}$ will override the 1–shot bit if it is equal to 1. This means that even if the part is set for one–shot mode, driving CLK/$\overline{\text{CONV}}$ low will initiate conversions.

3–WIRE COMMUNICATIONS

The 3–wire bus is comprised of three signals. These are the $\overline{\text{RST}}$ (reset) signal, the CLK (clock) signal, and the DQ (data) signal. All data transfers are initiated by driving the $\overline{\text{RST}}$ input high. Driving the $\overline{\text{RST}}$ input low terminates communication. (See Figures 3 and 4.) A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of a clock cycle. Data bits are output on the falling edge of the clock, and remain valid through the rising edge.

When reading data from the DS1620, the DQ pin goes to a high impedance state while the clock is high. Taking $\overline{RST}$ low will terminate any communication and cause the DQ pin to go to a high impedance state.

Data over the 3–wire interface is communicated LSB first. The command set for the 3–wire interface as shown in Table 3 is as follows; only these protocols should be written to the DS1620, as writing other protocols to the device may result in permanent damage to the part.

Read Temperature [AAh]
This command reads the contents of the register which contains the last temperature conversion result. The next nine clock cycles will output the contents of this register.

Write TH [01h]
This command writes to the TH (HIGH TEMPERATURE) register. After issuing this command, the next nine clock cycles clock in the 9–bit temperature limit which will set the threshold for operation of the T_{HIGH} output.

Write TL [02h]
This command writes to the TL (LOW TEMPERATURE) register. After issuing this command, the next nine clock cycles clock in the 9–bit temperature limit which will set the threshold for operation of the T_{LOW} output.

Read TH [A1h]
This command reads the value of the TH (HIGH TEMPERATURE) register. After issuing this command, the next nine clock cycles clock out the 9–bit temperature limit which sets the threshold for operation of the T_{HIGH} output.

Read TL [A2h]
This command reads the value of the TL (LOW TEMPERATURE) register. After issuing this command, the next nine clock cycles clock out the 9–bit temperature limit which sets the threshold for operation of the T_{LOW} output.

Start Convert T [EEh]
This command begins a temperature conversion. No further data is required. In one–shot mode, the temperature conversion will be performed and then the DS1620 will remain idle. In continuous mode, this command will initiate continuous conversions.

Stop Convert T [22h]
This command stops temperature conversion. No further data is required. This command may be used to halt a DS1620 in continuous conversion mode. After issuing this command, the current temperature measurement will be completed, and then the DS1620 will remain idle until a Start Convert T is issued to resume continuous operation.

Write Config [0Ch]
This command writes to the configuration register. After issuing this command, the next eight clock cycles clock in the value of the configuration register.

Read Config [ACh]
This command reads the value in the configuration register. After issuing this command, the next eight clock cycles output the value of the configuration register.

DS1620 COMMAND SET Table 3

INSTRUCTION	DESCRIPTION	PROTOCOL	3–WIRE BUS DATA AFTER ISSUING PROTOCOL	NOTES
TEMPERATURE CONVERSION COMMANDS				
Read Temperature	Reads last converted temperature value from temperature register.	AAh	<read data>	
Start Convert T	Initiates temperature conversion.	EEh	idle	1
Stop Convert T	Halts temperature conversion.	22h	idle	1
THERMOSTAT COMMANDS				
Write TH	Writes high temperature limit value into TH register.	01h	<write data>	2
Write TL	Writes low temperature limit value into TL register.	02h	<write data>	2
Read TH	Reads stored value of high temperature limit from TH register.	A1h	<read data>	2
Read TL	Reads stored value of low temperature limit from TL register.	A2h	<read data>	2
Write Config	Writes configuration data to configuration register.	0Ch	<write data>	2
Read Config	Reads configuration data from configuration register.	ACh	<read data>	2

NOTES:

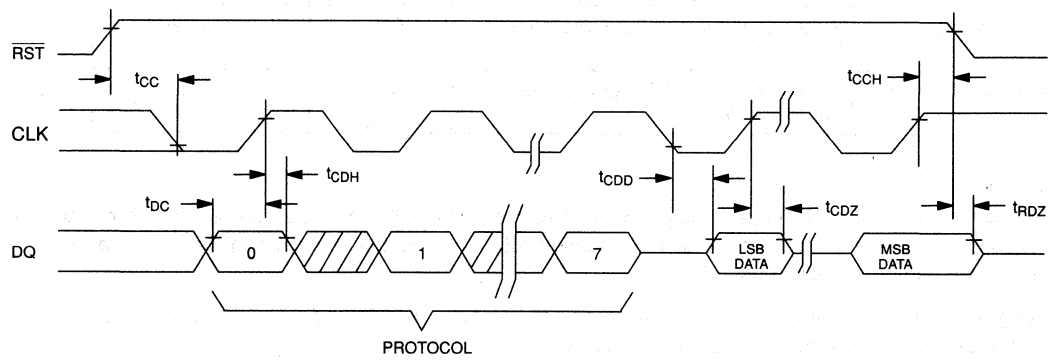
1. In continuous conversion mode, a Stop Convert T command will halt continuous conversion. To restart, the Start Convert T command must be issued. In one–shot mode, a Start Convert T command must be issued for every temperature reading desired.
2. Writing to the E^2 typically requires 10 ms at room temperature. After issuing a write command, no further reads or writes should be requested for at least 10 ms.

FUNCTION EXAMPLE

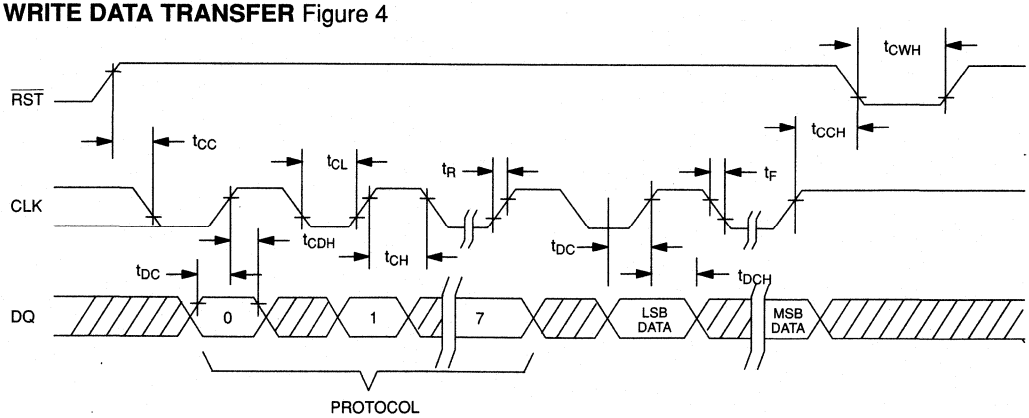
Example: CPU sets up DS1620 for continuous conversion and thermostatic function.

CPU MODE	DS1620 MODE (3–WIRE)	DATA (LSB FIRST)	COMMENTS
TX	RX	0Ch	CPU issues Write Config command.
TX	RX	00h	CPU sets DS1620 up for continuous conversion.
TX	RX	01h	CPU issues Write TH command.
TX	RX	0050h	CPU sends data for TH limit of +40°C.
TX	RX	02h	CPU issues Write TL command.
RX	TX	0014h	CPU sends data for TL limit of +10°C.
TX	RX	A1h	CPU issues Read TH command.
RX	TX	0050h	DS1620 sends back stored value of TH for CPU to verify.
TX	RX	A2h	CPU issues Read TL command.
RX	TX	0014h	DS1620 sends back stored value of TL for CPU to verify.
TX	RX	EEh	CPU issues Start Convert T command.

READ DATA TRANSFER Figure 3



WRITE DATA TRANSFER Figure 4



NOTE: t_{CL}, t_{CH}, t_R, and t_F apply to both read and write data transfer.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

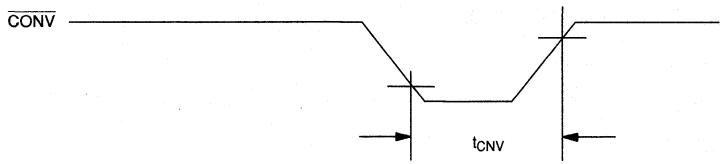
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply	V_{DD}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.0		V_{CC}+0.3	V	1
Logic 0	V_{IL}	–0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(–55°C to +125°C; V_{DD}=4.5V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	MAX	UNITS	NOTES
Thermometer Error	T_{ERR}	0°C to +70°C		$\pm^1/_2$	°C	
		–40°C to +0°C and +70°C to +85°C		±1	°C	
		–55°C to –40°C and +85°C to +125°C		±2	°C	
Logic 0 Output	V_{OL}			0.4	V	3
Logic 1 Output	V_{OH}		2.4		V	2
Input Resistance	R_I	$\overline{RST}$ to GND DQ,CLK to V_{DD}		2 2	mΩ mΩ	
Active Supply Current	I_{CC}	0°C to +70°C		1	mA	4, 5
Standby Supply Current	I_{STBY}	0°C to +70°C		1	µA	4, 5

SINGLE CONVERT TIMING DIAGRAM (STAND–ALONE MODE)



AC ELECTRICAL CHARACTERISTICS

(–55°C to +125°C; V_{DD}=4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Temperature Conversion Time	T_{TC}			1	s	
Data to CLK Setup	t_{DC}	35			ns	6
CLK to Data Hold	t_{CDH}	40			ns	6
CLK to Data Delay	t_{CDD}			100	ns	6, 7, 8
CLK Low Time	t_{CL}	250			ns	6
CLK High Time	t_{CH}	250			ns	6
CLK Frequency	f_{CLK}	DC		2.0	MHz	6
CLK Rise and Fall	t_R, t_F			500	ns	
$\overline{RST}$ to CLK Setup	t_{CC}	100			ns	6
CLK to $\overline{RST}$ Hold	t_{CCH}	40			ns	6
$\overline{RST}$ Inactive Time	t_{CWH}	125			ns	6, 9
CLK High to I/O High Z	t_{CDZ}			50	ns	6
$\overline{RST}$ Low to I/O High Z	t_{RDZ}			50	ns	6
Convert Pulse Width	t_{CNV}	250 ns		500 ms		
NV Write Cycle Time	t_{WR}		10	50	ms	

AC ELECTRICAL CHARACTERISTICS

(–55°C to +125°C; V_{DD}=4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_I		5		pF	
I/O Capacitance	$C_{I/O}$		10		pF	

NOTES:

1. All voltages are referenced to ground.
2. Logic one voltages are specified at a source current of 1 mA.
3. Logic zero voltages are specified at a sink current of 4 mA.
4. I_{CC} specified with DQ pin open.
5. I_{CC} specified with V_{CC} at 5.0V and $\overline{RST}$=GND.
6. Measured at V_{IH} = 2.0V or V_{IL} = 0.8V.
7. Measured at V_{OH} = 2.4V or V_{OL} = 0.4V.
8. Load capacitance = 50 pF.
9. t_{CWH} must be 10 ms minimum following any read or write command that involves the E^2 memory.

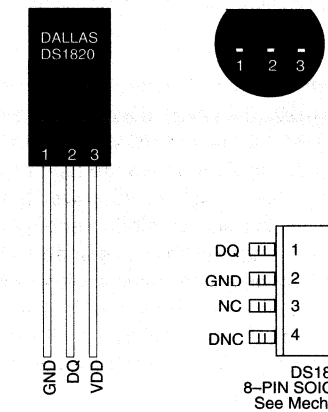
DALLAS SEMICONDUCTOR

DS1820
One–Wire Digital Thermometer

FEATURES

- Unique 1–Wire interface requires only one port pin for communication
- Multidrop capability simplifies distributed temperature sensing applications
- Requires no external components
- Can be powered from data line
- Zero standby power required
- Measures temperatures from –55°C to +125°C in 0.5°C increments. Fahrenheit equivalent is –67°F to 257°F in 0.9°F increments
- Temperature is read as a 9–bit digital value.
- Converts temperature to digital word in 1 second (typ.)
- User–definable, nonvolatile temperature alarm settings
- Alarm search command identifies and addresses devices whose temperature is outside of programmed limits (temperature alarm condition)
- Applications include thermostatic controls, industrial systems, consumer products, thermometers, or any thermally sensitive system

PIN ASSIGNMENT



DS1820
PR–35 PACKAGE

DS1820S
8–PIN SOIC (200 MIL)
See Mech. Drawing
Pg. 483

PIN DESCRIPTION

GND	–	Ground
DQ	–	Data In/Out
V_{DD}	–	Optional V_{DD}
NC	–	No Connect
DNC	–	Do Not Connect

DESCRIPTION

The DS1820 Digital Thermometer provides 9–bit temperature readings which indicate the temperature of the device.

Information is sent to/from the DS1820 over a 1–Wire interface, so that only one wire (and ground) needs to be connected from a central microprocessor to a DS1820. Power for reading, writing, and performing temperature conversions can be derived from the data line itself with no need for an external power source.

Because each DS1820 contains a unique silicon serial number, multiple DS1820s can exist on the same 1–Wire bus. This allows for placing temperature sensors in many different places. Applications where this feature is useful include HVAC environmental controls, sensing temperatures inside buildings, equipment or machinery, and in process monitoring and control.

DETAILED PIN DESCRIPTION

PIN 8–PIN SOIC	PIN PR35	SYMBOL	DESCRIPTION
5	1	GND	**Ground.**
4	2	DQ	**Data Input/Output pin** for 1–Wire operation: Open drain. (See "Parasite Power" section.)
3	3	V_{DD}	**Optional V_{DD} pin.** See "Parasite Power" section for details of connection.

DS1820S (8–pin SOIC): All pins not specified in this table are not to be connected.

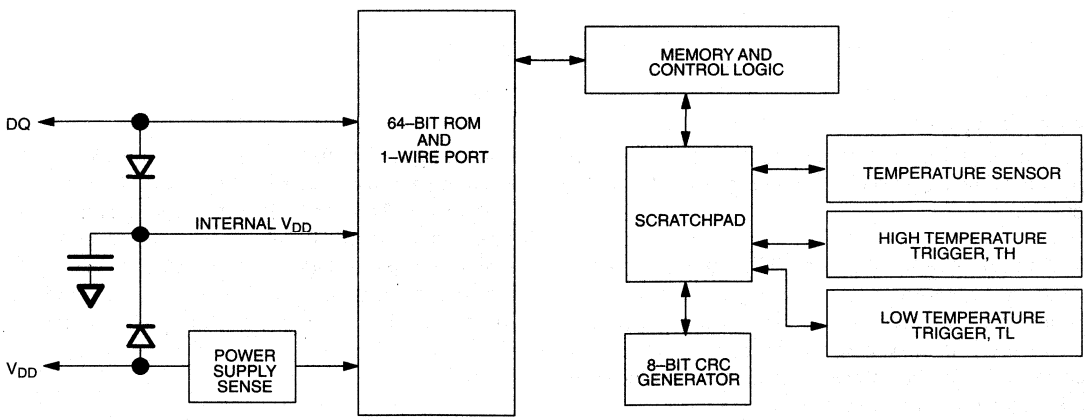
OVERVIEW

The block diagram of Figure 1 shows the major components of the DS1820. The DS1820 has three main data components: 1) 64–bit lasered ROM, 2) temperature sensor, and 3) nonvolatile temperature alarm triggers TH and TL. The device derives its power from the 1–Wire communication line by storing energy on an internal capacitor during periods of time when the signal line is high and continues to operate off this power source during the low times of the 1–Wire line until it returns high to replenish the parasite (capacitor) supply. As an alternative, the DS1820 may also be powered from an external 5V supply.

Communication to the DS1820 is via a 1–Wire port. With the 1–Wire port, the memory and control functions will not be available before the ROM function protocol has been established. The master must first provide one of five ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM, or 5) Alarm Search. These commands operate on the 64–bit lasered ROM portion of each device and can single out a specific device if many are present on the 1–Wire line as well as indicate to the bus master how many and what types of devices are present. After a ROM function sequence has been successfully executed, the memory and control functions are accessible and the master may then provide any one of the six memory and control function commands.

One control function command instructs the DS1820 to perform a temperature measurement. The result of this measurement will be placed in the DS1820's scratchpad memory, and may be read by issuing a memory function command which reads the contents of the scratchpad memory. The temperature alarm triggers TH and TL consist of one byte EEPROM each. If the alarm search command is not applied to the DS1820, these registers may be used as general purpose user memory. Writing TH and TL is done using a memory function command. Read access to these registers is through the scratchpad. All data is read and written least significant bit first.

DS1820 BLOCK DIAGRAM Figure 1



PARASITE POWER

The block diagram (Figure 1) shows the parasite powered circuitry. This circuitry "steals" power whenever the I/O or V_{DD} pins are high. I/O will provide sufficient power as long as the specified timing and voltage requirements are met (see the section titled "1–Wire Bus System"). The advantages of parasite power are two–fold: 1) by parasiting off this pin, no local power source is needed for remote sensing of temperature, and 2) the ROM may be read in absence of normal power.

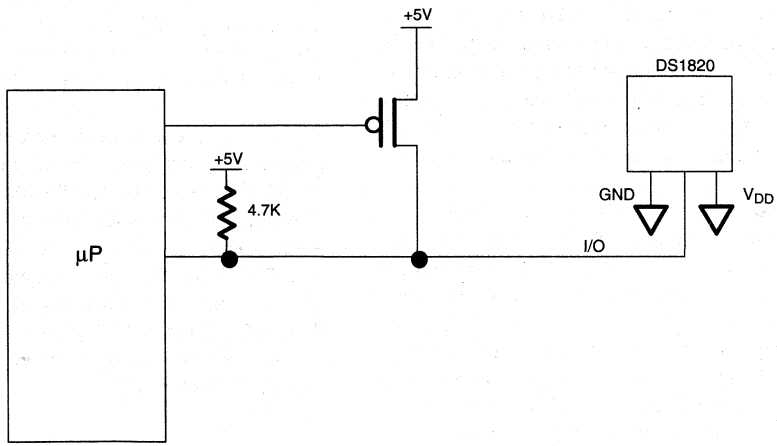
In order for the DS1820 to be able to perform accurate temperature conversions, sufficient power must be provided over the I/O line when a temperature conversion is taking place. Since the operating current of the DS1820 is up to 1 mA, the I/O line will not have sufficient drive due to the 5K pullup resistor. This problem is particularly acute if several DS1820's are on the same I/O and attempting to convert simultaneously.

There are two ways to assure that the DS1820 has sufficient supply current during its active conversion cycle. The first is to provide a strong pullup on the I/O line whenever temperature conversion is taking place. This may be accomplished by using a MOSFET to pull the I/O line directly to the power supply as shown in Figure 2. When using the parasite power mode, the V_{DD} pin must be tied to ground.

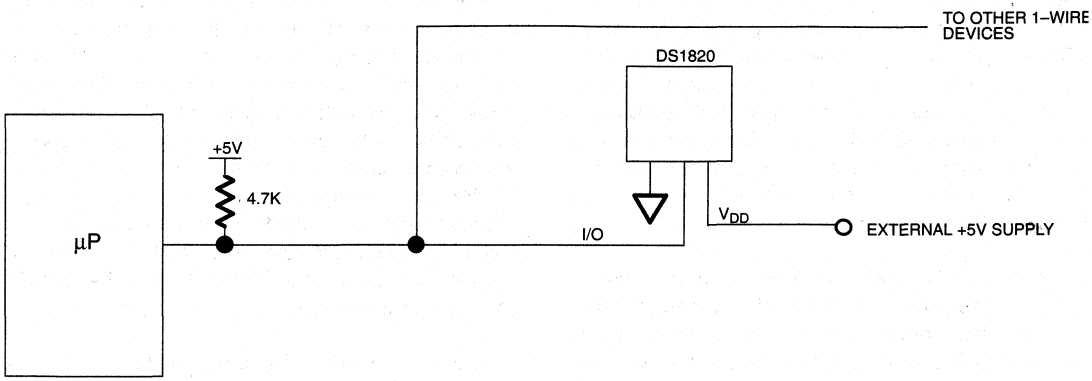
Another method of supplying current to the DS1820 is through the use of an external power supply tied to the V_{DD} pin, as shown in Figure 3. The advantage to this is that the strong pullup is not required on the I/O line, and the bus master need not be tied up holding that line high during temperature conversions. This allows other data traffic on the 1–Wire bus during the conversion time. In addition, any number of DS1820's may be placed on the 1–Wire bus, and if they all use external power, they may all simultaneously perform temperature conversions by issuing the Skip ROM command and then issuing the Convert T command. Note that as long as the external power supply is active, the GND pin may not be floating.

For situations where the bus master does not know whether the DS1820's on the bus are parasite powered or supplied with external V_{DD}, a provision is made in the DS1820 to signal the power supply scheme used. The bus master can determine if any DS1820's are on the bus which require the strong pullup by sending a Skip ROM protocol, then issuing the read power supply command. After this command is issued, the master then issues read time slots. The DS1820 will send back "0" on the 1–Wire bus if it is parasite powered; it will send back a "1" if it is powered from the V_{DD} pin. If the master receives a "0", it knows that it must supply the strong pull–up on the I/O line during temperature conversions. See "Memory Command Functions" section for more detail on this command protocol.

STRONG PULL–UP FOR SUPPLYING DS1820 DURING TEMPERATURE CONVERSION Figure 2



USING V_{DD} TO SUPPLY TEMPERATURE CONVERSION CURRENT Figure 3



OPERATION – MEASURING TEMPERATURE

The DS1820 measures temperatures through the use of an on–board proprietary temperature measurement technique. A block diagram of the temperature measurement circuitry is shown in Figure 4.

The DS1820 measures temperature by counting the number of clock cycles that an oscillator with a low temperature coefficient goes through during a gate period determined by a high temperature coefficient oscillator. The counter is preset with a base count that corresponds to –55°C. If the counter reaches zero before the gate period is over, the temperature register, which is also preset to the –55°C value, is incremented, indicating that the temperature is higher than –55°C.

At the same time, the counter is then preset with a value determined by the slope accumulator circuitry. This circuitry is needed to compensate for the parabolic behavior of the oscillators over temperature. The counter is then clocked again until it reaches zero. If the gate period is still not finished, then this process repeats.

The slope accumulator is used to compensate for the non–linear behavior of the oscillators over temperature, yielding a high resolution temperature measurement. This is done by changing the number of counts necessary for the counter to go through for each incremental degree in temperature. To obtain the desired resolution, therefore, both the value of the counter and the number of counts per degree C (the value of the slope accumulator) at a given temperature must be known.

Internally, this calculation is done inside the DS1820 to provide 0.5°C resolution. The temperature reading is provided in a 16–bit, sign–extended two's complement reading. Table 1 describes the exact relationship of output data to measured temperature. The data is transmitted serially over the 1–Wire interface. The DS1820 can measure temperature over the range of –55°C to +125°C in 0.5°C increments. For Fahrenheit usage, a lookup table or conversion factor must be used.

Note that temperature is represented in the DS1820 in terms of a $^1/_2$°C LSB, yielding the following 9–bit format:

MSB								LSB
1	1	1	0	0	1	1	1	0

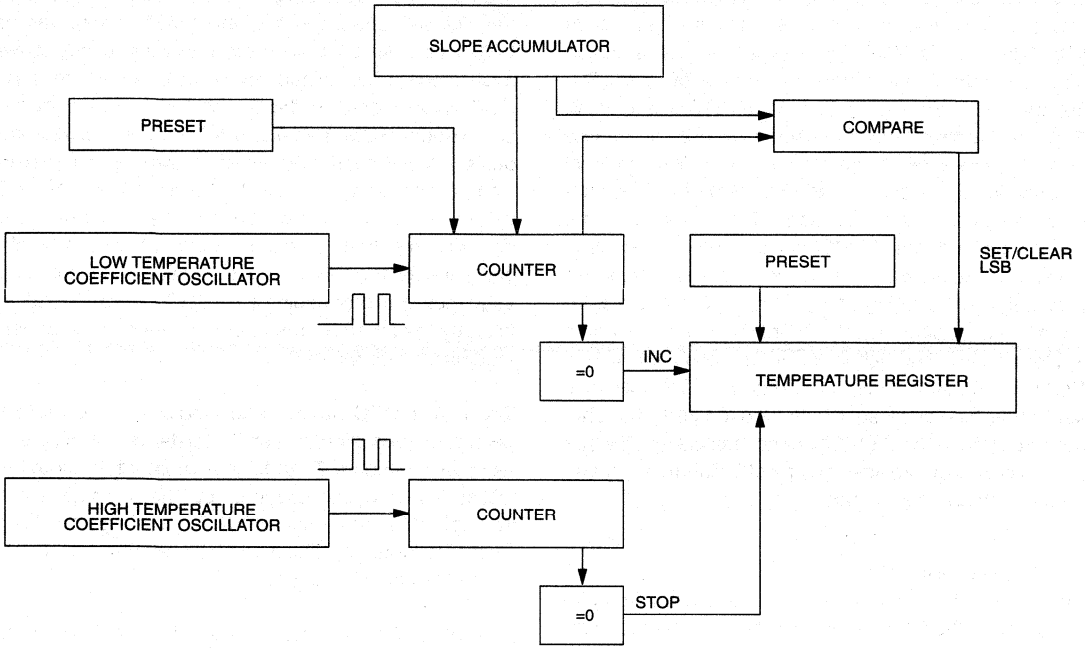
= –25°C

The most significant (sign) bit is duplicated into all of the bits in the upper MSB of the two–byte temperature register in memory. This "sign–extension" yields the 16–bit temperature readings as shown in Table 1.

Higher resolutions may be obtained by the following procedure. First, read the temperature, and truncate the 0.5°C bit (the LSB) from the read value. This value is TEMP_READ. The value left in the counter may then be read. This value is the count remaining (COUNT_REMAIN) after the gate period has ceased. The last value needed is the number of counts per degree C (COUNT_PER_C) at that temperature. The actual temperature may be then be calculated by the user using the following:

$$\text{TEMPERATURE} = \text{TEMP\_READ} - 0.25 + \frac{(\text{COUNT\_PER\_C} - \text{COUNT\_REMAIN})}{\text{COUNT\_PER\_C}}$$

TEMPERATURE MEASURING CIRCUITRY Figure 4



TEMPERATURE/DATA RELATIONSHIPS Table 1

TEMPERATURE	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
+125°C	00000000 11111010	00FA
+25°C	00000000 00110010	0032h
$+^1/_2$°C	00000000 00000001	0001h
+0°C	00000000 00000000	0000h
$-^1/_2$°C	11111111 11111111	FFFFh
–25°C	11111111 11001110	FFCEh
–55°C	11111111 10010010	FF92h

OPERATION – ALARM SIGNALLING

After the DS1820 has performed a temperature conversion, the temperature value is compared to the trigger values stored in TH and TL. Since these registers are 8 bit only, the 0.5°C bit is ignored for comparison. The most significant bit of TH or TL directly corresponds to the sign bit of the 16–bit temperature register. If the result of a temperature measurement is higher than TH or lower than TL, an alarm flag inside the device is set. This flag is updated with every temperature measurement. As long as the alarm flag is set, the DS1820 will respond to the alarm search command. This allows many DS1820s to be connected in parallel doing simultaneous temperature measurements. If somewhere the temperature exceeds the limits, the alarming device(s) can be identified and read immediately without having to read non–alarming devices.

64–BIT LASERED ROM

Each DS1820 contains a unique ROM code that is 64 bits long. The first eight bits are a 1–Wire family code (DS1820 code is 10h). The next 48 bits are a unique serial number. The last eight bits are a CRC of the first 56 bits. (See Figure 5.) The 64–bit ROM and ROM Function Control section allow the DS1820 to operate as a 1–Wire device and follow the 1–Wire protocol detailed in the section "1–Wire Bus System". The functions required to control sections of the DS1820 are not accessible until the ROM function protocol has been satisfied. This protocol is described in the ROM function protocol flowchart (Figure 6). The 1–Wire bus master must first provide one of five ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM, or 5) Alarm Search. After a ROM functions sequence has been successfully executed, the functions specific to the DS1820 are accessible and the bus master may then provide and one of the six memory and control function commands.

CRC GENERATION

The DS1820 has an 8–bit CRC stored in the most significant byte of the 64–bit ROM. The bus master can compute a CRC value from the first 56 bits of the 64–bit ROM and compare it to the value stored within the DS1820 to determine if the ROM data has been received error–free by the bus master. The equivalent polynomial function of this CRC is:

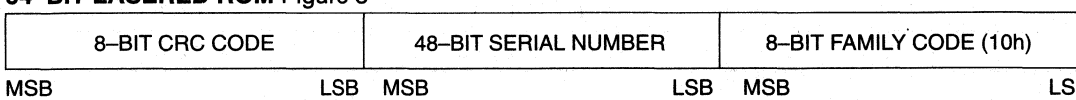
$$CRC = X^8 + X^5 + X^4 + 1$$

The DS1820 also generates an 8–bit CRC value using the same polynomial function shown above and provides this value to the bus master to validate the transfer of data bytes. In each case where a CRC is used for data transfer validation, the bus master must calculate a CRC value using the polynomial function given above and compare the calculated value to either the 8–bit CRC value stored in the 64–bit ROM portion of the DS1820 (for ROM reads) or the 8–bit CRC value computed within the DS1820 (which is read as a ninth byte when the scratchpad is read). The comparison of CRC values and decision to continue with an operation are determined entirely by the bus master. There is no circuitry inside the DS1820 that prevents a command sequence from proceeding if the CRC stored in or calculated by the DS1820 does not match the value generated by the bus master.

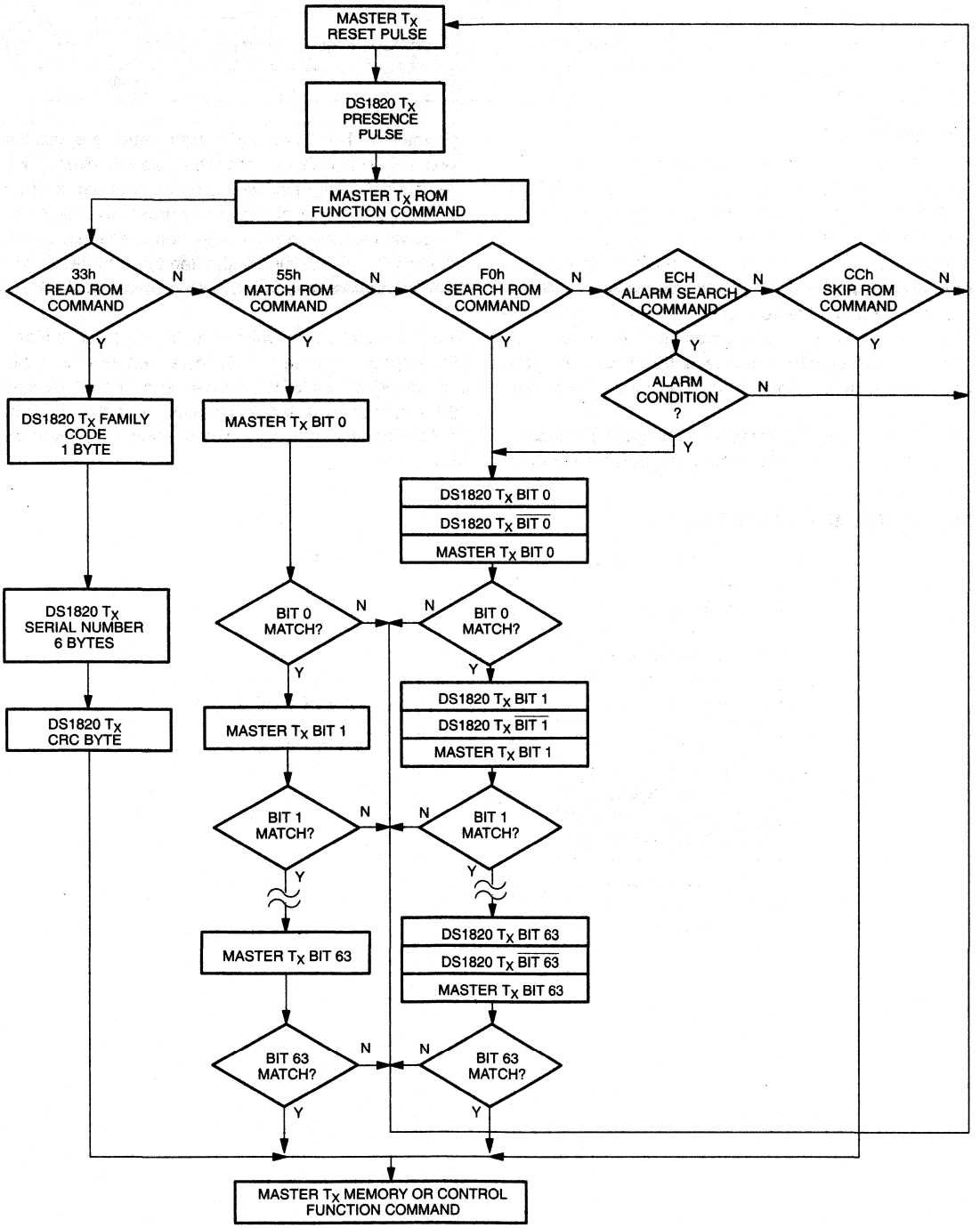
The 1–Wire CRC can be generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 7. Additional information about the Dallas 1–Wire Cyclic Redundancy Check is available in an application note entitled "Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Products".

The shift register bits are initialized to zero. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the eight bits of CRC should return the shift register to all zeros.

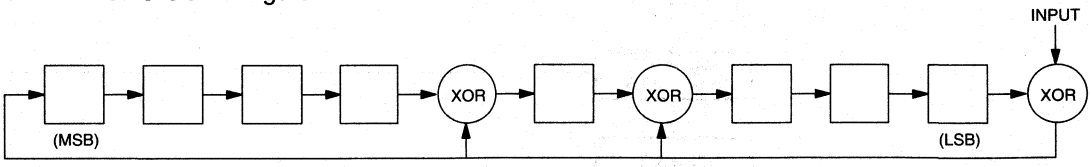
64–BIT LASERED ROM Figure 5



ROM FUNCTIONS FLOW CHART Figure 6



1–WIRE CRC CODE Figure 7



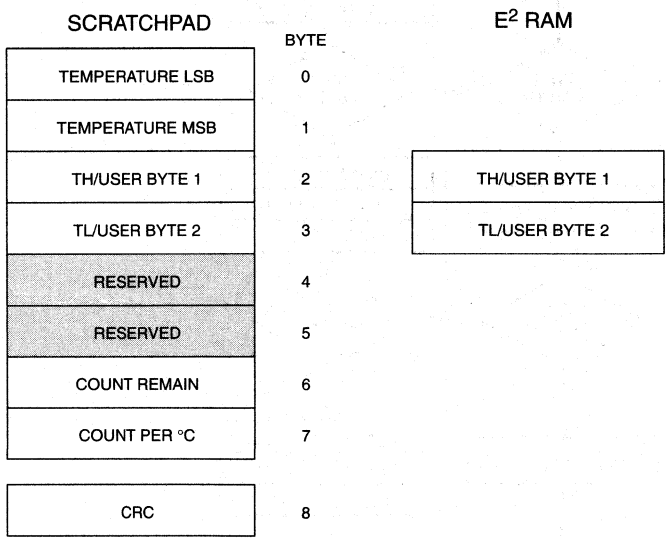
MEMORY

The DS1820's memory is organized as shown in Figure 8. The memory consists of a scratchpad RAM and a nonvolatile, electrically erasable (E^2) RAM, which stores the high and low temperature triggers TH and TL. The scratchpad helps insure data integrity when communicating over the 1–Wire bus. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command will transfer the data to the nonvolatile (E^2) RAM. This process insures data integrity when modifying the memory.

The scratchpad is organized as eight bytes of memory. The first two bytes contain the measured temperature information. The third and fourth bytes are volatile copies of TH and TL and are refreshed with every power–on reset. The next two bytes are not used; upon reading back, however, they will appear as all logic 1's. The seventh and eighth bytes are count registers, which may be used in obtaining higher temperature resolution (see "Operation–measuring Temperature" section).

There is a ninth byte which may be read with a Read Scratchpad command. This byte contains a cyclic redundancy check (CRC) byte which is the CRC over all of the eight previous bytes. This CRC is implemented in the fashion described in the section titled "CRC Generation".

DS1820 MEMORY MAP Figure 8



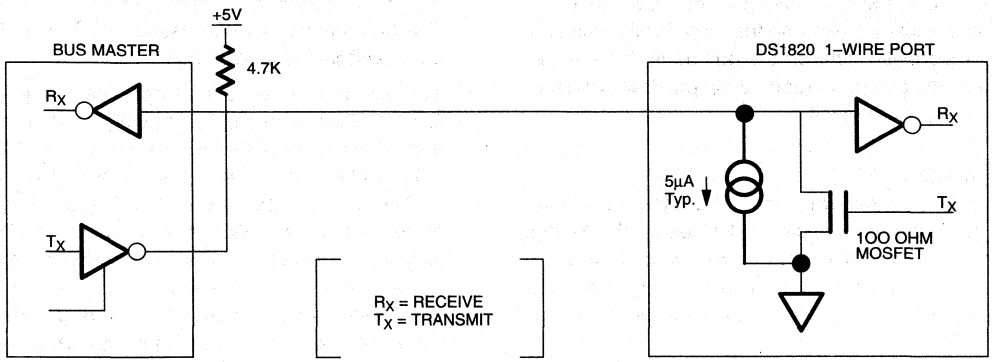
1–WIRE BUS SYSTEM

The 1–Wire bus is a system which has a single bus master and one or more slaves. The DS1820 behaves as a slave. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1–Wire signaling (signal types and timing).

HARDWARE CONFIGURATION

The 1–Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1–Wire bus must have open drain or 3–state outputs. The 1–Wire port of the DS1820 (I/O pin) is open drain with an internal circuit equivalent to that shown in Figure 9. A multidrop bus consists of a 1–Wire bus with multiple slaves attached. The 1–Wire bus requires a pullup resistor of approximately 5KΩ.

HARDWARE CONFIGURATION Figure 9



The idle state for the 1–Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 480 µs, all components on the bus will be reset.

TRANSACTION SEQUENCE

The protocol for accessing the DS1820 via the 1–Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1–Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS1820 is on the bus and is ready to operate. For more details, see the "1–Wire Signaling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 6):

Read ROM [33h]

This command allows the bus master to read the DS1820's 8–bit family code, unique 48–bit serial number, and 8–bit CRC. This command can only be used if there is a single DS1820 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired AND result).

Match ROM [55h]
The match ROM command, followed by a 64–bit ROM sequence, allows the bus master to address a specific DS1820 on a multidrop bus. Only the DS1820 that exactly matches the 64–bit ROM sequence will respond to the following memory function command. All slaves that do not match the 64–bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

Skip ROM [CCh]
This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64–bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pulldowns will produce a wired AND result).

Search ROM [F0h]
When a system is initially brought up, the bus master might not know the number of devices on the 1–Wire bus or their 64–bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64–bit ROM codes of all slave devices on the bus.

Alarm Search [ECh]
The flowchart of this command is identical to the Search ROM command. However, the DS1820 will respond to this command only if an alarm condition has been encountered at the last temperature measurement. An alarm condition is defined as a temperature higher than TH or lower than TL. The alarm condition remains set as long as the DS1820 is powered up, until another temperature measurement reveals a non–alarming value, or the settings of TH or TL are modified so that the measured value again is within the allowed limits. For alarming, the trigger values stored in EEPROM are taken into acccount.

Example of a ROM Search
The ROM search process is the repetition of a simple 3–step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, 3–step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes.

The following example of the ROM search process assumes four different devices are connected to the same 1–Wire bus. The ROM data of the four devices is as shown:

ROM1	00110101...
ROM2	10101010...
ROM3	11110101...
ROM4	00010001...

The search process is as follows:

1. The bus master begins the initialization sequence by issuing a reset pulse. The slave devices respond by issuing simultaneous presence pulses.
2. The bus master will then issue the Search ROM command on the 1–Wire bus.
3. The bus master reads a bit from the 1–Wire bus. Each device will respond by placing the value of the first bit of their respective ROM data onto the 1–Wire bus. ROM1 and ROM4 will place a 0 onto the 1–Wire bus, i.e., pull it low. ROM2 and ROM3 will place a 1 onto the 1–Wire bus by allowing the line to stay high. The result is the logical AND of all devices on the line, therefore the bus master sees a 0. The bus master reads another bit. Since the Search ROM data command is being executed, all of the devices on the 1–Wire bus respond to this second read by placing the complement of the first bit of their respective ROM data onto the 1–Wire bus. ROM1 and ROM4 will place a 1 onto the 1–Wire, allowing the line to stay high. ROM2 and ROM3 will place a 0 onto the 1–Wire, thus it will be pulled low. The bus master again observes a 0 for the complement of the first ROM data bit. The bus master has determined that there are some devices on the 1–Wire bus that have a 0 in the first position and others that have a 1.

   The data obtained from the two reads of the 3–step routine have the following interpretations:

   00 There are still devices attached which have conflicting bits in this position.

   01 All devices still coupled have a 0 bit in this bit position.

   10 All devices still coupled have a 1 bit in this bit position.

   11 There are no devices attached to the 1–Wire bus.

4. The bus master writes a 0. This deselects ROM2 and ROM3 for the remainder of this search pass, leaving only ROM1 and ROM4 connected to the 1–Wire bus.
5. The bus master performs two more reads and receives a 0 bit followed by a 1 bit. This indicates that all devices still coupled to the bus have 0's as their second ROM data bit.
6. The bus master then writes a 0 to keep both ROM1 and ROM4 coupled.
7. The bus master executes two reads and receives two 0 bits. This indicates that both 1 bits and 0 bits exist as the third bit of the ROM data of the attached devices.
8. The bus master writes a 0 bit. This deselects ROM1 leaving ROM4 as the only device still connected.
9. The bus master reads the remainder of the ROM bits for ROM4 and continues to access the part if desired. This completes the first pass and uniquely identifies one part on the 1–Wire bus.
10. The bus master starts a new ROM search sequence by repeating steps 1 through 7.
11. The bus master writes a 1 bit. This decouples ROM4, leaving only ROM1 still coupled.
12. The bus master reads the remainder of the ROM bits for ROM1 and communicates to the underlying logic if desired. This completes the second ROM search pass, in which another of the ROMs was found.
13. The bus master starts a new ROM search by repeating steps 1 through 3.
14. The bus master writes a 1 bit. This deselects ROM1 and ROM4 for the remainder of this search pass, leaving only ROM2 and ROM3 coupled to the system.
15. The bus master executes two read time slots and receives two zeros.
16. The bus master writes a 0 bit. This decouples ROM3, and leaving only ROM2.
17. The bus master reads the remainder of the ROM bits for ROM2 and communicates to the underlying logic if desired. This completes the third ROM search pass, in which another of the ROMs was found.
18. The bus master starts a new ROM search by repeating steps 13 through 15.
19. The bus master writes a 1 bit. This decouples ROM2, leaving only ROM3.
20. The bus master reads the remainder of the ROM bits for ROM3 and communicates to the underlying logic if desired. This completes the fourth ROM search pass, in which another of the ROMs was found.

Note the following:

The bus master learns the unique ID number (ROM data pattern) of one 1–Wire device on each ROM Search operation. The time required to derive the part's unique ROM code is:

$$960\ \mu s + (8 + 3 \times 64)\ 61\ \mu s = 13.16\ ms$$

The bus master is therefore capable of identifying 75 different 1–Wire devices per second.

I/O SIGNALING

The DS1820 requires strict protocols to insure data integrity. The protocol consists of several types of signaling on one line: reset pulse, presence pulse, write 0, write 1, read 0, and read 1. All of these signals, with the exception of the presence pulse, are initiated by the bus master.

The initialization sequence required to begin any communication with the DS1820 is shown in Figure 11. A reset pulse followed by a presence pulse indicates the DS1820 is ready to send or receive data given the correct ROM command and memory function command.

The bus master transmits (TX) a reset pulse (a low signal for a minimum of 480 µs). The bus master then releases the line and goes into a receive mode (RX). The 1–Wire bus is pulled to a high state via the 5K pull–up resistor . After detecting the rising edge on the I/O pin, the DS1820 waits 15–60 µs and then transmits the presence pulse (a low signal for 60–240 µs).

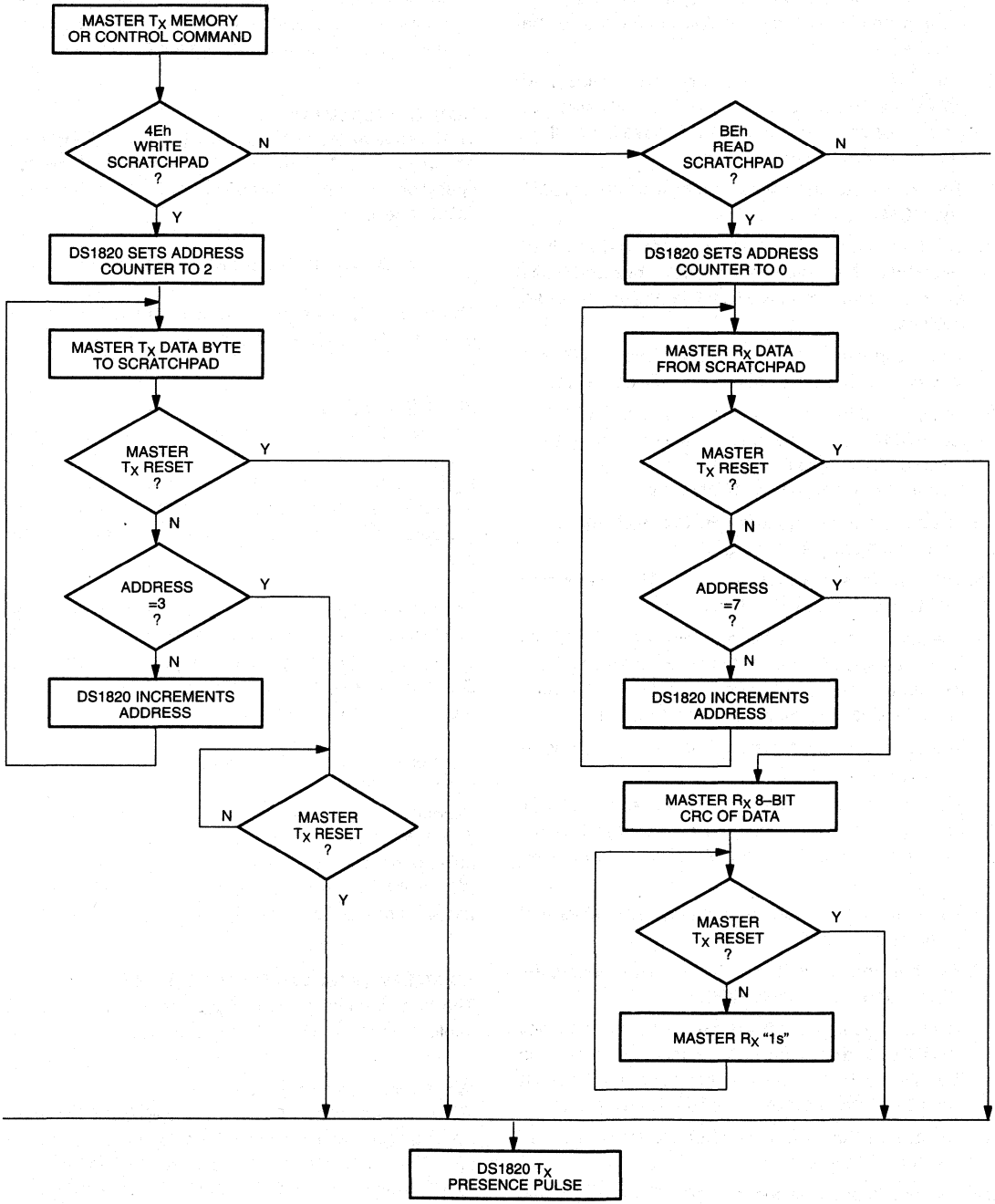
MEMORY COMMAND FUNCTIONS

The following command protocols are summarized in Table 2, and by the flowchart of Figure 10.

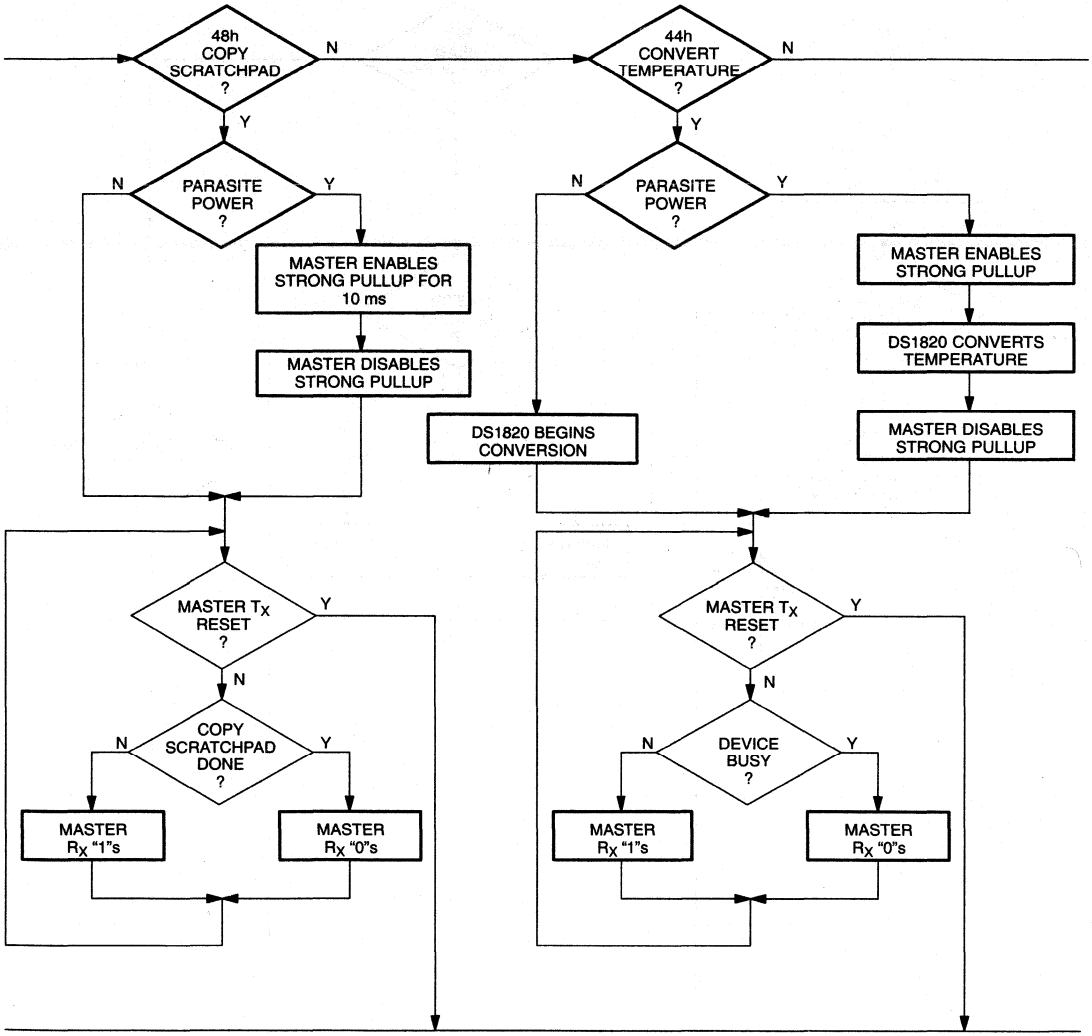
Write Scratchpad [4Eh]

This command writes to the scratchpad of the DS1820, starting at address 2. The next two bytes written will be saved in scratchpad memory, at address locations 2 and 3. Writing may be terminated at any point by issuing a reset.

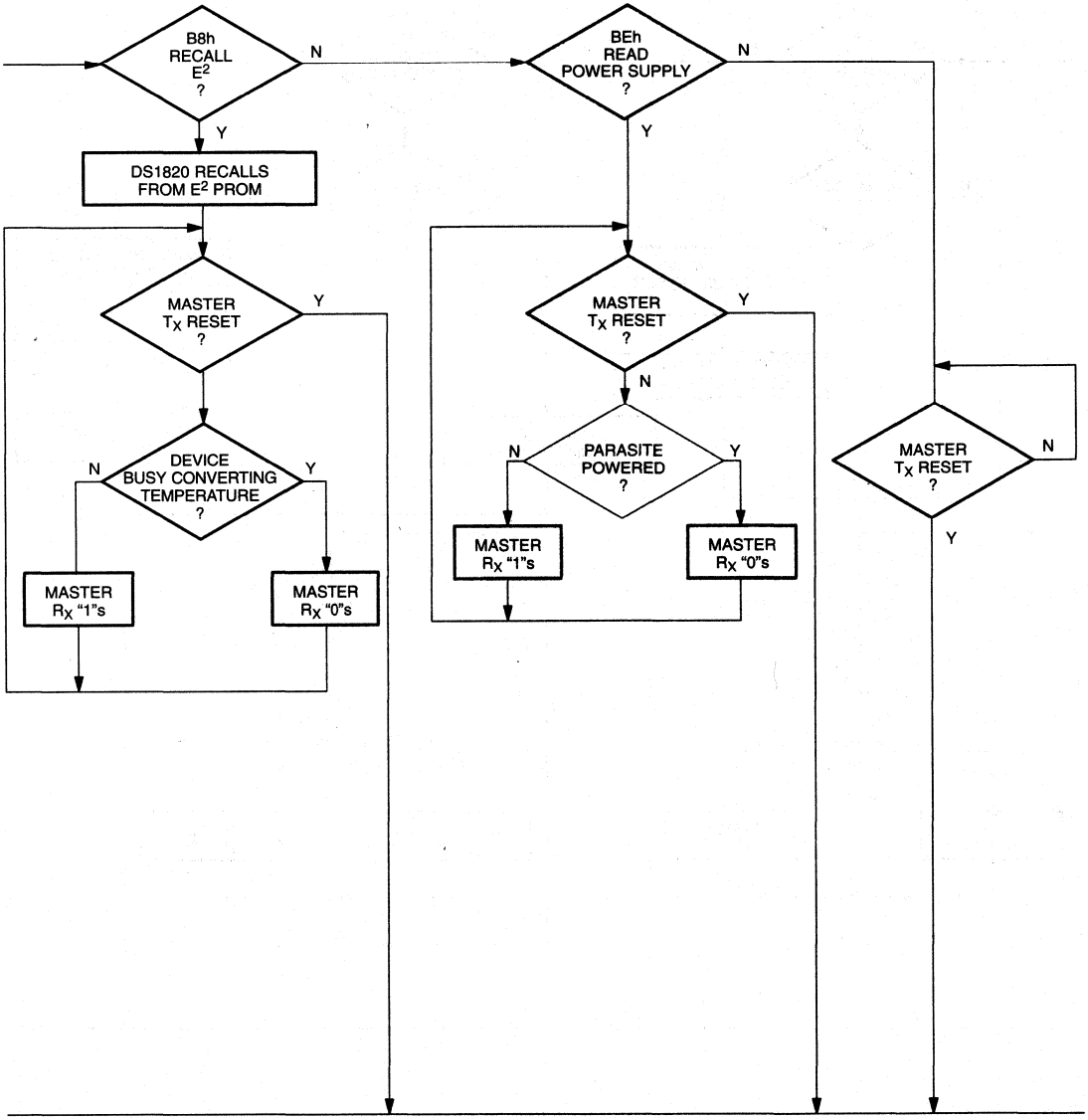
MEMORY FUNCTIONS FLOW CHART Figure 10



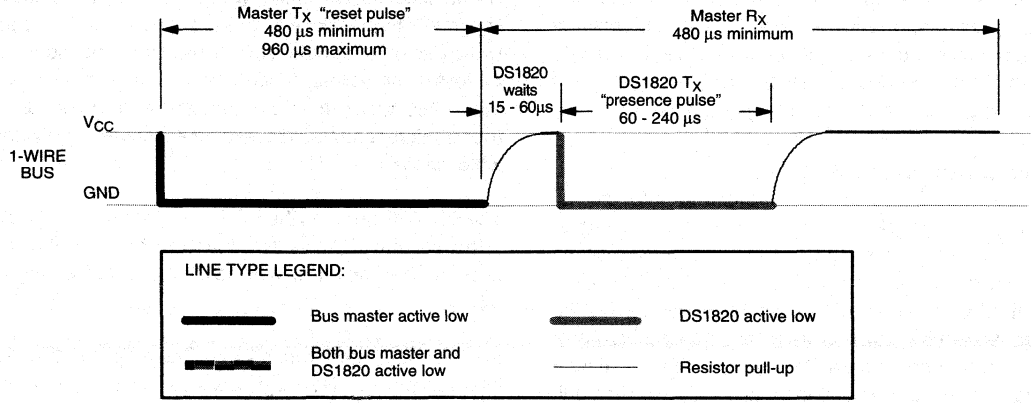
MEMORY FUNCTIONS FLOW CHART Figure 10 (cont'd)



MEMORY FUNCTIONS FLOW CHART Figure 10 (cont'd)



INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 11



DS1820 COMMAND SET Table 2

INSTRUCTION	DESCRIPTION	PROTOCOL	1–WIRE BUS AFTER ISSUING PROTOCOL	NOTES
TEMPERATURE CONVERSION COMMANDS				
Convert T	Initiates temperature conversion.	44h	<read temperature busy status>	1
MEMORY COMMANDS				
Read Scratchpad	Reads bytes from scratchpad and reads CRC byte.	BEh	<read data up to 9 bytes>	
Write Scratchpad	Writes bytes into scratchpad at addresses 2 and 3 (TH and TL temperature triggers).	4Eh	<write data into 2 bytes at addr. 2 and addr. 3>	
Copy Scratchpad	Copies scratchpad into nonvolatile memory (addresses 2 and 3 only).	48h	<read copy status>	2
Recall E^2	Recalls values stored in nonvolatile memory into scratchpad (temperature triggers).	B8h	<read temperature busy status>	
Read Power Supply	Signals the mode of DS1820 power supply to the master.	B4h	<read supply status>	

NOTE:

1. Temperature conversion takes up to 2 seconds. After receiving the Convert T protocol, if the part does not receive power from the V_{DD} pin, the I/O line for the DS1820 must be held high for at least 2 seconds to provide power during the conversion process. As such, no other activity may take place on the 1–Wire bus for at least this period after a Convert T command has been issued.
2. After receiving the Copy Scratchpad protocol, if the part does not receive power from the V_{DD} pin, the I/O line for the DS1820 must be held high for at least 10 ms to provide power during the copy process. As such, no other activity may take place on the 1–Wire bus for at least this period after a Copy Scratchpad command has been issued.

Read Scratchpad [BEh]
This command reads the contents of the scratchpad. Reading will commence at byte 0, and will continue through the scratchpad until the 9th (byte 8, CRC) byte is read. If not all locations are to be read, the master may issue a reset to terminate reading at any time.

Copy Scratchpad [48h]
This command copies the scratchpad into the E^2 memory of the DS1820, storing the temperature trigger bytes in nonvolatile memory. If the bus master issues read time slots following this command, the DS1820 will output "0" on the bus as long as it is busy copying the scratchpad to E^2; it will return a "1" when the copy process is complete. If parasite powered, the bus master has to enable a strong pullup for at least 10 ms immediately after issuing this command.

Convert T [44h]
This command begins a temperature conversion. No further data is required. The temperature conversion will be performed and then the DS1820 will remain idle. If the bus master issues read time slots following this command, the DS1820 will output "0" on the bus as long as it is busy making a temperature conversion; it will return a "1" when the temperature conversion is complete. If parasite powered, the bus master has to enable a strong pullup for 2 seconds immediately after issuing this command.

Recall E2 [B8h]
This command recalls the temperature trigger values stored in E^2 to the scratchpad. This recall operation happens automatically upon power–up to the DS1820 as well, so valid data is available in the scratchpad as soon as the device has power applied. With every read data time slot issued after this command has been sent, the device will output its busy flag "0"=busy, "1"=ready.

Read Power Supply [B4h]
With every read data time slot issued after this command has been sent to the DS1820, the device will signal its power mode: "0"=parasite power, "1"=external power supply provided.

READ/WRITE TIME SLOTS
DS1820 data is read and written through the use of time slots to manipulate bits and a command word to specify the transaction.

Write Time Slots
A write time slot is initiated when the host pulls the data line from a high logic level to a low logic level. There are two types of write time slots: Write One time slots and Write Zero time slots. All write time slots must be a minimum of 60 microseconds in duration with a minimum of a one microsecond recovery time between individual write cycles.

The DS1820 samples the I/O line in a window of 15 µs to 60 µs after the I/O line falls. If the line is high, a Write One occurs. If the line is low, a Write Zero occurs (see Figure 12).

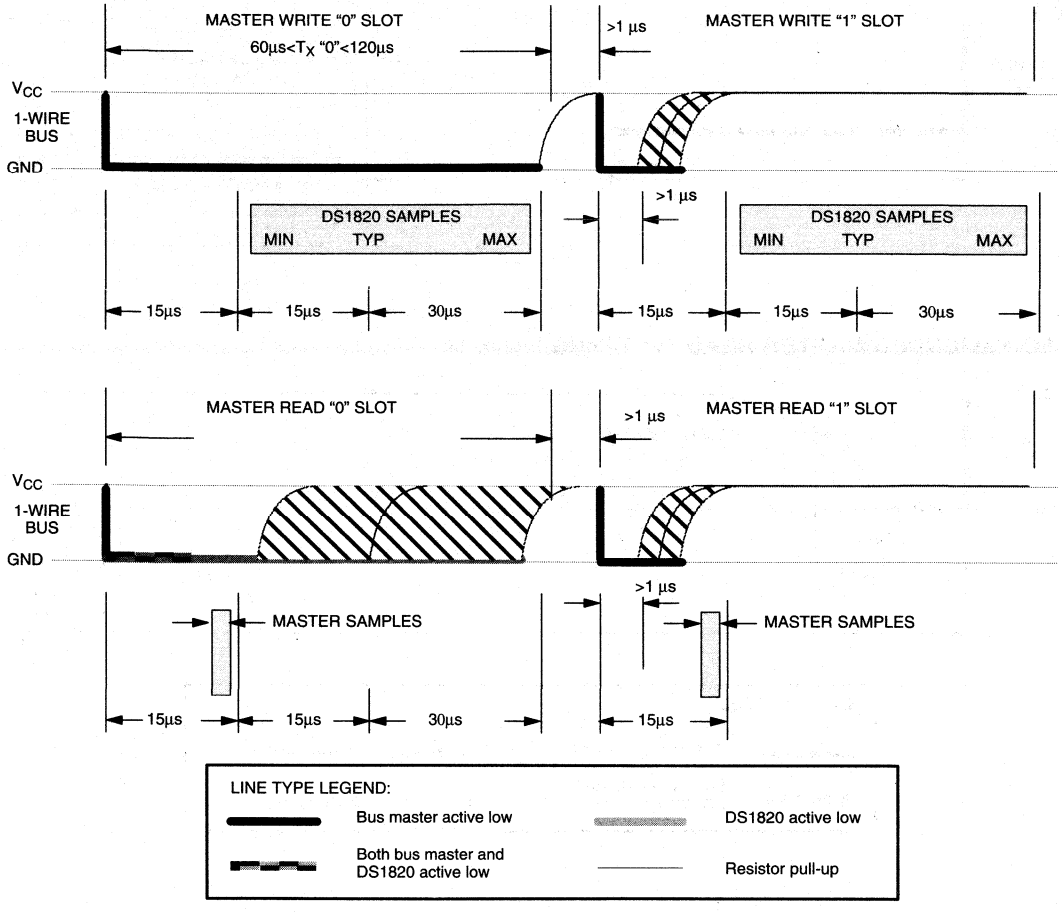
For the host to generate a Write One time slot, the data line must be pulled to a logic low level and then released, allowing the data line to pull up to a high level within 15 microseconds after the start of the write time slot.

For the host to generate a Write Zero time slot, the data line must be pulled to a logic low level and remain low for 60 µs.

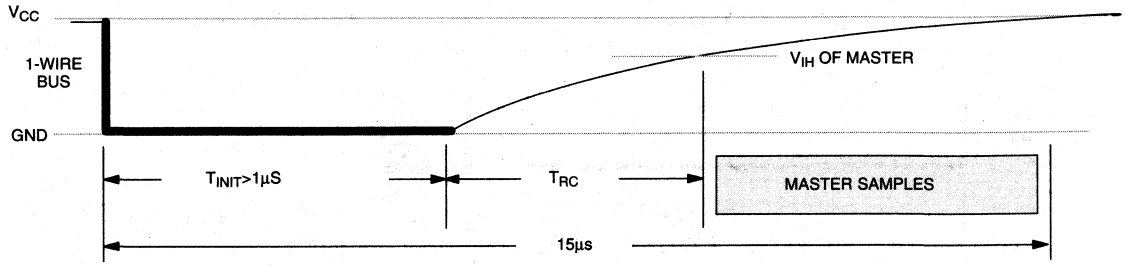
Read Time Slots
The host generates read time slots when data is to be read from the DS1820. A read time slot is initiated when the host pulls the data line from a logic high level to logic low level. The data line must remain at a low logic level for a minimum of one microsecond; output data from the DS1820 is valid for 15 microseconds after the falling edge of the read time slot. The host therefore must stop driving the I/O pin low in order to read its state 15 microseconds from the start of the read slot (see Figure 12). By the end of the read time slot, the I/O pin will pull back high via the external pull–up resistor. All read time slots must be a minimum of 60 microseconds in duration with a minimum of a one microsecond recovery time between individual read slots.

Figure 13 shows that the sum of T_{INIT}, T_{RC}, and T_{SAMPLE} must be less than 15 µs. Figure 14 shows that system timing margin is maximized by keeping T_{INIT} and T_{RC} as small as possible and by locating the master sample time towards the end of the 15 µs period.

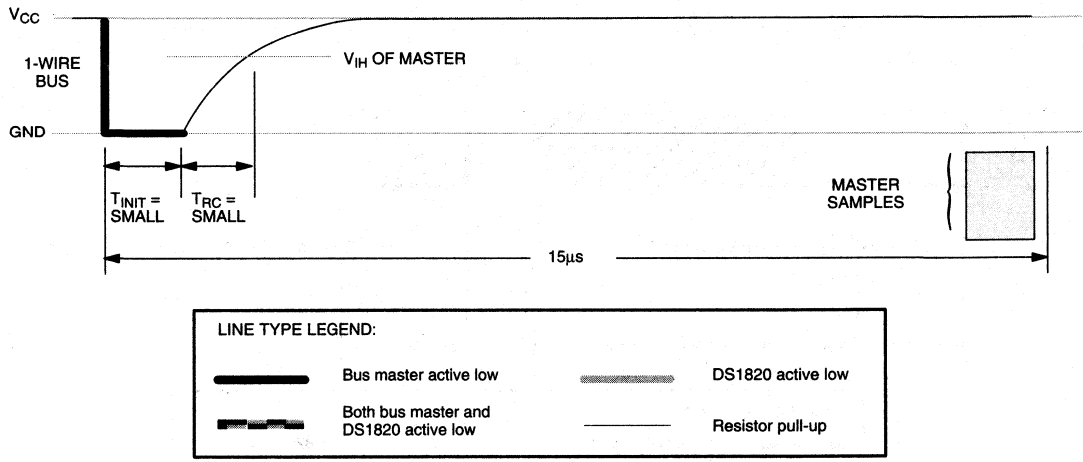
READ/WRITE TIMING DIAGRAM Figure 12



DETAILED MASTER READ "1" TIMING Figure 13



RECOMMENDED MASTER READ "1" TIMING Figure 14



MEMORY FUNCTION EXAMPLE Table 3

Example: Bus Master initiates temperature conversion, then reads temperature (parasite power assumed).

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse (480–960 µs)
RX	Presence	Presence pulse.
TX	55h	Issue "Match ROM" command.
RX	<64–bit ROM code>	Issue address for DS1820.
TX	EEh	Issue "Convert T" command.
TX	<I/O LINE HIGH>	I/O line is held high for at least 2 seconds by bus master to allow conversion to complete.
TX	Reset	Reset pulse.
RX	Presence	Presence pulse.
TX	55h	Issue "Match ROM" command.
TX	<64–bit ROM code>	Issue address for DS1820.
TX	BEh	Issue "Read Scratchpad" command.
RX	<9 data bytes>	Read entire scratchpad plus CRC; the master now recalculates the CRC of the eight data bytes received from the scratchpad, compares the CRC calculated and the CRC read. If they match, the master continues; if not, this read operation is repeated.
TX	Reset	Reset Pulse
RX	Presence	Presence pulse, done.

MEMORY FUNCTION EXAMPLE Table 4

Example: Bus Master writes memory (parasite power and only one DS1820 assumed).

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset pulse.
RX	Presence	Presence pulse.
TX	CCh	Skip ROM command.
TX	4Eh	Write Scratchpad command.
TX	<2 data bytes>	Writes two bytes to scratchpad (TH and TL).
TX	Reset	Reset pulse.
RX	Presence	Presence pulse.
TX	CCh	Skip ROM command.
TX	BEh	Read Scratchpad command.
RX	<9 data bytes>	Read entire scratchpad plus CRC. The master now recalculates the CRC of the eight data bytes received from the scratchpad, compares the CRC and the two other bytes read back from the scratchpad. If data match, the master continues; if not, repeat the sequence.
TX	Reset	Reset pulse.
RX	Presence	Presence pulse.
TX	CCh	Skip ROM command.
TX	48h	Copy Scratchpad command; after issuing this command, the master must wait 6 ms for copy operation to complete.
TX	Reset	Reset pulse.
RX	Presence	Presence pulse, done.

MEMORY FUNCTION EXAMPLE Table 5
Example: Temperature conversion and interpolation (external power supply and only one DS1820 assumed).

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	CCh	Skip ROM command.
TX	44h	Convert T command.
RX	<1 data byte>	Read busy flag eight times. The master continues reading one byte (or bit) after another until the data is FFh (all bits 1).
TX	Reset	Reset pulse.
RX	Presence	Presence pulse.
TX	CCh	Skip ROM command.
TX	BEh	Read Scratchpad command.
RX	<9 data bytes>	Read entire scratchpad plus CRC. The master now recalculates the CRC of the eight data bytes received from the scratchpad and compares both CRCs. If the CRCs match, the data is valid. The master saves the temperature value and stores the contents of the count register and count per °C register as COUNT_REMAIN and COUNT_PER_C, respectively
TX	Reset	Reset pulse.
RX	Presence	Presence pulse, done
–	–	CPU calculates temperature as described in the data sheet for higher resolution.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	I/O Functions	2.8	5.0	5.5		1, 2
		±1/2°C Accurate Temperature Conversions	4.3		5.5	V	
Data Pin	I/O		–0.5		5.5	V	2
Logic 1	V_{IH}		2.0		V_{CC}+0.3	V	2, 3
Logic 0	V_{IL}		–0.3		+0.8	V	2, 4

DC ELECTRICAL CHARACTERISTICS

(–55°C to +125°C; V_{DD}=3.6V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Thermometer Error	t_{ERR}	0°C to +70°C			±1/2	°C	
		–40°C to +0°C and +70°C to +85°C			±1	°C	
		–55°C to –40°C and +85°C to +125°C			±2	°C	
Input Logic High	V_{IH}		2.2		5.5	V	2, 3
Input Logic Low	V_{IL}		–0.3		+0.8	V	2, 4
Sink Current	I_L	$V_{I/O}$=0.4V	–4.0			mA	2
Standby Current	I_Q			100	150	nA	8
Active Current	I_{DD}			500	1000	µA	5, 6
Input Resistance	R_I			500		kΩ	7

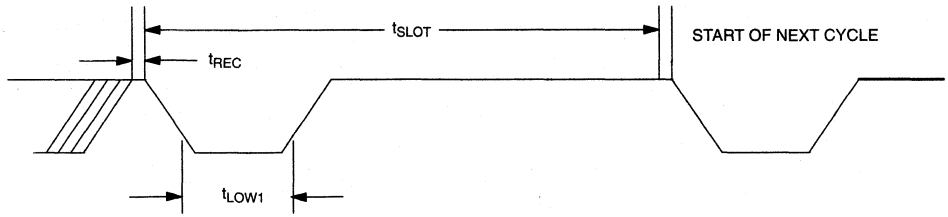
AC ELECTRICAL CHARACTERISTICS: 1–WIRE INTERFACE (–55°C to +125°C; V_{DD}=3.6V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Temperature Conversion Time	t_{CONV}		1.2	2	second	
Time Slot	t_{SLOT}	60		120	µs	
Recovery Time	t_{REC}	1			µs	
Write 0 Low Time	r_{LOW0}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Read Data Valid	t_{RDV}			15	µs	
Reset Time High	t_{RSTH}	480			µs	
Reset Time Low	t_{RSTL}	480		4800	µs	
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	
Capacitance	$C_{IN/OUT}$			25	pF	

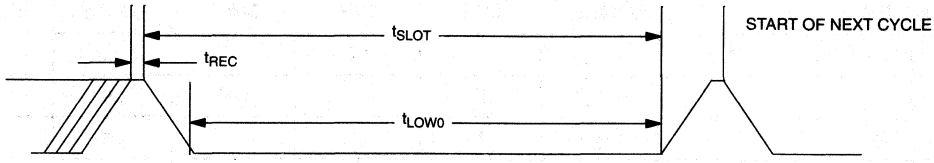
NOTES:

1. Temperature conversion will work with ±2°C accuracy down to V_{DD} = 3.4V.
2. All voltages are referenced to ground.
3. Logic one voltages are specified at a source current of 1 mA.
4. Logic zero voltages are specified at a sink current of 4 mA.
5. I_{DD} specified with V_{CC} at 5.0V
6. Active current refers to either temperature conversion of writing to the E^2 memory. Writing to E^2 memory consumes approximately 200 µA for up to 10 ms.
7. I/O line in "high–Z" state and $I_{I/O}$ = 0.
8. Standby current specified up to 70°C. Standby current may be up to 5 µA at 125°C.

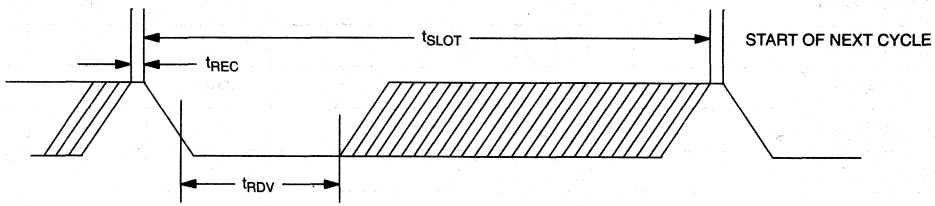
1–WIRE WRITE ONE TIME SLOT



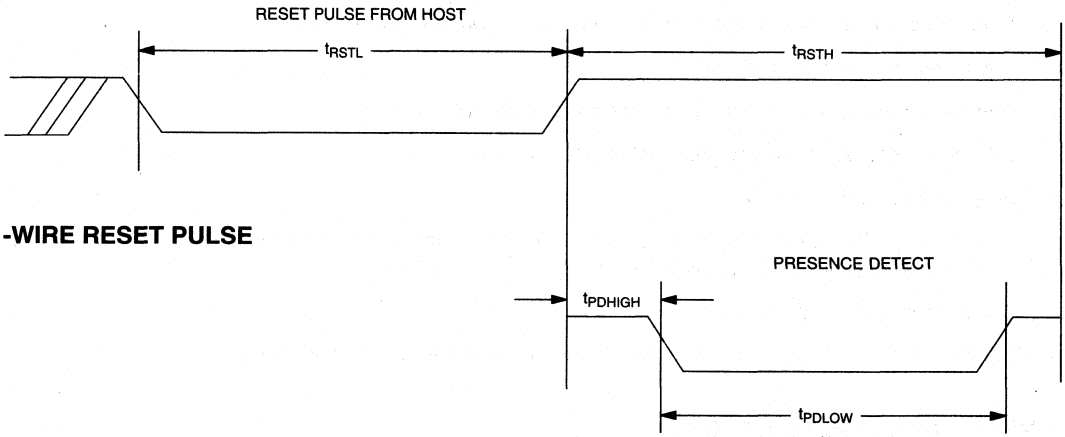
1–WIRE WRITE ZERO TIME SLOT



1-WIRE READ ZERO TIME SLOT



1-WIRE PRESENCE DETECT



1-WIRE RESET PULSE

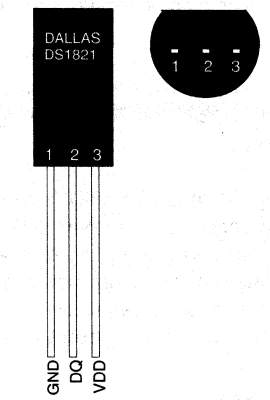
DALLAS SEMICONDUCTOR

DS1821
Programmable Digital Thermostat

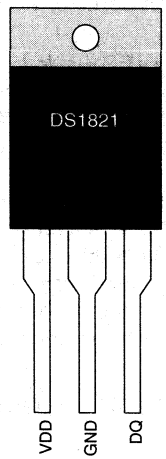
FEATURES

- Requires no external components
- Measures temperatures from –55°C to +125°C in 1°C increments, Fahrenheit equivalent is –67°F to 257°F in 1.8°F increments
- Converts temperature to digital word in 1 second
- Thermostatic settings are user definable and nonvolatile
- Available in 3–pin PR35, TO–220, and 8–pin SOIC packages
- Applications include thermostatic controls, industrial systems, consumer products, thermometers, or any thermally sensitive system

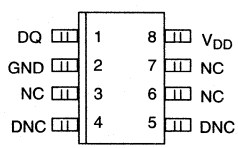
PIN ASSIGNMENT



DS1821
PR–35 PACKAGE



DS1821T
TO–220 PACKAGE
See Mech. Drawing
Pg. 488



DS1821S
8–PIN SOIC (200 MIL)
See Mech. Drawing
Pg. 483

PIN DESCRIPTION

GND	–	Ground
DQ	–	Data In/Out, Thermostat
V_{DD}	–	Power Supply Voltage +5V
NC	–	No Connect
DNC	–	Do Not Connect

DESCRIPTION

The DS1821 Programmable Digital Thermostat provides a thermal alarm logic output when the temperature of the device exceeds a user–defined temperature TH. The output remains active until the temperature drops below user defined temperature TL, allowing for any hysteresis necessary.

User–defined temperature settings are stored in non–volatile memory, so parts can be programmed prior to insertion in a system. Communication to/from the DS1821 is accomplished through the DQ pin in a programming mode; this same pin is used in operation as the thermostat output.

DETAILED PIN DESCRIPTION

PIN PR35	PIN TO–220	PIN 8–PIN SOIC	SYMBOL	DESCRIPTION
1	2/TAB	2	GND	**Ground.**
2	3	1	DQ	**Data input/output pin** for one–wire programming mode. **Thermostat output pin** in operation mode.
3	1	8	V_{DD}	**V_{DD}** pin. See "Parasite Power" section for details of connection.

DS1821S (8–pin SOIC): All pins not specified in this table are not to be connected.

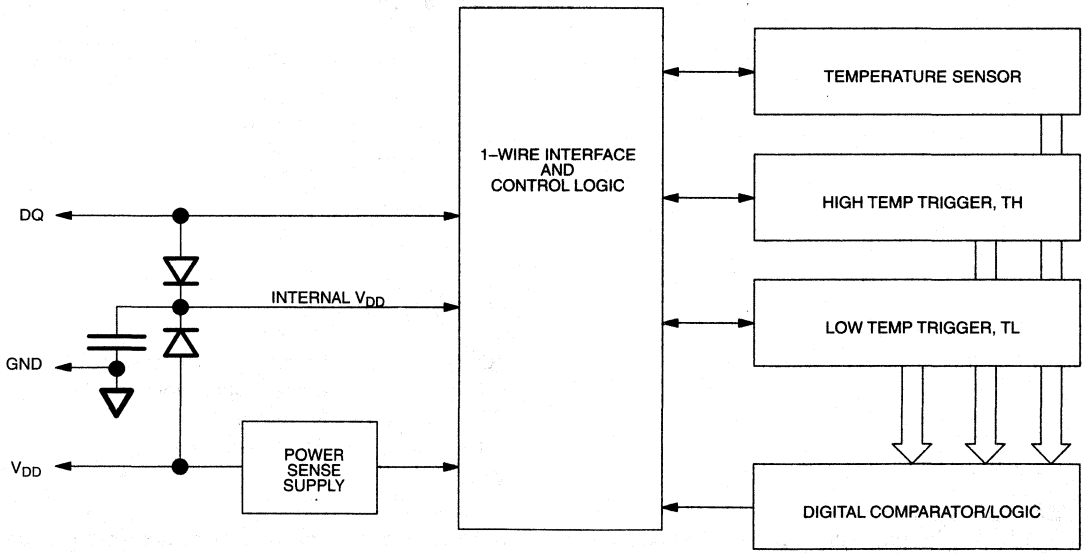
OVERVIEW

The block diagram of Figure 1 shows the major components of the DS1821. The DS1821 has two operating modes: program and operation.

In program mode, the V_{DD} pin of the DS1821 is connected to ground. The part derives power from the DQ pin, which would be connected to a microprocessor. The microprocessor will write data into the high and low temperature trigger registers, TH and TL, respectively, to set up the temperature limits for thermostat operation. In this mode, the result of the last temperature measurement made by the DS1821 may also be read directly by the microprocessor.

In normal operating mode, the V_{DD} line is connected to +5V, and the DQ line becomes the thermostat output. This output will go to its active state (programmable high/low) when the temperature of the DS1821 goes above the limit set in the TH register, and will remain active until the temperature goes below the limit programmed into the TL register.

DS1821 BLOCK DIAGRAM Figure 1



OPERATION–TEMPERATURE MEASUREMENT

The DS1821 measures temperatures through the use of an on–board proprietary temperature measurement technique. The temperature reading is provided in an 8–bit, two's complement reading. Table 1 describes the exact relationship of output data to measured temperature. The data is transmitted serially over the 1–wire interface. The DS1821 can measure temperature over the range of –55°C to +125°C in 1°C increments. For Fahrenheit usage, a lookup table or conversion factor must be used.

TEMPERATURE/DATA RELATIONSHIPS Table 1

TEMPERATURE	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
+125°C	01111101	7Dh
+25°C	00011001	19h
0°C	00000000	00h
–1°C	11111111	FFh
–25°C	11100111	E7h
–55°C	11001001	C9h

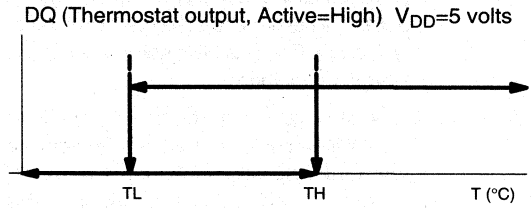
OPERATION–THERMOSTAT CONTROLS

In its operating mode, the DS1821 functions as a thermostat with programmable hysteresis, as shown in Figure 2. Temperature conversions begin as soon as V_{DD} is applied to the device, and are continually made, so that the thermostat output updates as soon as a temperature conversion is complete. This is approximately once every second.

When the DS1821's temperature meets or exceeds the value stored in the high temperature trip register (TH), the output becomes active, and will stay active until the temperature falls below the temperature stored in the low temperature trigger register (TL). In this way, any amount of hysteresis may be obtained.

The active state for the output is programmable by the user, so that an active state may either be a logic 1 (+5V) or a logic 0 (0V).

THERMOSTAT OUTPUT OPERATION Figure 2



PROGRAMMING THE DS1821

To program the DS1821, it must be placed in program mode. This mode is active when the V_{DD} pin is tied to ground. Power to the device is then supplied by the DQ pin through the use of "parasite power". The block diagram (Figure 1) shows the parasite–powered circuitry. This circuitry "steals" power whenever the DQ pin is high and V_{DD} is low. DQ will provide sufficient power as long as the specified timing and voltage requirements are met.

The DS1821 has four internal registers that may be accessed through the DQ pin when the device is in program mode. These registers are the high temperature trigger (TH), low temperature trigger (TL), the actual measured temperature result, and the status register. The TH, TL, and status registers are all nonvolatile.

The DS1821 must have temperature settings resident in the TH and TL registers for thermostatic operation. The temperature result register and the thermostat limit registers (TH and TL) hold an eight bit number in the two's complement format described in Table 1.

A status register is also present, indicating the status of the thermostatic control, and allowing configuration of the output polarity as either active high or active low.

The status register is defined as follows:

STATUS REGISTER

X	X	X	X	X	THF	THL	POL

where

X = Don't Care

THF= Temperature High Flag. This bit will normally be "0", but will be set to "1" when the temperature exceeds the value of TH. It will remain "1"

until reset by writing 0 into this location. This feature provides a method of determining if the DS1821 has ever been subjected to temperatures above TH. This bit is nonvolatile, and is stored in E^2 memory.

TLF= Temperature Low Flag. This bit will normally be "0", but will be set to "1" when the temperature is lower than the value of TL. It will remain "1" until reset by writing 0 into this location. This feature provides a method of determining if the DS1821 has ever been subjected to temperatures below TL. This bit is nonvolatile, and is stored in E^2 memory.

POL= Output Polarity Bit. "1" = active high, "0" = active low. This bit is nonvolatile, and is stored in E^2 memory.

PROGRAMMING COMMAND FUNCTIONS

The command set for the DS1821 as shown in Table 2 is as follows:

Read Temperature [AAh]

This command reads the contents of the register which contains the last temperature conversion result.

Write TH [01h]

This command writes to the TH (HIGH TEMPERATURE) register. After issuing this command, the user writes eight bits of data to the TH register.

Write TL [02h]

This command writes to the TL (LOW TEMPERATURE) register. After issuing this command, the user writes eight bits of data to the TL register.

Read TH [A1h]

This command reads the value of the TH (HIGH TEMPERATURE) register. After issuing this command, the user reads the eight bits of data present in the TH register.

Read TL [A2h]

This command reads the value of the TL (LOW TEMPERATURE) register. After issuing this command, the user reads the eight bits of data present in the TL register.

Write Status [0Ch]

This command writes to the status register. This would be used for clearing the values of the THF and TLF flags or for setting the POL bit. After issuing this command, the user writes the eight bit data into the register.

Read Status [ACh]

This command reads the value in the status register. After issuing this command, the user reads the eight bits present in the status register.

DS1821 COMMAND SET Table 2

INSTRUCTION	DESCRIPTION	PROTOCOL	1–WIRE BUS DATA AFTER ISSUING PROTOCOL
TEMPERATURE CONVERSION COMMANDS			
Read Temperature	Reads last converted temperature value from temperature register.	AAh	<read data>
THERMOSTAT COMMANDS			
Write TH	Writes high temperature limit value into TH register.	01h	<write data>
Write TL	Writes low temperature limit value into TL register.	02h	<write data>
Read TH	Reads stored value of high temperature limit from TH register.	A1h	<read data>
Read TL	Reads stored value of low temperature limit from TL register.	A2h	<read data>
Write Status	Writes configuration data to configuration register.	0Ch	<write data>
Read Status	Reads configuration data from configuration register.	ACh	<read data>

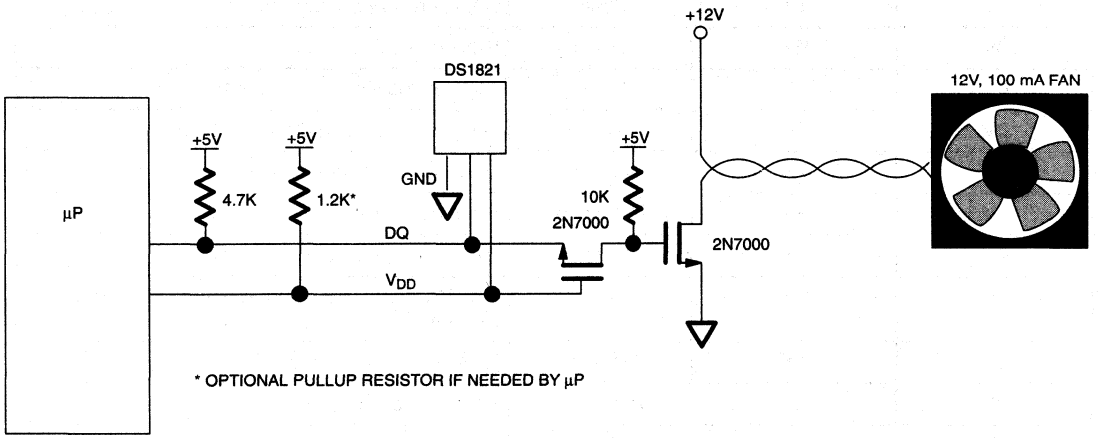
APPLICATION EXAMPLE

The application circuit shown in Figure 3 shows how a DS1821 could be used with a microprocessor in a system where it is desirable to reprogram the trigger points in the system, or where the temperature reading may need to be taken occasionally. Using only two port pins on a microprocessor, the DS1821 provides a simple application solution to monitoring the internal temperature for a piece of equipment, and then turning on a fan when the temperature rises too high.

One port pin of the microprocessor is used as the DQ data line. This line is pulled up by a 4.7K resistor, as required for the one–wire interface. The other port pin supplies power to the DS1821. In some microprocessors, this is an actual output; provided that it can source 1mA, no pullup resistor is needed in this case. If the port pin is an open drain output, however, a pullup resistor will be required, and this must be sized so as to allow t he DS1821 to pull 1mA of current though it and still provide adequate supply voltage to the DS1821.

The part is placed in programming mode by pulling the V_{DD} port pin low, and communicating to the DS1821 over the DQ line. When the programming operation is complete, the V_{DD} port pin is brought high, and the fan now operates when the DS1821 pulls the DQ line high (output is programmed so that active= logic high).

APPLICATION EXAMPLE CIRCUIT Figure 3



Example: CPU sets up DS1821 for low temp limit of +10°C and high temp limit of +40°C, output active high.

V_{DD} PORT PIN	DQ PORT PIN	DATA (LSB FIRST)	COMMENTS
0V	TX	Reset	Reset pulse (480–960 µs).
0V	RX	Presence	Presence pulse.
0V	TX	0Ch	CPU issues Write Config command.
0V	TX	01h	CPU sets DS1821 up for active high output.
0V	TX	Reset	Reset pulse (480–960 µs).
0V	RX	Presence	Presence pulse.
0V	TX	01h	CPU issues Write TH command.
0V	TX	28h	CPU sends data for TH limit of +40°C.
0V	TX	Reset	Reset pulse (480–960 µs).
0V	RX	Presence	Presence pulse.
0V	TX	02h	CPU issues Write TL command.
0V	TX	0Ah	CPU sends data for TL limit of +10°C.
0V	TX	Reset	Reset pulse (480–960 µs).
0V	RX	Presence	Presence pulse.
0V	TX	A1h	CPU issues Read TH command.
0V	RX	28h	DS1821 sends back stored value of TL for CPU to verify.
0V	TX	Reset	Reset pulse (480–960 µs).
0V	RX	Presence	Presence pulse.
0V	TX	A2h	CPU issues Read TL command.
0V	RX	0Ah	DS1821 sends back stored value of TL for CPU to verify.
0V	TX	Reset	Reset pulse (480–960 µs).
0V	RX	Presence	Presence pulse.
0V	TX	ACh	CPU issues Read Status command.
0V	RX	01h	DS1821 sends back contents of status register for CPU to verify.
5V	<high impedance>		CPU raises V_{DD}, DS1821 now in operation mode.

1–WIRE BUS SYSTEM

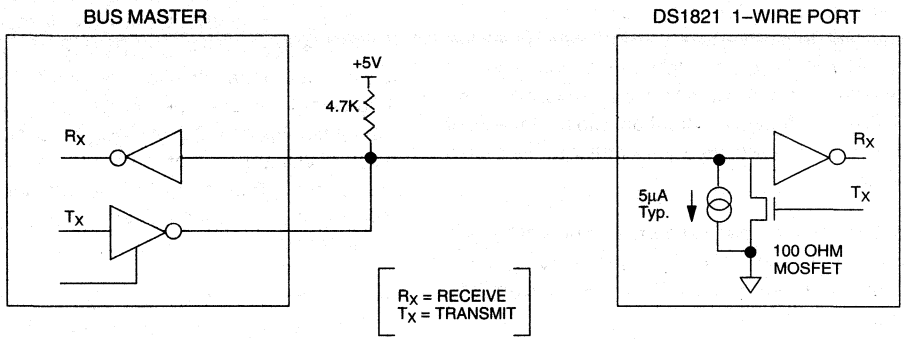
The DS1821 1–wire bus is a system which has a single bus master and one slave. The DS1821 behaves as a slave. The DS1821 is not able to be multidropped, unlike other 1–wire devices from Dallas Semiconductor.

The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1–wire signalling (signal types and timing).

HARDWARE CONFIGURATION

The 1–wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1–wire bus must have open drain or tri–state outputs. The 1–wire port of the DS1821 (DQ pin) is open drain with an internal circuit equivalent to that shown in Figure 4. The 1–wire bus requires a pullup resistor of approximately 5KΩ.

HARDWARE CONFIGURATION Figure 4



The idle state for the 1–wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 480 µs, all components on the bus will be reset.

TRANSACTION SEQUENCE

The protocol for accessing the DS1821 via the 1–wire port is as follows:

- Initialization
- Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1–wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS1821 is on the bus and is ready to operate. For more details, see the "1–Wire Signalling" section.

1–WIRE SIGNALLING

The DS1821 requires strict protocols to insure data integrity. The protocol consists of several types of signaling on one line: reset pulse, presence pulse, write 0, write 1, read 0, and read 1. All of these signals, with the exception of the presence pulse, are initiated by the bus master.

The initialization sequence required to begin any communication with the DS1821 is shown in Figure 5. A reset pulse followed by a presence pulse indicates the DS1821 is ready to send or receive data given the correct function command.

The bus master transmits (TX) a reset pulse (a low signal for a minimum of 480 µs). The bus master then

releases the line and goes into a receive mode (RX). The 1–wire bus is pulled to a high state via the 5K pull–up resistor . After detecting the rising edge on the DQ pin, the DS1821 waits 15–60 µs and then transmits the presence pulse (a low signal for 60–240 µs).

READ/WRITE TIME SLOTS

DS1821 data is read and written through the use of time slots to manipulate bits and a command word to specify the transaction.

Write Time Slots

A write time slot is initiated when the host pulls the data line from a high logic level to a low logic level. There are two types of write time slots: Write One time slots and Write Zero time slots. All write time slots must be a minimum of 60 microseconds in duration with a minimum of a one microsecond recovery time between individual write cycles.

The DS1821 samples the DQ line in a window of 15 µs to 60 µs after the DQ line falls. If the line is high, a Write One occurs. If the line is low, a Write Zero occurs (See Figure 6).

For the host to generate a Write One time slot, the data line must be pulled to a logic low level and then released, allowing the data line to pull up to a high level within 15 microseconds after the start of the write time slot.

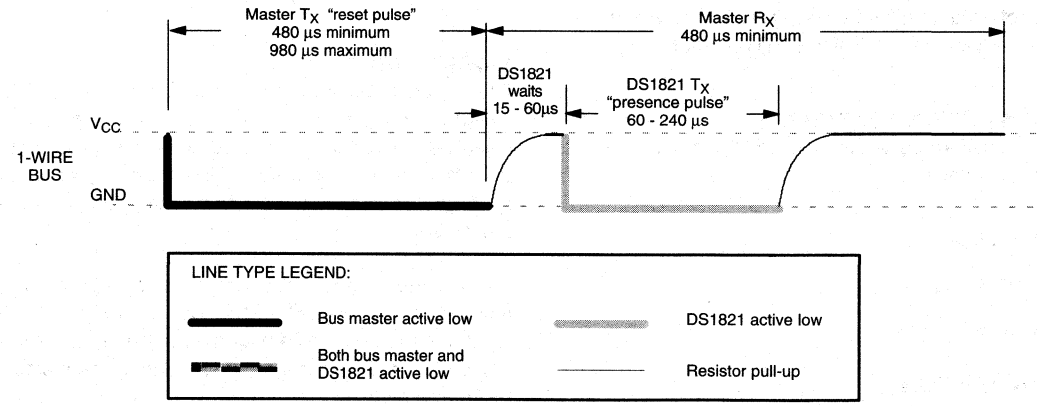
For the host to generate a Write Zero time slot, the data line must be pulled to a logic low level and remain low for the duration of the write time slot.

Read Time Slots

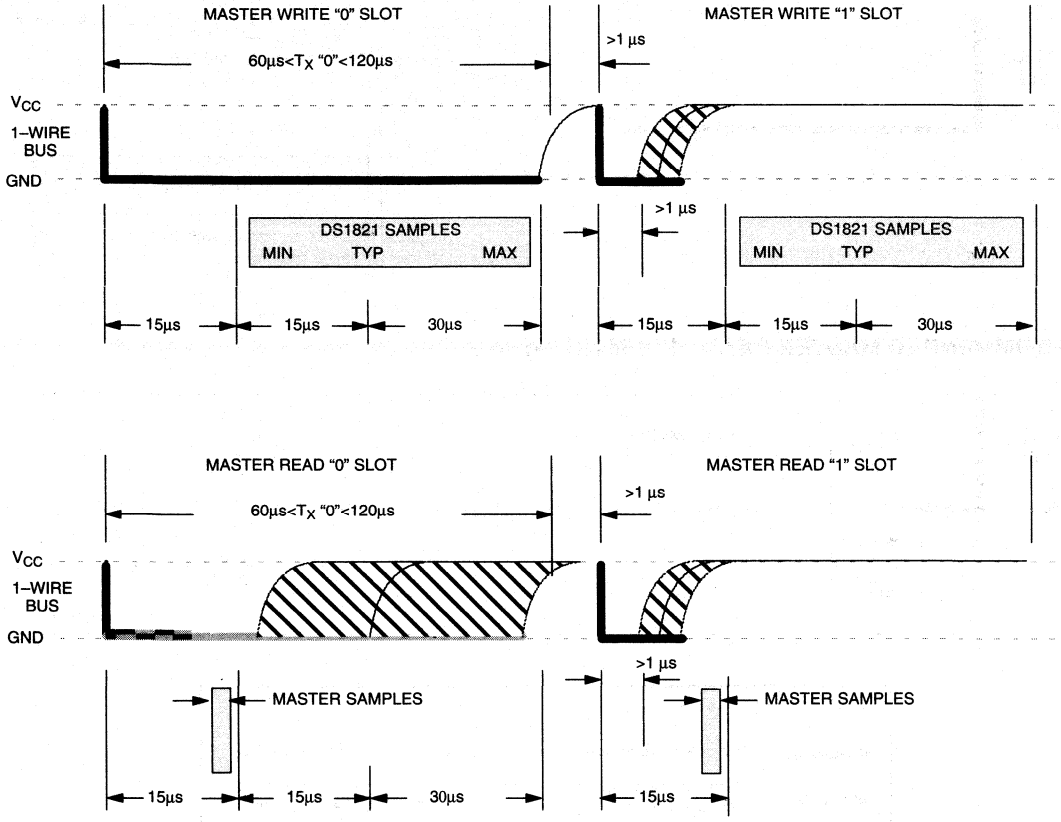
The host generates read time slots when data is to be read from the DS1821. A read time slot is initiated when the host pulls the data line from a logic high level to logic low level. The data line must remain at a low logic level for a minimum of one microsecond; output data from the DS1821 is then valid for the next 14 microseconds maximum. The host therefore must stop driving the DQ pin low in order to read its state 15 microseconds from the start of the read slot. (See Figure 6.) By the end of the read time slot, the DQ pin will pull back high via the external pull–up resistor. All read time slots must be a minimum of 60 microseconds in duration with a minimum of a one microsecond recovery time between individual read slots.

Figure 7 shows that the sum of T_{INIT}, T_{RC}, and T_{SAMPLE} must be less than 15 µs. Figure 8 shows that system timing margin is maximized by keeping T_{INIT} and T_{RC} as small as possible and by locating the master sample time toward s the end of the 15 µs period.

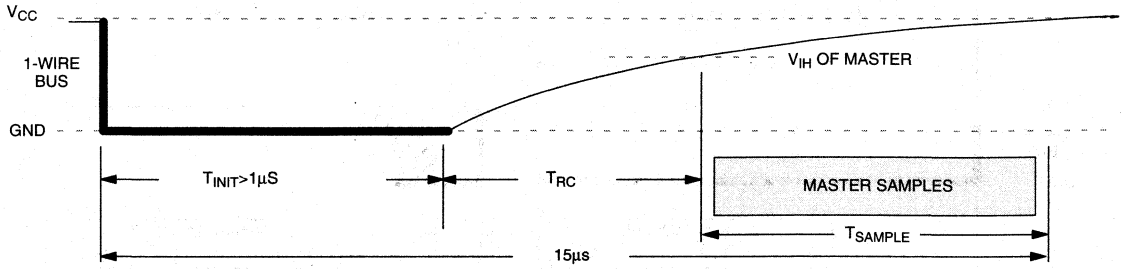
INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 5



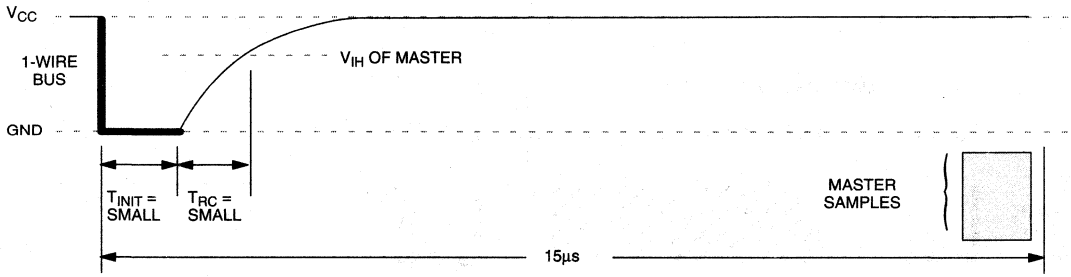
READ/WRITE TIMING DIAGRAM Figure 6

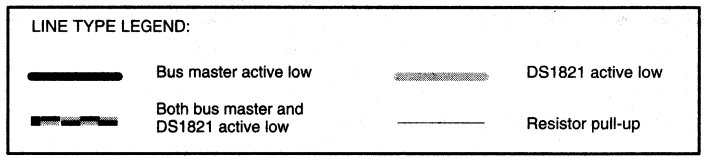


DETAILED MASTER READ "1" TIMING Figure 7



RECOMMENDED MASTER READ "1" TIMING Figure 8





ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	I/O Functions	2.5	5.0	5.5	V	1, 2
		±1°C Accurate Temp. Conversions	4.3		5.5	V	
Data Pin	DQ		–0.5		5.5	V	2
Logic 1	V_{IH}		2.0		V_{CC}+0.3	V	2, 3
Logic 0	V_{IL}		–0.3		+0.8	V	2, 4

DC ELECTRICAL CHARACTERISTICS

(–55°C to +125°C; V_{DD}=3.6V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Thermometer Error	T_{ERR}	–40°C to +85°C				°C	
		–55°C to –40°C and +85°C to +125°C				°C	
Output Logic High	V_{OH}		2.2			V	2, 3
Output Logic Low	V_{OL}		–0.3		0.8	V	2, 4
Sink Current	I_L	V_{DQ}=0.4V			–4.0	mA	2
Source Current	I_H	V_{DQ}=2.2V	1			mA	
Standby Current	I_Q			100	150	nA	9
Active Current	I_{DD}	Temperature Conversions, Programming		500	1000	µA	5
Input Resistance	R_I			500		KΩ	6

AC ELECTRICAL CHARACTERISTICS: 1–WIRE INTERFACE

(–55°C to +125°C; V_{DD}=3.6V to 5.5V)

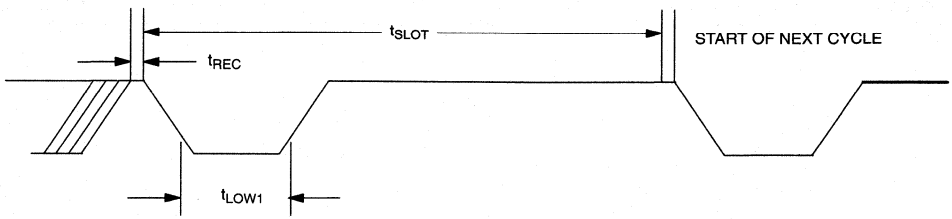
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Temperature Conversion Time	t_{CONV}		1.2	2	s	
Time Slot	t_{SLOT}	60		120	µs	
Recovery Time	t_{REC}	1			µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Read Data Valid	t_{RDV}			15	µs	
Reset Time High	t_{RSTH}	480			µs	
Reset Time Low	t_{RSTL}	480		4800	µs	
Presence Detect High	t_{PDHIGH}	15		60	µs	
Presence Detect Low	t_{PDLOW}	60		240	µs	
V_{DD} Active to DQ High Z	t_{DZ}		250	1000	ns	7
DQ High to Reset After V_{DD} Inactive	t_{DQR}	1			µs	
Time from Prog. End to Operate mode (V_{DD}=0)	t_{PE}		10	50	ms	8
Capacitance	$C_{IN/OUT}$			25	pF	

NOTES:

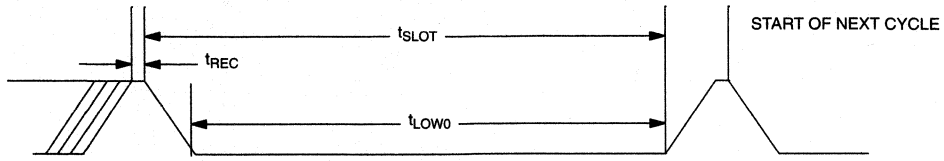
1. Temperature conversion will work with ±2°C accuracy down to V_{DD} = 3.4V.
2. All voltages are referenced to ground.
3. Logic one voltages are specified at a source current of 1 mA.
4. Logic zero voltages are specified at a sink current of 4 mA.
5. I_{DD} specified with V_{CC} at 5.0V
6. DQ line in "hi–Z" state and I_{DQ}=0.
7. Time for part to disable thermostat output.
8. Time to insure completion of E^2 write.
9. Standby current specified up to 70°C. Standby current may be up to 5 µA at 125°C.

TIMING DIAGRAMS

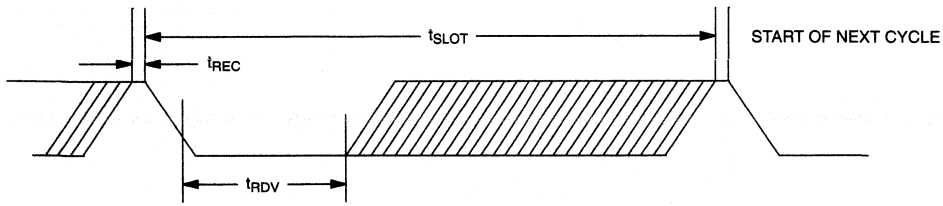
1–WIRE WRITE ONE TIME SLOT



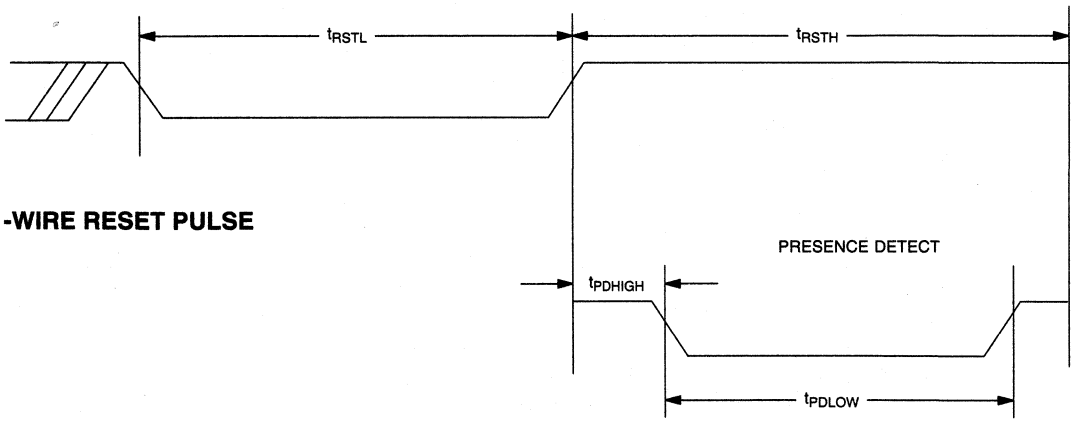
1–WIRE WRITE ZERO TIME SLOT



1-WIRE READ ZERO TIME SLOT

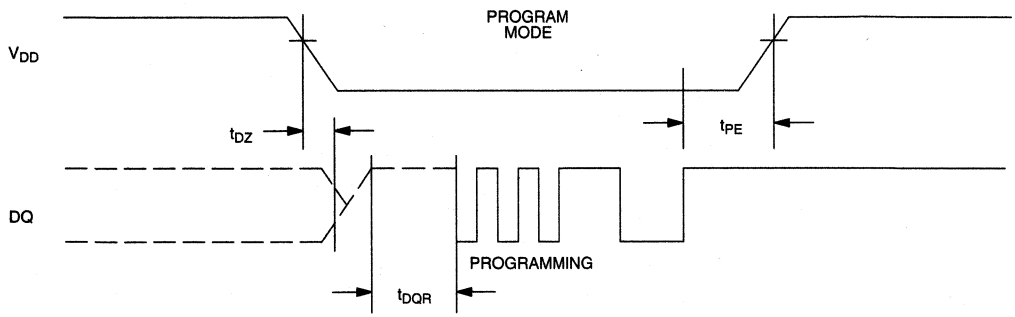


1-WIRE PRESENCE DETECT



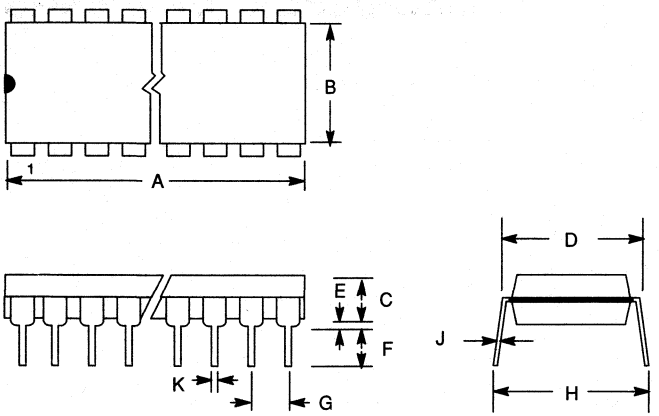
1-WIRE RESET PULSE

PROGRAM MODE TIMING



MECHANICAL DRAWINGS

8– TO 28–PIN DIP (300 MIL)



Includes:

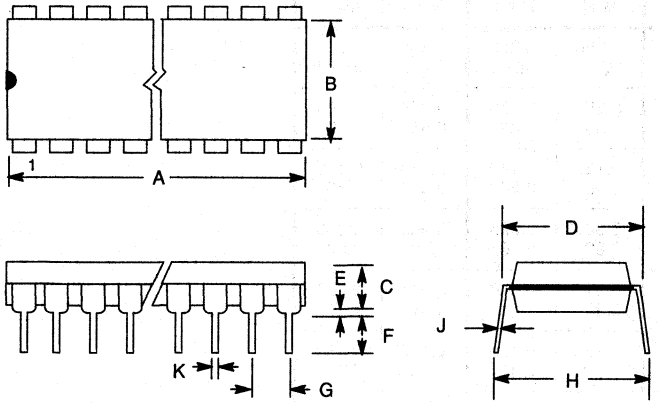
DS1000	DS1211	DS1632
DS1000M	DS1215	DS1640
DS1003	DS1221	DS1651
DS1003M	DS1222	DS1652
DS1004M	DS1228	DS1652B
DS1005	DS1229	DS1653
DS1005M	DS1231	DS1666
DS1007	DS1232	DS1667
DS1010	DS1232LP	DS1669
DS1012M	DS1234	DS1802
DS1013	DS1236	DS1830
DS1013M	DS1237	DS1867
DS1020	DS1238	DS1868
DS1033M	DS1239	DS1869
DS1035M	DS1259	DS2009D
DS1040M	DS1267	DS2010D
DS1044	DS1275	DS2011D
DS1045	DS1291	DS2013D
DS1200	DS1293	
DS1206	DS1336	
DS1210	DS1620	

PKG	8-PIN		10-PIN		14-PIN		16-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	0.360	0.400	0.480	0.520	0.740	0.780	0.740	0.780
MM	9.14	10.16	12.19	13.21	18.80	19.81	18.80	19.81
B IN.	0.240	0.260	0.240	0.260	0.240	0.260	0.240	0.260
MM	6.10	6.60	6.10	6.60	6.10	6.60	6.10	6.60
C IN.	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140
MM	3.05	3.56	3.05	3.56	3.05	3.56	3.05	3.56
D IN.	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325
MM	7.62	8.26	7.62	8.26	7.62	8.26	7.62	8.26
E IN.	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040
MM	0.38	1.02	0.38	1.02	0.38	1.02	0.38	1.02
F IN.	0.120	0.140	0.110	0.130	0.120	0.140	0.120	0.140
MM	3.04	3.56	2.79	3.30	3.O4	3.56	3.04	3.56
G IN.	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
MM	2.29	2.79	2.29	2.79	2.29	2.79	2.29	2.79
H IN	0.320	0.370	0.320	0.370	0.320	0.370	0.320	0.370
MM	8.13	9.40	8.13	9.40	8.13	9.40	8.13	9.40
J IN	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
MM	0.20	0.30	0.20	0.30	0.20	0.30	0.20	0.30
K IN.	0.015	0.021	0.015	0.021	0.015	0.021	0.015	0.021
MM	0.38	0.53	0.38	0.53	0.38	0.53	0.38	0.53

Continued on following page.

PKG	18-PIN		20-PIN		24-PIN		28-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	0.890	0.920	0.970	1.040	1.150	1.260	1.345	1.370
MM	22.61	23.36	24.63	26.42	29.21	32.00	34.16	34.80
B IN.	0.240	0.260	0.240	0.270	0.250	0.270	0.270	0.295
MM	6.10	6.60	6.09	6.86	6.35	6.86	6.85	7.49
C IN.	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140
MM	3.05	3.56	3.05	3.56	3.05	3.56	3.05	3.56
D IN.	0.300	0.325	0.295	0.325	0.300	0.325	0.300	0.325
MM	7.62	8.26	7.49	8.26	7.62	8.26	7.62	8.26
E IN.	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.050
MM	0.38	1.02	0.38	1.02	0.38	1.02	0.38	1.27
F IN.	0.120	0.140	0.120	0.140	0.125	0.135	0.125	0.135
MM	3.04	3.56	3.04	3.56	3.18	3.48	3.18	3.48
G IN.	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
MM	2.23	2.79	2.23	2.79	2.23	2.79	2.23	2.79
H IN	0.320	0.370	0.310	0.390	0.320	0.370	0.320	0.370
MM	8.13	9.40	7.87	9.91	8.13	9.40	8.13	9.40
J IN	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
MM	0.20	0.30	0.20	0.30	0.20	0.30	0.20	0.30
K IN.	0.015	0.021	0.015	0.021	0.015	0.022	0.015	0.022
MM	0.38	0.53	0.38	0.53	0.38	0.56	0.38	0.56

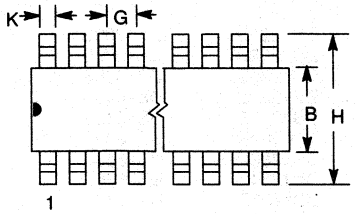
24– TO 40–PIN DIP (600 MIL)

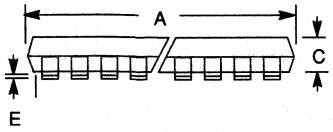


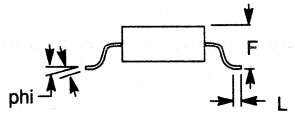
Includes:
DS1212
DS1609
DS2009
DS2010
DS2011
DS2012
DS2013

PKG	24-PIN		28-PIN		40-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	1.245	1.270	1.445	1.470	2.050	2.075
MM	31.62	32.25	36.70	37.34	52.07	52.71
B IN.	0.530	0.550	0.530	0.550	0.530	0.550
MM	13.46	13.97	13.46	13.97	13.46	13.97
C IN.	0.140	0.160	0.140	0.160	0.140	0.160
MM	3.56	4.06	3.56	4.06	3.56	4.06
D IN.	0.600	0.625	0.600	0.625	0.600	0.625
MM	15.24	15.88	15.24	15.88	15.24	15.88
E IN.	0.015	0.050	0.015	0.040	0.015	0.040
MM	0.380	1.27	0.380	1.02	0.380	1.02
F IN.	0.120	0.145	0.120	0.145	0.120	0.145
MM	3.05	3.68	3.05	3.68	3.05	3.68
G IN.	0.090	0.110	0.090	0.110	0.090	0.110
MM	2.29	2.79	2.29	2.79	2.29	2.79
H IN	0.625	0.675	0.625	0.675	0.625	0.675
MM	15.88	17.15	15.88	17.15	15.88	17.15
J IN	0.008	0.012	0.008	0.012	0.008	0.012
MM	0.20	0.30	0.20	0.30	0.20	0.30
K IN.	0.015	0.022	0.015	0.022	0.015	0.022
MM	0.38	0.56	0.38	0.56	0.38	.56

8–PIN SOIC (150 MIL AND 200 MIL)





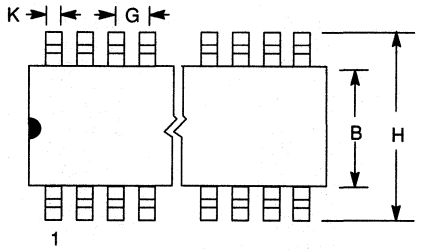


150 Mil Includes:
DS1000Z
DS1004Z
DS1012Z
DS1033Z
DS1035Z
DS1040Z
DS1218S
DS1830
DS2430
DS2502

200 Mil Includes:
DS1232LPS-2
DS1620S
DS1651S
DS1652S
DS1652B
DS1669S
DS1820S
DS1821S
DS1869

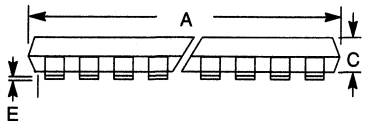
PKG	8-PIN (150 MIL)		8-PIN (200 MIL)	
DIM	MIN	MAX	MIN	MAX
A IN. MM	0.188 4.78	0.196 4.98	0.203 5.16	0.213 5.41
B IN. MM	0.150 3.81	0.158 4.01	0.203 5.16	0.213 5.41
C IN. MM	0.052 1.32	0.062 1.57	0.070 1.78	0.074 1.88
E IN. MM	0.004 0.10	0.010 0.25	0.004 0.10	0.010 0.25
F IN. MM	0.058 1.47	0.068 1.73	.074 1.88	.084 2.13
G IN. MM	.050 BSC 1.27 BSC			
H IN MM	0.230 5.84	0.244 6.20	0.302 7.67	0.318 8.07
J IN MM	0.007 0.17	0.010 0.25	0.006 0.15	0.010 0.25
K IN. MM	0.013 0.33	0.019 0.49	0.013 0.33	0.020 0.51
L IN. MM	.016 .40	.035 .89	.019 0.48	.030 .76
PHI	0°	8°	0°	8°

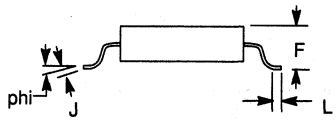
16–, 20–, AND 24–PIN SOIC (300 MIL)



Includes:

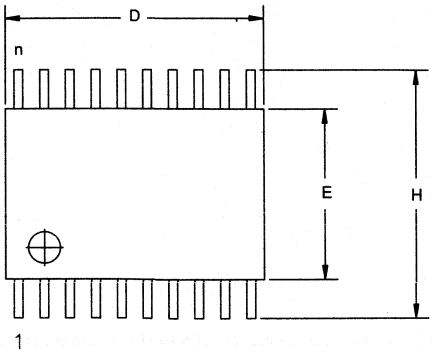
DS1000S	DS1221S	DS1259S
DS1005S	DS1222S	DS1267S
DS1007S	DS1231S	DS1336S
DS1010S	DS1228S	DS1609S
DS1013S	DS1229S	DS1632S
DS1020S	DS1232S	DS1640S
DS1045S	DS1232LPS	DS1653S
DS1200S	DS1234S	DS1666S
DS1205S	DS1236S	DS1667
DS1206	DS1237S	DS1867
DS1210S	DS1238S	DS1868
DS1211S	DS1239S	DS2404S–C01



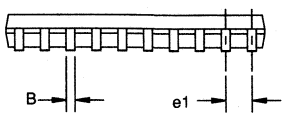


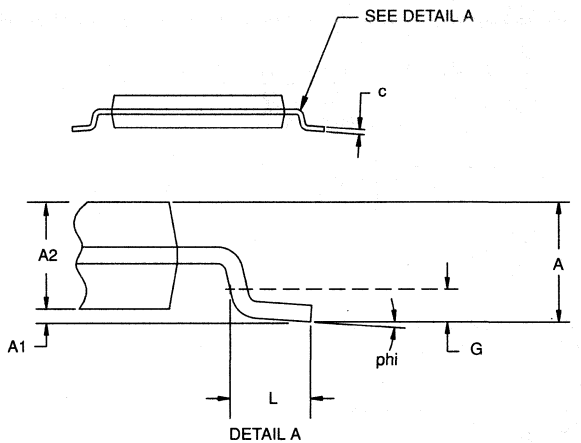
PKG	16-PIN		20-PIN		24-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX
A IN. MM	0.402 10.21	0.412 10.46	0.500 12.70	0.511 12.99	0.602 15.29	0.612 15.54
B IN. MM	0.290 7.37	0.300 7.65	0.290 7.37	0.300 7.65	0.290 7.37	0.300 7.65
C IN. MM	0.089 2.26	0.095 2.41	0.089 2.26	0.095 2.41	0.089 2.26	0.095 2.41
E IN. MM	0.004 0.102	0.012 0.30	0.004 0.102	0.012 0.30	0.004 0.102	0.012 0.30
F IN. MM	0.094 2.38	0.105 2.68	0.094 2.38	0.105 2.68	0.094 2.38	0.105 2.68
G IN. MM	.050 BSC 1.27 BSC					
H IN MM	0.398 10.11	0.416 10.57	0.398 10.11	0.416 10.57	0.398 10.11	0.416 10.57
J IN MM	0.009 0.229	0.013 0.33	0.009 0.229	0.013 0.33	0.009 0.229	0.013 0.33
K IN. MM	0.013 0.33	0.019 0.48	0.013 0.33	0.019 0.48	0.013 0.33	0.019 0.48
L IN MM	.016 .40	.040 1.02	.016 .406	.040 1.20	.016 .40	.040 1.02
PHI	0°	8°	0°	8°	0°	8°

20-PIN TSSOP



Includes:
DS1033E
DS1035E
DS1802
DS1867
DS2430



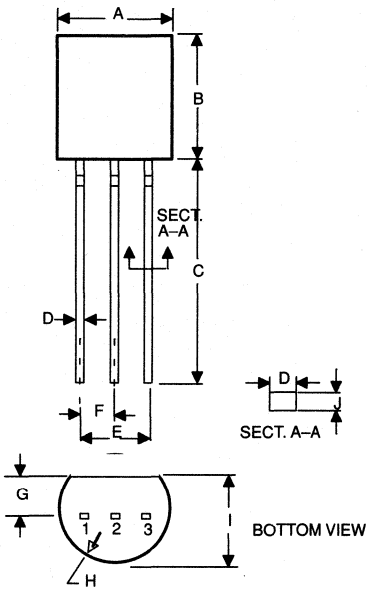


DIM	MIN	MAX
A MM	–	1.10
A1 MM	0.05	–
A2 MM	0.75	1.05
C MM	0.09	0.18
L MM	0.50	0.70
e1 MM	0.65 BSC	
B MM	0.18	0.30
D MM	6.40	6.90
E MM	4.40 NOM	
G MM	0.25 REF	
H MM	6.25	6.55
phi	0°	8°

TO-92 PACKAGE

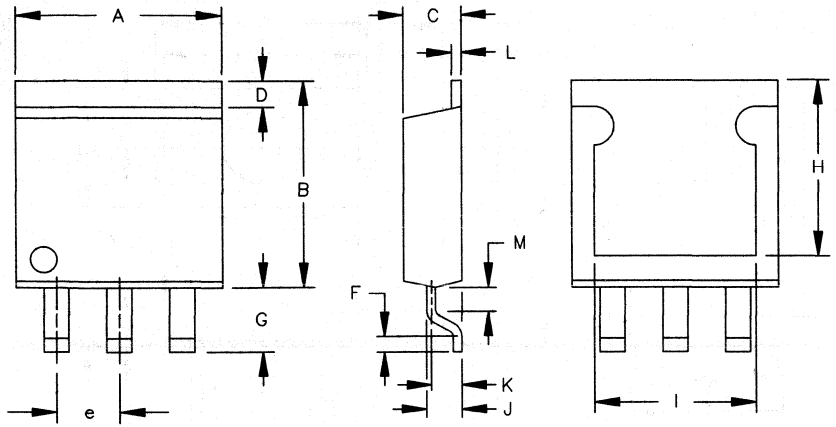
Includes:

DS1233
DS1233A
DS1233D
DS1833
DS2223
DS2224
DS2401
DS2405
DS2430
DS2502
DS2505



PKG	TO-92	
DIM	MIN	MAX
A IN.	0.175	0.195
MM	4.45	4.96
B IN.	0.170	0.195
MM	4.32	4.96
C IN.	0.500	0.610
MM	12.70	15.49
D IN.	0.016	0.022
MM	0.406	0.559
E IN.	0.095	0.105
MM	2.41	2.67
F IN.	0.045	0.060
MM	1.14	1.52
G IN.	0.45	0.060
MM	1.14	1.52
H IN	0.085	0.095
MM	2.16	2.41
I IN	0.130	0.155
MM	3.30	3.94
J IN	0.014	0.020
MM	0.35	0.51

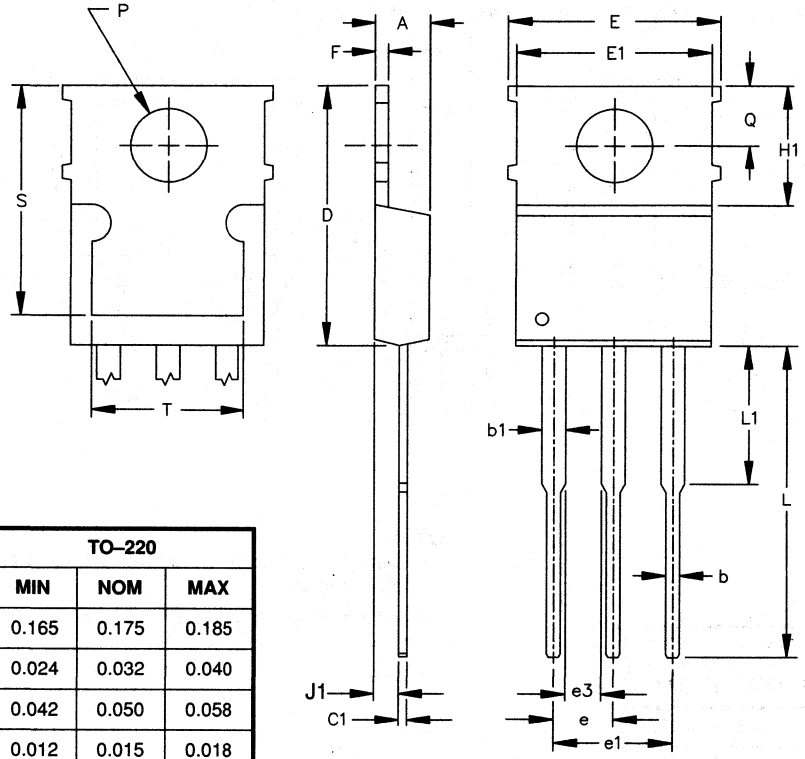
3L D2PAK (TO–220 TABLESS)



NOTES:
1. Dimensions F and M are measured to the center of radius.
2. All dimensions are shown in inches.

PKG	TO–220		
DIM	MIN	NOM	MAX
A	0.386	0.396	0.406
B	0.410	0.420	0.430
C	0.160	0.170	0.180
D	0.035	0.045	0.055
e	0.095	0.105	0.115
F	0.025	0.035	0.045
G	0.125	0.135	0.145
H	0.265	0.275	0.285
I	0.195	0.205	0.215
J	0.088	0.098	0.108
K	0.080	0.090	0.100
L	0.040	0.050	0.060
M	0.070	0.080	0.090

3L TO–220



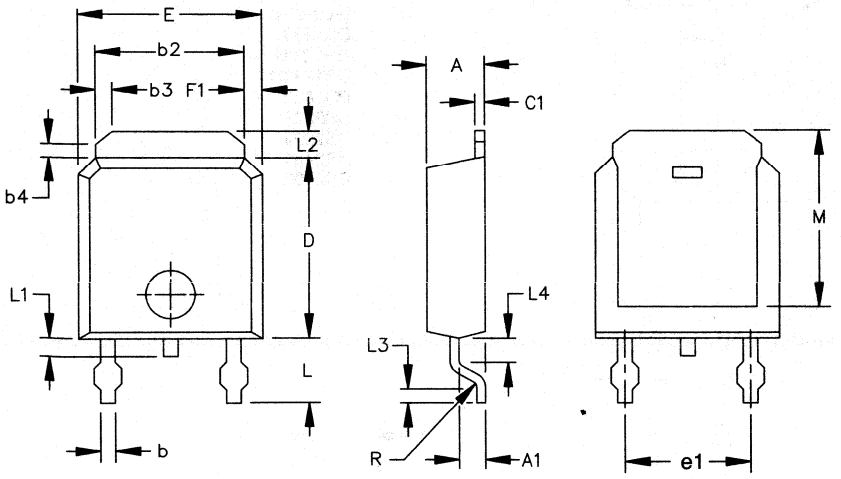
Includes:
DS1633
DS1821T
DS1837

PKG	TO–220		
DIM	MIN	NOM	MAX
A	0.165	0.175	0.185
b	0.024	0.032	0.040
b1	0.042	0.050	0.058
C1	0.012	0.015	0.018
D	0.573	0.588	0.603
E	0.394	0.404	0.414
E1	0.390	0.400	0.410
e	0.090	0.100	0.110
e1	0.190	0.200	0.210
e3	0.045	0.050	0.055
F	0.045	0.050	0.055
H1	0.236	0.248	0.260
J1	0.095	0.105	0.115
L	0.535	0.545	0.555
L1	0.220	0.230	0.240
P	0.146	0.151	0.156
Q	0.100	0.108	0.116
S	0.465	0.475	0.485
T	0.195	0.205	0.215

All dimensions are shown in inches.

3L DPAK (TO–252)

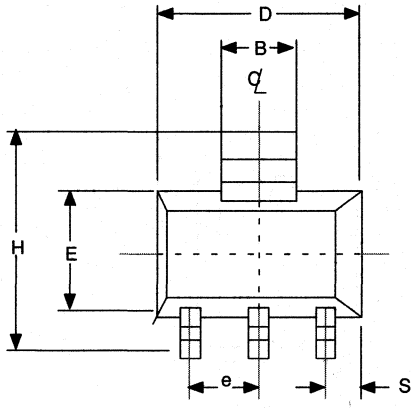
Includes:
DS1837



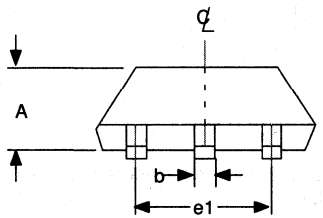
PKG	TO–252		
DIM	MIN	NOM	MAX
A	0.080	0.090	0.100
A1	0.035	0.040	0.045
b	0.025	0.030	0.035
b2	0.205	0.210	0.215
b3	0.030	0.035	0.040
b4	0.020	0.025	0.030
C1	0.018	0.020	0.023
D	0.230	0.240	0.250
E	0.250	0.260	0.270
F1	0.020	0.025	0.030
L	0.090	0.100	0.110
L1	0.010	0.025	0.040
L2	0.030	0.040	0.050
L3	0.021	0.024	0.028
L4	0.033	0.038	0.043
M	0.165	0.175	0.185
e1	0.170	0.180	0.190
R	0.008	0.010	0.012

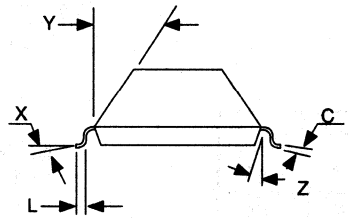
NOTE:
1. Dimensions L3 and L4 are measured to the center of radius.
2. All dimensions are shown in inches.

SOT–223 PACKAGE



Includes:
DS1233
DS1233A
DS1233D
DS1833
DS2223
DS2224
DS2401
DS2405

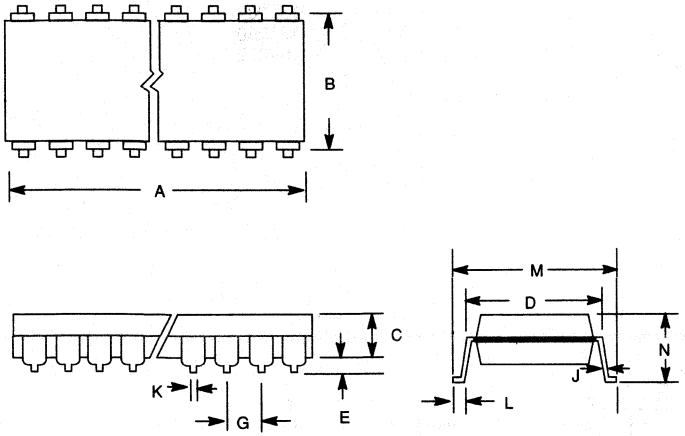




DIM	INCHES	
	MIN	MAX
A	–	0.067
B	0.025	0.033
B	0.116	0.124
C	0.009	0.013
D	0.248	0.263
E	0.0905 TYP.	
E1	0.181 TYP.	
E	0.130	0.145
H	0.264	0.287
L	0.016	0.036
S	0.033	0.041
X	10° MAX	
Y	10°	20°
Z	10°	20°

8- TO 20-PIN GULLWING (300 MIL)

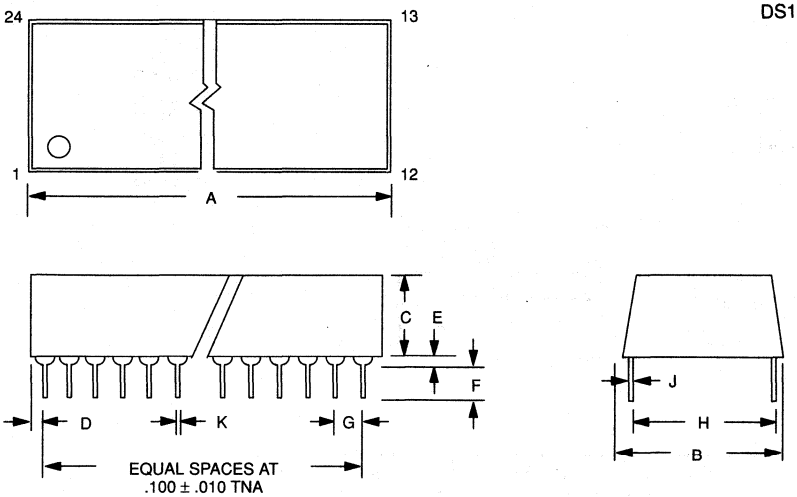
Includes:
DS1000G
DS1000H
DS1003G
DS1003H
DS1005G
DS1005H
DS1010G
DS1012H
DS1013G
DS1013H
DS1040H
DS1044G



PKG	8-PIN		14-PIN		16-PIN		20-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	0.345	0.400	0.740	0.780	0.740	0.780	0.960	1.040
MM	8.76	10.16	12.19	13.20	18.79	9.81	24.38	26.41
B IN.	0.240	0.260	0.240	0.260	0.240	0.260	0.240	0.260
MM	6.10	6.60	6.10	6.60	6.10	6.60	6.10	6.60
C IN.	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140
MM	3.05	3.56	3.05	3.56	3.05	3.56	3.05	3.56
D IN.	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325
MM	7.62	8.26	7.62	8.26	7.62	8.26	7.62	8.26
E IN.	0.020	0.040	0.020	0.040	0.020	0.040	0.020	0.040
MM	0.51	1.02	0.51	1.02	0.51	1.02	0.51	1.02
G IN.	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
MM	2.29	2.79	2.29	2.79	2.29	2.79	2.29	2.79
J IN.	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
MM	0.20	0.30	0.20	0.30	0.20	0.30	0.20	0.30
K IN.	0.015	0.021	0.015	0.021	0.015	0.021	0.015	0.021
MM	0.38	0.53	0.38	0.53	0.38	0.53	0.38	0.53
L IN.	0.030	0.050	0.030	0.050	0.030	0.050	0.030	0.050
MM	0.76	1.27	0.76	1.27	0.76	1.27	0.76	1.27
M IN.	0.370	0.420	0.370	0.420	0.370	0.420	0.370	0.420
MM	9.40	10.67	9.40	10.67	9.40	10.67	9.40	10.67
N IN.	0.160	0.180	0.160	0.180	0.160	0.180	0.160	0.180
MM	4.06	4.57	4.06	4.57	4.06	4.57	4.06	4.57

16- AND 24- PIN ENCAPSULATED PACKAGE (FLUSH BOTTOM – 450 MIL.)

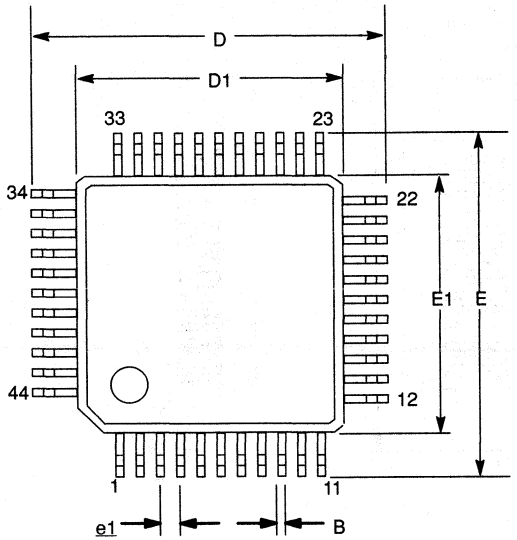
Includes:
DS1287
DS1287A
DS1290
DS1292

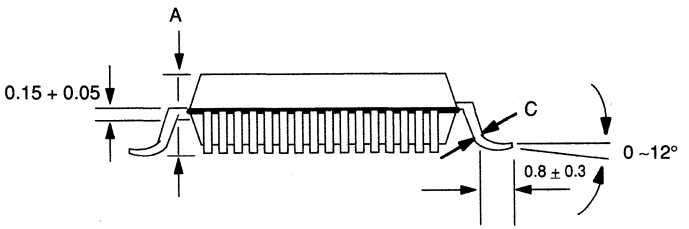


PKG	16-PIN		24-PIN	
DIM	MIN	MAX	MIN	MAX
A IN.	0.820	0.840	1.310	1.330
MM	20.83	21.34	33.27	33.78
B IN.	0.440	0.460	0.440	0.460
MM	11.18	11.68	11.18	11.68
C IN.	0.330	0.370	0.330	0.370
MM	8.38	9.40	8.38	9.40
D IN.	0.180	0.210	0.215	0.245
MM	4.57	5.33	5.46	6.22
E IN.	0.020	0.040	0.020	0.040
MM	0.51	1.02	0.51	1.02
F IN.	0.110	0.140	0.110	0.140
MM	2.79	3.56	2.79	3.56
G IN.	0.090	0.110	0.090	0.110
MM	2.29	2.79	2.29	2.79
H IN	0.330	0.380	0.330	0.380
MM	8.38	9.65	8.38	9.65
J IN	0.008	0.012	0.008	0.012
MM	0.20	0.31	0.20	0.31
K IN.	0.015	0.021	0.015	0.021
MM	0.38	0.53	0.38	0.53

44–PIN QUAD FLAT PACK (PRELIMINARY)

Includes:
DS1280

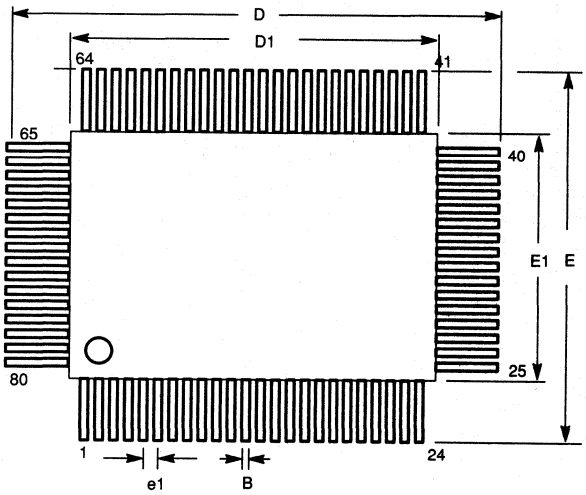


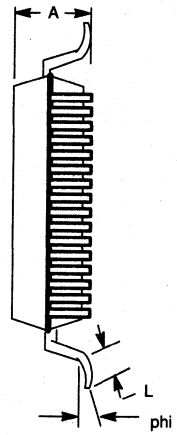


PKG	10 X 10 BODY		14 X 14 BODY	
DIM	MIN	MAX	MIN	MAX
A MM	–	2.45	–	3.4
B MM	0.30	0.45	0.20	0.50
C MM	0.13	0.23	0.10	0.20
D MM	13.65	14.35	16.95	18.00
E MM	13.65	14.35	16.95	18.00
D1 MM	9.90	10.10	13.80	14.20
E1 MM	9.90	10.10	13.80	14.20
L MM	0.65	0.95	0.50	1.10
e1 IN MM	0.315 0.80 BSC		0.039 1.00 BSC	

80-PIN QUAD FLAT PACK (14.0 MM X 20.0 MM)

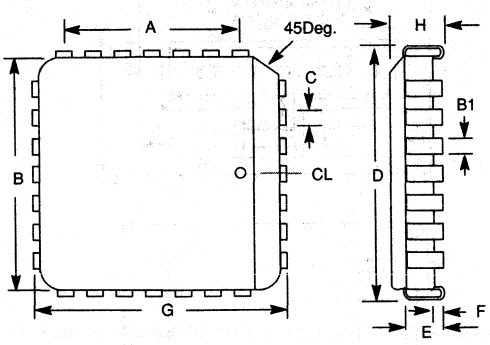
Includes:
DS1280

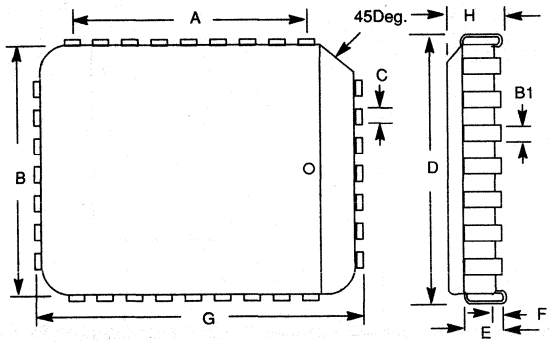




PKG	80-PIN	
DIM	MIN	MAX
A IN. MM	0.11 2.80	0.128 3.25
B IN. MM	0.010 0.25	0.020 0.45
e1 IN. MM	0.031 BSC 0.80 BSC	
D1 IN. MM	0.781 19.85	0.793 20.15
E1 IN. MM	0.545 13.85	0.557 14.15
E IN. MM	0.688 17.50	0.720 18.30
D IN. MM	0.921 23.40	0.953 24.20
L IN MM	0.025 0.65	0.038 0.95
phi	0°	8°

28- AND 32- PIN PLASTIC LEADED CHIP CARRIERS (PLCC)





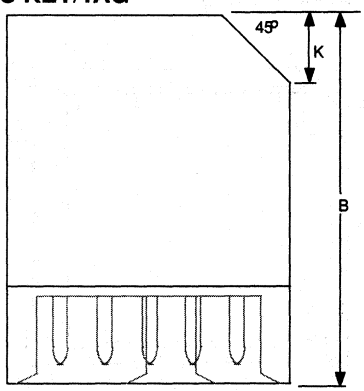
28- Pin Includes:
DS1212Q

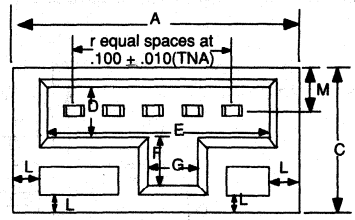
32-Pin Includes:
DS2009Q
DS2010Q
DS2011Q
DS2012Q

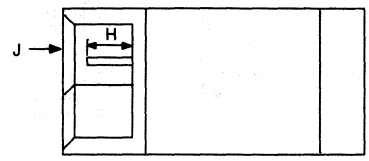
PKG	28-PIN		32-PIN	
DIM	MIN	MAX	MIN	MAX
A IN. MM	0.300 BSC 7.62		0.400 BSC 10.16	
B IN. MM	0.445 11.30	0.460 11.68	0.442 11.30	0.460 11.68
B1 IN MM	0.013 0.33	0.021 0.53	0.013 0.33	0.021 0.53
C IN MM	0.027 0.68	0.33 0.84	0.027 0.68	0.33 0.84
D IN. MM	0.480 12.19	0.500 12.70	0.480 12.19	0.500 12.70
D2 IN. MM	0.390 9.91	0.430 10.92	0.390 9.91	0.430 10.92
E IN. MM	0.090 2.29	0.120 3.05	0.060 1.52	0.095 2.41
E2 IN. MM	0.390 9.91	0.430 10.92	0.490 12.45	0.530 13.46
F IN. MM	0.020 0.51		0.015 0.38	
G IN MM	0.480 12.19	0.500 12.70	0.580 14.7	0.600 15.24
H IN MM	0.165 4.19	0.180 4.57	0.100 2.54	0.140 3.56

ELECTRONIC KEY/TAG

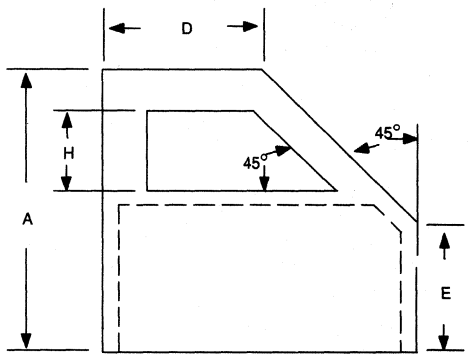
Includes:
DS1201
DS1204V
DS1205V
DS1207

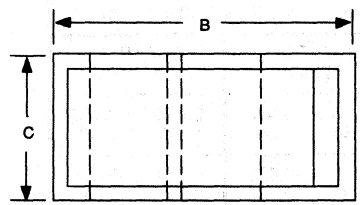






KEY/TAG CAP

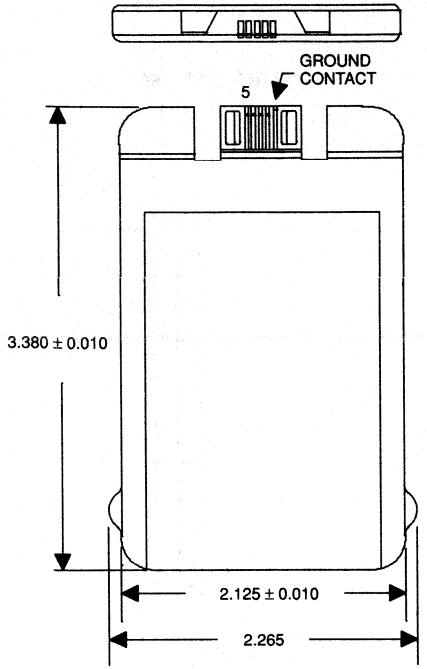


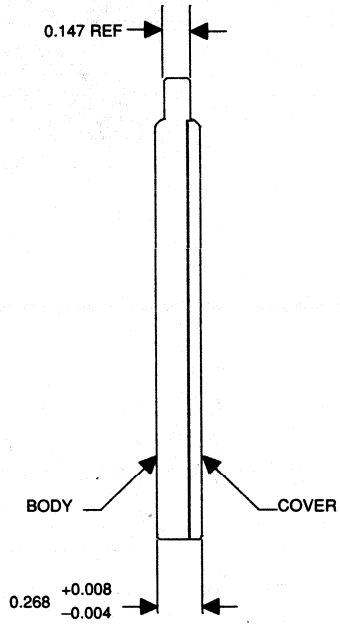


PKG	ELECTRONIC KEY/TAG		KEY/TAG CAP	
DIM	MIN	MAX	MIN	MAX
A IN. MM	0.610 15.50	0.650 16.51	0.790 20.07	0.810 20.57
B IN. MM	0.740 18.80	0.760 19.30	0.680 17.27	0.700 17.78

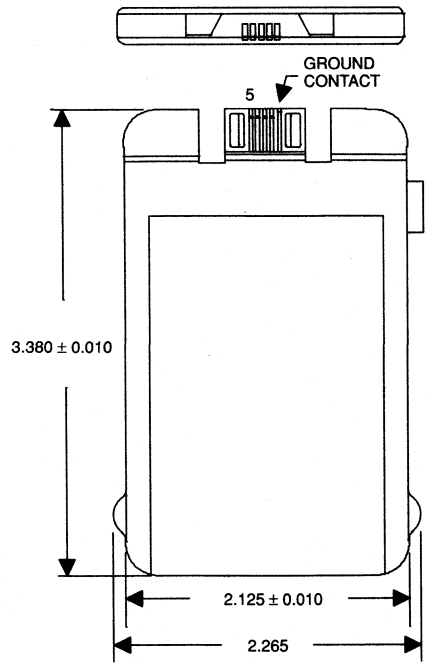
C IN. MM	0.310 7.87	0.355 9.02	0.405 10.29	0.425 10.80
D IN. MM	0.100 2.54	0.110 2.79	0.290 7.37	0.310 7.87
E IN. MM	0.505 12.83	0.515 13.08	0.410 10.41	0.430 10.92
F IN. MM	0.100 2.54	0.110 2.79		

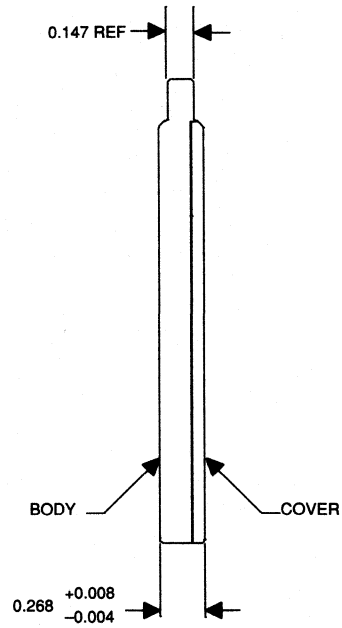
CYBERCARD PACKAGE, NON–POLARIZED



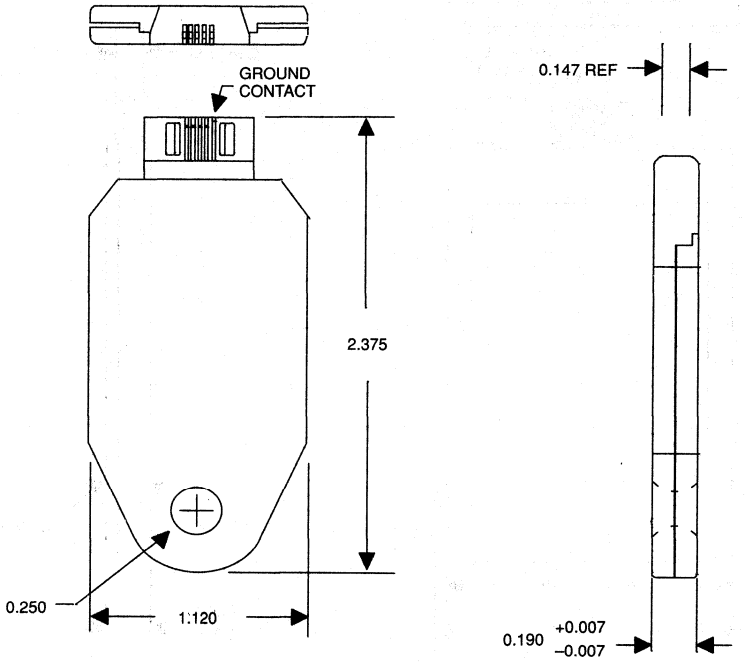


CYBERCARD PACKAGE, POLARIZED

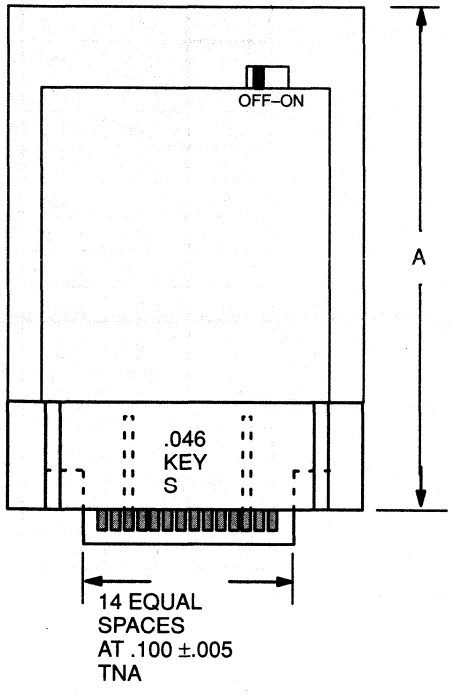




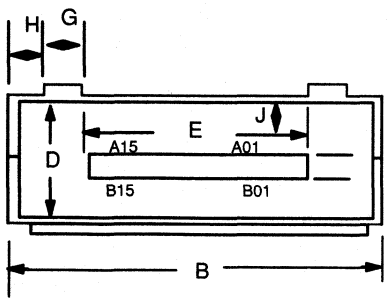
CYBERKEY PACKAGE

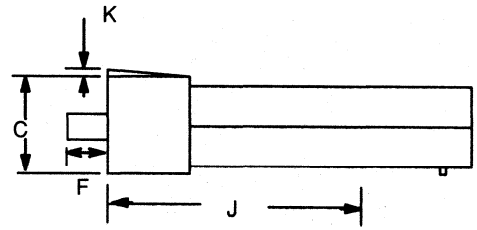


NON-VOLATILE READ/WRITE CARTRIDGE

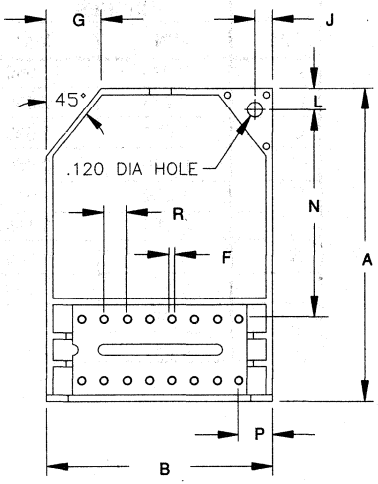


	INCHES	
DIM	MIN	MAX
A	3.020	3.040
B	2.275	2.295
C	0.600	0.630
D	0.440	0.460
E	1.590	1.607
F	0.115	0.135
G	0.115	0.135
H	0.140	0.160
J	1.760	1.790
K	0.040	0.060



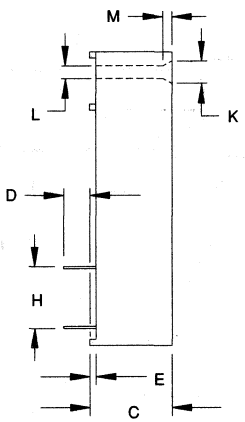


DS1260 SMART BATTERY

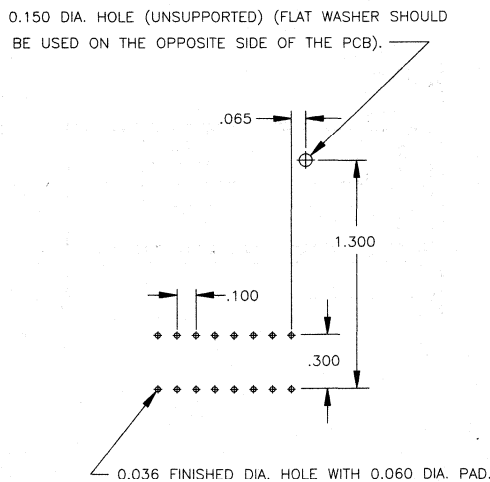


BOTTOM VIEW

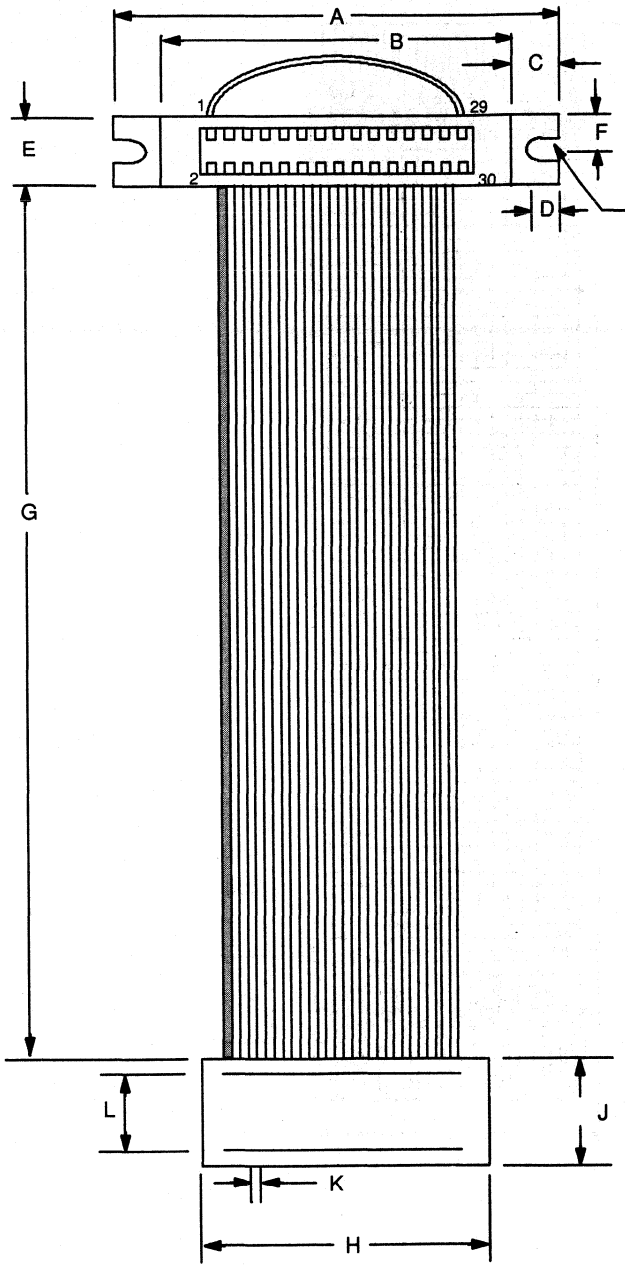
DIM	INCHES	
	MIN	MAX
A	1.480	1.500
B	1.030	1.050
C	0.390	0.415
D	0.125	0.145
E	0.020	0.040
F	0.016	0.020
G	0.240	0.260
H	0.295	0.315
J	0.090	0.110
K	0.160	0.180
L	0.110	0.130
M	0.035	0.065
N	0.985	1.010
P	0.155	0.175
R	0.095	0.105



SIDE VIEW



BYTEWIDE CABLE HARNESS



DIM.	INCHES	
	MIN.	MAX.
A	2.480	2.520
B	1.940	1.980
C	.260	.280
D	.160	.175
E	.395	.415
F	.195	.205
G	5.25	5.65
H	1.470	1.500
J	.715	.735
K	.090	.110
L	.590	.610

NOTES: COLOR STRIPE INDICATES PIN 1
END ON 28-PIN PULG.
DIMENSION L IS CENTER TO CENTER

DS9003
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BOARD